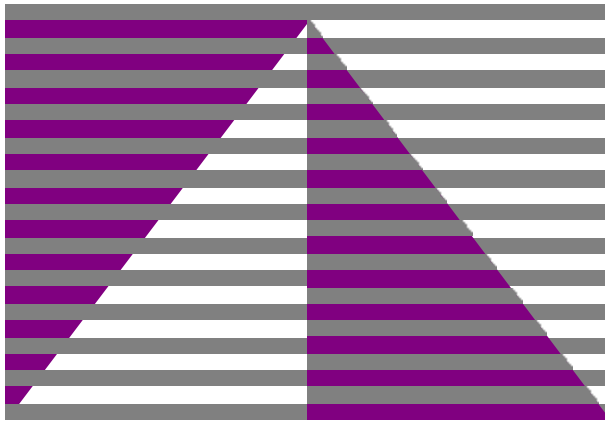


# The 27<sup>th</sup> Annual International Symposium on Computer Architecture



## *Final Program*

June 10-14, 2000  
Vancouver, British Columbia, Canada



Sponsored by the ACM Special  
Interest Group on Computer  
Architecture and the IEEE  
Computer Society Technical  
Committee on Computer Architecture



## Saturday, June 10

07:30 – 08:30 Bayshore Ballroom Foyer Breakfast

08:30 – 18:00 Salon A

**Workshop 4: Scalable Shared Memory Multiprocessors**

Jeff Kuskin (*Growth Networks*), Ashwini Nanda (*IBM*) and Josep Torrellas (*University of Illinois*), organizers

09:00 – 17:00 Thompson

**Workshop 3: Computer Architecture Education**

Edward F. Gehringer (*North Carolina State University*), organizer

08:30 – 18:00 Salon B

**Workshop 1: Complexity-Effective Design**

David H. Albonesi (*University of Rochester*), Pradip Bose (*IBM*) and Subbarao Palacharla (*Intel*), organizers

14:00 – 18:00 Seymour

**Tutorial 1: IA-64 Architecture and Compiler Technology**

Jesse Fang, Wei Li, and Hans Mulder (*Intel Corporation*)

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## Sunday, June 11

07:30 – 08:30 Bayshore Ballroom Foyer Breakfast

08:00 – 18:00 Salon A

**Workshop 2: Solving the Memory Wall Problem**

Haldun Hadimioglu (*Polytechnic University*), David Kaeli (*Northeastern University*), organizers

08:30 – 18:00 Seymour

**Tutorial 2: Low Power Design: From Soup to Nuts**

Mary Jane Irwin and Vijaykrishnan Narayanan (*Penn State University*)

08:30 – 12:30 Thompson

**Tutorial 3: High Performance Cluster Computing: Architecture, Systems, and Applications**

Rajkumar Buyya (*Monash University*)

14:00 – 18:00 Thompson

**Tutorial 4: Emerging Processor Techniques for General-Purpose and Embedded Computing**

Sriram Vajapeyam (*Indian Institute of Science*)

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18:00 – 20:00

## Welcome Reception

*Garden/pool area of the Westin Bayshore Hotel*  
(Salon C in the event of inclement weather)

## Monday, June 12

07:30 – 08:30 Bayshore Ballroom Foyer Breakfast

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08:30 – 10:00 Salon AB

### Welcome and Keynote Address

All the Chips Outside: The Architecture Challenge  
*Gordon Bell (Microsoft)*

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10:00 – 10:30 Bayshore Ballroom Foyer Break

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10:30 – 12:00 Salon AB

### Session 1 - Using Threads

Session Chair: Brad Calder (*UC San Diego*)

- A Scalable Approach to Thread-Level Speculation  
*J. Gregory Steffan, Christopher Colohan, Antonia Zhai, Todd Mowry (Carnegie Mellon University)*
  - Architectural Support for Scalable Speculative Parallelization in Shared-Memory Multiprocessors  
*Marcelo Cintra, José Martinez, Josep Torrellas (University of Illinois)*
  - Transient Fault Detection via Simultaneous Multithreading  
*Steven Reinhardt (University of Michigan), Shubhendu Mukherjee (Compaq Computer Corporation)*
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12:00 – 13:30 Lunch (on your own)

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13:30 – 15:00 Salon A

### Session 2a - Exploiting Traces

Session Chair: Tom Conte (*NC State*)

- Trace Preconstruction  
*Quinn Jacobson (Sun Microsystems), James E. Smith (University of Wisconsin)*
- Completion-Time Multiple-Branch Prediction for Enhancing Trace Cache Performance  
*Ryan Rakvic, Bryan Black, John Paul Shen (Carnegie Mellon University)*
- A Hardware Mechanism for Dynamic Extraction and Relay of Program Hot Spots  
*Matthew Merten, Andrew Trick, Erik Nystrom, Ronald Barnes, Wen-mei Hwu (University of Illinois)*

## Monday, June 12

13:30 – 15:00 Salon B

### Session 2b - Modeling Performance and Power

Session Chair: Dirk Grunvald (University of Colorado)

- HLS: Combining Statistical and Symbolic Simulation to Guide Microprocessor Designs  
*Mark Oskin, Frederic Chong, Matthew Farrens (U.C. Davis)*
  - Wattch: A Framework for Architectural-Level Power Analysis and Optimizations  
*David Brooks (Princeton University), Vivek Tiwari (Intel Corporation), Margaret Martonosi (Princeton University)*
  - Energy-Driven Integrated Hardware-Software Optimizations Using SimplePower  
*N. Vijaykrishnan., Mahmut Kandemir, Mary Jane Irwin, Hyun Kim, Wu Ye (Penn State)*
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15:00 – 15:30 Bayshore Ballroom Foyer Break

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15:30 – 17:00 Salon AB

### Session 3 - Memory Hierarchy Improvements

Session Chair: Kourosh Gharachorloo (*Compaq Computer Corporation*)

- A Fully Associative Software-Managed Cache  
*Erik Hallnor, Steven Reinhardt (University of Michigan)*
  - Recency-based TLB Preloading  
*Ashley Saulsbury (Sun Microsystems), Fredrik Dahlgren (Ericsson Mobile Communications), Per Stenström (Chalmers University)*
  - Memory Access Scheduling  
*Scott Rixner, William Dally, Ujval Kapasi, Peter Mattson, John Owens (Stanford University)*
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## Excursion to the Museum of Anthropology, University of British Columbia

Board buses from 17:45 to 18:15

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## Tuesday, June 13

07:30 – 08:30 Bayshore Ballroom Foyer Breakfast

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08:30 – 10:00 Salon AB

### Session 4 – Multiprocessors

Session Chair: Per Stenström (*Chalmers University*)

- Selective, Accurate and Timely Self-Invalidation Using Last-Touch Prediction  
*An-Chow Lai, Babak Falsafi (Purdue University)*
  - An Embedded DRAM Architecture for Large-Scale Spatial-Lattice Computations  
*Norman Margolus (MIT Artificial Intelligence Laboratory)*
  - Smart Memories: A Modular Reconfigurable Architecture  
*Kenneth Mai, Timothy Paaske, Nuwan Jayasena, Ron Ho, William Dally, Mark Horowitz (Stanford University)*
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10:00 – 10:30 Bayshore Ballroom Foyer Break

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10:30 – 12:00 Salon A

### Session 5a - Analysis of Workloads and Systems

Session Chair: Antonio González (*UPC*)

- Understanding the Backward Slices of Performance Degrading Instructions  
*Craig Zilles, Gurindar Sohi (University of Wisconsin)*
- On the Value Locality of Store Instructions  
*Kevin Lepak, Mikko Lipasti (University of Wisconsin)*
- Performance Analysis of the Alpha 21264-based Compaq ES40 System  
*Zarka Cvetanovic, R. E. Kessler (Compaq Computer Corporation)*

10:30 – 12:00 Salon B

### Session 5b - Customizable Systems

Session Chair: Margaret Martonosi (*Princeton University*)

- Lx: A Technology Platform for Customizable VLIW Embedded Processing  
*Paolo Faraboschi, Joseph Fisher, Geoffrey Brown, Giuseppe Desoli (Hewlett-Packard Laboratories), Fred Homewood (ST Microelectronics)*
- Reconfigurable Caches and their Application to Media Processing  
*Parthasarathy Ranganathan (Rice University), Sarita Adve (University of Illinois), Norman Jouppi (Compaq Western Research Lab)*
- CHIMAERA: A High Performance Architecture with a Tightly-Coupled Reconfigurable Functional Unit  
*Alex Ye, Prithviraj Banerjee, Andreas Moshovos (Northwestern University), Scott Hauck (Washington University)*

## Tuesday, June 13

12:00 – 14:00 Salon DE  
Eckert-Mauchly Award Luncheon

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14:00 – 15:00 Salon AB

### Session 6 - Circuit Considerations

Session Chair: Ravi Nair (*IBM*)

- Circuits for Wide-Window Superscalar Processors  
*Dana Henry, Bradley Kuszmaul, Gabriel Loh, Rahul Sami (Yale)*
  - Clock Rate versus IPC: The End of the Road for Conventional Microarchitectures  
*Vikas Agarwal, M. S. Hrishikesh, Stephen Keckler, Doug Burger (University of Texas)*
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15:00 – 15:30 Bayshore Ballroom Foyer Break

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15:30 – 17:00 Salon AB

### Panel Discussion

Slow Wires, Hot Chips and Leaky Transistors: New Challenges in the New Millennium

Moderator: *Shubu Mukherjee (Compaq Corporation)*

Panelists: *Bob Colwell (Intel), Dirk Grunwald (University of Colorado), Mark Horowitz (Stanford University), Norm Jouppi (Compaq Computer Corporation), T. N. Vijaykumar (Purdue University), Jim Smith (University of Wisconsin)*

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18:00 – 20:00 Salon AB

ACM/SIGARCH and IEEE-CS/TCCA business meeting

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## Wednesday, June 14

**07:30 – 08:30 Bayshore Ballroom Foyer Breakfast**

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### **08:30 – 10:00 Salon DE**

#### **Session 7 - Extracting Parallelism**

Session Chair: David Wood (*University of Wisconsin*)

- Vector Instruction Set Support for Conditional Operations  
*James Smith (University of Wisconsin), Greg Faanes (SGI/Cray Research), Rabin Sugumar (Sun Microsystems)*
  - Instruction Path Coprocessors  
*Yuan Chou, John Paul Shen (Carnegie Mellon University)*
  - Piranha: A Scalable Architecture Based on Single-Chip Multiprocessing  
*Luiz Barroso, Kourosh Gharachorloo, Robert McNamara, Andreas Nowatzky, Shaz Qadeer, Barton Sano, Scott Smith, Robert Stets, Ben Verghese (Compaq Computer Corporation)*
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**10:00 – 10:30 Bayshore Ballroom Foyer Break**

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### **10:30 – 12:00 Salon DE**

#### **Session 8 - Microarchitecture Innovations**

Session Chair: Matt Farrens (*UC Davis*)

- Allowing for ILP in an Embedded Java Processor  
*Ramesh Radhakrishnan, Deependra Talla, Lizy John (University of Texas)*
  - Early Load Address Resolution Via Register Tracking  
*Michael Bekerman (HAL Computer Systems), Adi Yoaz (Intel Corporation), Freddy Gabbay (Mellanox Technologies), Stephan Jourdan, Maxim Kalaev, Ronny Ronen (Intel Corporation)*
  - Multiple-Banked Register File Architectures  
*José Lorenzo Cruz, Antonio González, Mateo Valero (UPC Barcelona), Nigel Topham (Siroyan, Ltd.)*
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Saturday, 10 June to Tuesday, 13 June

07:30 – 18:00 Bayshore Ballroom Foyer

Registration

07:30 – 17:00 Fraser

Speaker preparation and Internet terminals  
(Internet Service provided by UBC-CS)

For more information, see:

<http://www.cs.rochester.edu/~ISCA2k/>

## Organizing Committee

**General Chair:** Alan Berenbaum, *Lucent*  
**Program Chair:** Joel Emer, *Compaq*  
**Finance Chair:** Cliff Young, *Lucent*  
**Tutorial Chair:** Sarita Adve, *Illinois*  
**Workshops Chair:** J.P. Singh, *Princeton*  
**Publicity Chair:** Sandhya Dwarkadas, *Rochester*  
**Local Arrangements:** Bob Ito, *UBC*

## Steering Committee

Paul Chow *Toronto* Bob Colwell *Intel*  
Allan Gottlieb *NYU* Mary Jane Irwin *Penn State*  
Andy Pleszkun *Colorado*

## Program Committee

Saman Amarasinghe *MIT* Todd Austin *Michigan*  
Brad Calder *UC San Diego* Tom Conte *NC State*  
Michel Dubois *USC* Matt Farrens *UC Davis*  
Josh Fisher *HP* Kourosh Gharachorloo *Compaq*  
Antonio González *UPC* Dirk Grunwald *Colorado*  
Mark Horowitz *Stanford* John Kubiawicz *Berkeley*  
Corinna Lee *ATI* Margaret Martonosi *Princeton*  
Todd Mowry *CMU* Dave Nagle *CMU*  
Ravi Nair *IBM* Jim Smith *Wisconsin*  
Mike Smith *Harvard* Per Stenström *Chalmers*  
Uri Weiser *Intel* David Wood *Wisconsin*