

Curriculum Vitae

Arrvindh Shriraman

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Education

Pursuing a Ph.D. in Computer Science, expected Summer 2010

University of Rochester, Rochester, NY.

Thesis: Architectural Support for Monitoring, Isolating, and Protecting Memory in Multiprocessors.

Advisor: Prof. Sandhya Dwarkadas

M.S. in Computer Science, May 2006

University of Rochester, Rochester, NY.

Area Paper: Evolution of Hardware Support for Transactional Memory.

B.Engg. in Computer Science, July 2004

University of Madras, Chennai, TN, India.

Undergraduate Thesis: PASCOM - Power model for Supercomputers.

Advisor: Prof. Nagarajan Venkateswaran

Research Interests

Multiprocessor and multicore memory system design, hardware-software interface, hardware support for improving software debugging and reliability, and programming models for multiprocessors.

Publications

Journals and Magazines

1. *"Flexible Decoupled Transactional Memory Support,"* A. Shriraman, S. Dwarkadas, and M. L. Scott. Journal of Parallel and Distributed Computing (JPDC) Special issue on Transactional Memory, 2010.
2. *"Tapping into Parallelism with Transactional Memory,"* A. Shriraman, S. Dwarkadas, and M. L. Scott. ;login: The USENIX Magazine, Apr 2009.
3. *"Analyzing Conflicts in Hardware-Supported Memory Transactions,"* A. Shriraman and S. Dwarkadas. International Journal of Parallel Programming, 2010. **(ICS'09 Award Paper)**

Refereed Conferences

4. *"Sentry: An Auxiliary Memory Access Control,"* A. Shriraman and S. Dwarkadas. 37th Intl. Symposium on Computer Architecture (**ISCA**), 2010.
 5. *"Refereeing Conflicts in Hardware Transactional Memory,"* A. Shriraman and S. Dwarkadas. 23rd Intl. Conf. on Supercomputing (**ICS**), June 2009. Shortlisted amongst top six papers for IJPP Journal.
 6. *"Flexible Decoupled Transactional Memory Support,"* A. Shriraman, S. Dwarkadas, and M. L. Scott. 35th Intl. Symp. on Computer Architecture (**ISCA**), June 2008. Extended version appears as TR-925.
 7. *"An Integrated Hardware-Software Approach to Flexible Transactional Memory,"* A. Shriraman, M. F. Spear, H. Hossain, V. Marathe, S. Dwarkadas, and M. L. Scott. 34th Intl. Symp. on Computer Architecture (**ISCA**), June 2007. Extended version appears as TR-910.
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8. "Nonblocking Transactions Without Indirection Using Alert-on-Update," M. F. Spear, A. Shriraman, L. Dalessandro, S. Dwarkadas, and M. L. Scott. 19th ACM Symp. on Parallelism in Algorithms and Architectures (**SPAA**), June 2007.
9. "Alert-on-Update: A Communication Aid for Shared Memory Multiprocessors,"(Poster Paper) M. F. Spear, A. Shriraman, H. Hossain, S. Dwarkadas, and M. L. Scott. 11th ACM Symp. on Principles and Practice of Parallel Programming (**PPOPP**), March 2007.
10. "PASCOM: Power Model for Supercomputers," A. Shriraman, N. Venkateswaran, and S. Niranjana. 19th Intl. Conference on Architecture of Computing Systems (**ARCS**), March 2006.

Newsletters and Refereed Workshops

11. "Transactional Mutex Locks," M. F. Spear, A. Shriraman, L. Dalessandro and M. L. Scott. Workshop on Languages, Compilers, and Hardware Support for Transactional Computing (**TRANSACT**), held in conjunction with **HPCA**, Feb 2009.
12. "Hardware Acceleration of Software Transactional Memory," A. Shriraman, V. Marathe, S. Dwarkadas, M. L. Scott, D. Eisenstat, C. Heriot, W. N. Scherer III, and M. F. Spear. Workshop on Languages, Compilers, and Hardware Support for Transactional Computing (**TRANSACT**), held in conjunction with **PLDI**, June 2006. Extended version appears as TR-887.
13. "Memory In Processor-SuperComputer On a Chip : Processor Design and Execution Semantics for Massive On-Chip Parallelism," N. Venkateswaran, A. Shriraman, and S. Niranjana. Workshop on Massively Parallel Processing (**WMPP**), held in conjunction with **IPDPS**, April 2005.
14. "Memory In Processor: A Novel Design Paradigm for Supercomputing Architectures," N. Venkateswaran, A. Krishnan, A. Shriraman, S. Niranjana, and S. Srinivas. **ACM Computer Architecture News**, June 2004.

Work-In-Progress

15. "DIMM: Architecture Support for Data Isolation and Memory Monitoring," A. Shriraman and S. Dwarkadas. 13th Intl. Symp. on Architectural Support for Programming Languages and Operating Systems (**ASPLOS**), March 2008.

Technical Reports

16. "Memory Monitoring: Hardware Mechanisms for Watching and Protecting Memory," A. Shriraman and S. Dwarkadas. Computer Sciences Technical Report #945, University of Rochester, 2009.

Work Experience

Fall 2004 - Present, Research Assistant

High-Performance Synchronization group, Advisor: Sandhya Dwarkadas

My dissertation research proposes hardware mechanisms to help software developers build fast, correct, and robust applications. These hardware mechanisms expose information in the memory system (e.g., which locations are cached) that helps programs understand their own behavior and react to it. I have developed the necessary software interface to demonstrate their use in high performance synchronization, low-overhead debugging, and improving software reliability. Our group was also the first to explore the use of such hardware mechanisms to accelerate software-based transactional memory, an emerging parallel programming model (as per Google scholar, the TRANSACT'05, ISCA'07, and ISCA'08 papers have received ~100 citations).

Summer 2005, Research Intern

Log & Lifeguards group, Intel Research, Pittsburgh; Advisor: Steve Schlosser

- I analyzed the information needed by debuggers and built a generic logging infrastructure on a dynamic instrumentation framework. I also developed a device model on a full-system simulator to emulate hardware support for logging.
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Spring 2005 - Spring 2006, Teaching Assistant

Department of Computer Science, University of Rochester

- Teaching assistant for courses in introductory computer programming (Spring'05, Fall'05). Led three discussion classes for a programming course.
- Teaching assistant for Parallel and Distributed Systems (Spring'06, Spring'09). Noteworthy responsibilities included setting up and evaluating assignments that required programming multiprocessors with various frameworks (e.g., pthreads, Cilk, OpenMP).
- I developed and maintained a php-based forum on which students can discuss problems and interact with TAs.

Software Development

My research lays emphasis on enabling new hardware functionality that software can exploit directly. This requires infrastructure across multiple levels in the system hierarchy. I have implemented my hardware mechanisms within a full-system emulation/simulation framework and developed C libraries to expose the new features to software developers. Specifically, I led the development of RTM [ISCA'07] transactional memory framework. Currently, I am working on using the Qemu emulation framework to develop a software version of Sentry [ISCA'10 submission].

Patents

- *System and Method for Hardware Acceleration of a Software Transactional Memory*, US Patent filed 12/2005 (Pending).
- *Flexible Decoupled Transactional Memory Support*, US Patent filed 12/2007 (Pending).

Invited and Conference Talks

Presented papers at ISCA-34 (June 2007), ISCA-35 (June 2008), ICS-23 (June 2009).

Service

Paper Submission Chair for ISPASS'07 and TRANSACT'07.

Organizer of weekly computer systems seminar at the University of Rochester, 2006-2009.

Reviewed papers for PACT'05, MICRO'05, ASPLOS'06, HPCA'08, ISCA'08, ISCA'09, MICRO'09, HPCA'10, ASPLOS'10, JPDC'10.

Personal Information

Date of Birth : January 9, 1983 Citizenship : India Visa status : F1

References

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