

Curriculum Vitae

Arrvindh Shriraman

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Education

Pursuing a Ph.D. in Computer Science, since Fall 2004

University of Rochester, Rochester, NY.

Thesis proposal: Architecture Support for Data Isolation and Memory Monitoring in Shared Memory Multiprocessors, May 2007

Advisor: Prof. Sandhya Dwarkadas

M.S. in Computer Science, May 2006

University of Rochester, Rochester, NY.

Area Paper: Evolution of Hardware Support for Transactional Memory, May 2006

B.Engg. in Computer Science, July 2004

University of Madras, Chennai, TN, India.

Undergraduate Thesis: PASCOM - Power model for Supercomputers

Advisor: Prof. Nagarajan Venkateswaran

Research Interests

Multiprocessor and multi-core memory system design, cache coherence protocols, on-chip interconnects, transactional memory, hardware-software interface and programming models for multiprocessor systems.

Work Experience

Fall 2004 - Present, Research Assistant

High-Performance Synchronization group, University of Rochester, Advisor: Sandhya Dwarkadas

- Developed generic decoupled hardware primitives for monitoring memory and software-transparent write isolation to permit usage across different application domains (e.g., TM, Debugging, Security). [ISCA'08]
- Developed the cache protocol and hardware support for the Rochester Transactional Memory (RTM) system. [ISCA'07, TRANSACT'06]
- Proposed a generic event trigger mechanism in cache coherent systems and evaluated acceleration application, elimination of read-set validation in software TMs. [SPAA'07, PPOPP'07 short paper]

Summer 2005, Research Intern

Log & Lifeguards group, Intel Research Lab, Pittsburgh. Advisor: Steve Schlosser

- Built a generic application-level logging infrastructure using Pin-based dynamic binary instrumentation. Developed a memory mapped device in Simics to simulate a hardware log device.

Fall 2002 - Summer 2004, Undergraduate Research Assistant

Advisor: Nagarajan Venkateswaran

- Played a leading role in the Memory In Processor (MIP) Supercomputer-On-A-Chip (S.C.O.C) microarchitecture design [MEDEA'03].
- Developed a power model and software framework for processing application traces to estimate the energy dissipated by multiprocessor systems [ARCS'06].

Spring 2005 - Spring 2006, Teaching Assistant

Department of Computer Science, University of Rochester

- Led three discussion classes for a programming course.
- Developed and maintained a php-based forum page for the students of an parallel and distributed systems course.

Publications

Journals and Magazines

1. "Tapping into Parallelism with Transactional Memory," A. Shriraman, S. Dwarkadas, and M. L. Scott. ;login: The USENIX Magazine, Apr 2009

Refereed Conferences

2. "Refereeing Conflicts in Hardware Transactional Memory," A. Shriraman and S. Dwarkadas 23rd Intl. Conf. on Supercomputing (**ICS**), June 2009. (Shortlisted amongst top six papers for IJPP Journal).
3. "Flexible Decoupled Transactional Memory Support," A. Shriraman, S. Dwarkadas, and M. L. Scott. 35th Intl. Symp. on Computer Architecture (**ISCA**), June 2008. Extended version appears as TR-925.
4. "An Integrated Hardware-Software Approach to Flexible Transactional Memory," A. Shriraman, M. F. Spear, H. Hossain, V. Marathe, S. Dwarkadas, and M. L. Scott. 34th Intl. Symp. on Computer Architecture (**ISCA**), June 2007. Extended version appears as TR-910.
5. "Nonblocking Transactions Without Indirection Using Alert-on-Update," M. F. Spear, A. Shriraman, L. Dalessandro, S. Dwarkadas, and M. L. Scott. 19th ACM Symp. on Parallelism in Algorithms and Architectures (**SPAA**), June 2007.
6. "Alert-on-Update: A Communication Aid for Shared Memory Multiprocessors,"(Poster Paper) M. F. Spear, A. Shriraman, H. Hossain, S. Dwarkadas, and M. L. Scott. 11th ACM Symp. on Principles and Practice of Parallel Programming (**PPOPP**), March 2007.
7. "PASCOM: Power Model for Supercomputers," A. Shriraman, N. Venkateswaran, and S. Niranjana. 19th Intl. Conference on Architecture of Computing Systems (**ARCS**), March 2006.

Newsletters and Refereed Workshops

8. "Transactional Mutex Locks," M. F. Spear, A. Shriraman, L. Dalessandro and M. L. Scott. Workshop on Languages, Compilers, and Hardware Support for Transactional Computing (**TRANSACT**), held in conjunction with **HPCA**, Feb 2009.
9. "Hardware Acceleration of Software Transactional Memory," A. Shriraman, V. Marathe, S. Dwarkadas, M. L. Scott, D. Eisenstat, C. Heriot, W. N. Scherer III, and M. F. Spear. Workshop on Languages, Compilers, and Hardware Support for Transactional Computing (**TRANSACT**), held in conjunction with **PLDI**, June 2006. Extended version appears as TR-887.
10. "Memory In Processor-SuperComputer On a Chip : Processor Design and Execution Semantics for Massive On-Chip Parallelism," N. Venkateswaran, A. Shriraman, and S. Niranjana. Workshop on Massively Parallel Processing (**WMPP**), held in conjunction with **IPDPS**, April 2005.
11. "Memory In Processor: A Novel Design Paradigm for Supercomputing Architectures," N. Venkateswaran, A. Krishnan, A. Shriraman, S. Niranjana, and S. Srinivas. **ACM Computer Architecture News**, June 2004.
12. "The MIP Project: Evolution of a Novel Supercomputer Architecture," N. Venkateswaran, A. Shriraman, A. Krishnan, S. Niranjana, and S. Srinivas. Workshop on MEMory performance: DEaling with Applications Systems & Architecture (**MEDEA**), held in conjunction with **PACT**, September 2003.

Work-In-Progress

13. "DIMM: Architecture Support for Data Isolation and Memory Monitoring," A. Shriraman and S. Dwarkadas. 13th Intl. Symp. on Architectural Support for Programming Languages and Operating Systems (**ASP-LOS**), March 2008.

Software Development

“FlexTM and RTM Transactional Memory Simulators”

Developed the simulation module using full system GEMS-Simics simulation framework. Extended the timing-only model of the GEMS framework to support data value logging for multi-versioning in the different caches of a TM system. Employed the “Magic” no-ops in Simics for defining new instructions to interface with the decoupled hardware primitives. Used the GEMS SLICC language to specify the complete TMESI cache protocol (including the transient states) under directory and snooping based systems.

Technical Proficiency

Programming	C/C++, Java, SQL, Assembly (x86,SPARC), Python
Linux Kernel	Medium user level
Tools	Virtutech Simics, Multifacet GEMS, SLICC cache protocol builder, SimpleScalar
Other Software	Matlab, Latex, Svn, CVS
Platforms	Linux, Solaris, Windows

Service

Reviewed papers for PACT'05, MICRO'05, ASPLOS'06, HPCA'08.
Paper Submission Chair for ISPASS'07 and TRANSACT'07.

Personal Information

Date of Birth : January 9, 1983
Citizenship : India
Visa status : F1

References

Sandhya Dwarkadas Professor Computer Science Department University of Rochester Rochester, NY 14627 sandhya@cs.rochester.edu	Michael Scott Professor Computer Science Department University of Rochester Rochester, NY 14627 scott@cs.rochester.edu
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