Cashmere-2L: Software Coherent Shared Memory on a Clustered Remote-Write Network

Jiasheng Shi
Background & Motivation

- Shared-memory programming model
- Hardware-coherent machines
- Software techniques
- Low-latency remote-write networks
  - DEC Memory Channel
Cashmere-2L

- Coherence Algorithm for SHared MEmory aRchitectures
- Primary Goals
  - Exploit hardware shared memory locally
  - Software overhead for only necessary communication
- Hardware Interface
  - 8-node, 32-processor DEC AlphaServer
  - DEC Memory Channel
Memory Channel

- Low-latency remote-write network
- Memory mapping
  - MC adapter & network
  - Mappings
  - Loop-back
- Synchronization Req.
Overview

- Moderately lazy RC
- Home-based protocol
- Directory-based coherence
- Exclusive mode
- Hardware Coherence exploitation
- Hardware-Software coherence interaction
  - Timestamp
  - Two-way diffing & shootdown
Directory-Based Coherence

- Global directory
- Synchronization objects
- Second-level directory
Directory-Based Coherence

- Other global meta-data

- Private to node
Directory-Based Coherence

- Write notice lists
Directory-Based Coherence

- Explicit requests
  - Interrupt
  - Polling
  - Code

```
label:
  ldq   $7, 0($13)  ; Check poll flag.
  beq   $7, nomsg   ; If message,
  jsr   $26, handler ; call handler.
  ldgp  $29, 0($26)  ; restore global pointer.
nomsg:
```
Home-Based Protocol

- Implementation
Home-Based Protocol

- Home node selection
  - Initialize
  - Relocate
- Superpage
Protocol Actions

- Page Faults
  - Directory update
  - Read & Write faults
- Acquires
  - Invalidation
  - Process write notices
- Releases
  - Page flush
  - Send outgoing diffs and write notices
Protocol Actions

- Example

Diagram:

- TWIN
  - $w(x)$
  - Rel
  - $x$

- DIFF
  - to home node

- P0
  - (data from home node)

- P1
  - mod(page(x))

- P2
  - Acq
  - inv(page(x))

- $r(x)$
Protocol Actions

- Twin Maintenance
  - Outgoing diffs
  - Incoming diffs

Compare up-to-date data to the twin.

Copy differences to the working copy and the twin.
Cashmere-1L VS TreadMark

- Cashmere-1L
- Performance Comparison
- Reasons

![Graph showing speedup comparison between TMK and CSM-1L for various benchmarks.](image-url)
Effect of Clustering

![Speedup Chart]

- **Speedup (32 processors)**
- **CSM-2L**
- **CSM-1L**

- SOR
- LU
- Water
- TSP
- Gauss
- Ilink
- Em3d
- Barnes
Summary

- Motivation and Background
- Hardware Interface (MC)
- Implementation Details
  - Home-based
  - Directory-based
  - Protocol Actions
  - Highly asynchronous
- Comparison to TreadMarks