The Sun Fireplane System Interconnect

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Overview

- Highly Scalable system (8-96 UltraSPARC-III processors)
- Scalability achieved through a 2-level coherence protocol
- Made possible by utilizing separate address and data interconnect
Cache Coherency Types

- **Broadcast (Snoopy) coherency**
  - Accesses to all memory addresses are announced on the bus
  - Processors snoop on the bus and manage their own cache
  - Low Latency, higher bandwidth usage
Cache Coherency Types

- **Point-to-point (Directory) coherency**
  - Hardware manages a directory and only sends messages to devices that are interested in the address
  - Higher Latency, lower bandwidth usage
  - Typically used only in large machines
Sunfire Cache Coherency

- Two-level coherency uses both Snoopy and Directory based coherency types for improved scalability and performance.
  - Snoopy for groups of < 24 Processors
  - Directory between groups of 24 Processors
Cache Tags

3 Sets of tags:

- Cache Tags
  - MOESI
- Dual Tags
  - Shared, Owned, Temporary, Invalid
- Mtags (Global)
  - Modified, Shared, Invalid
Cache Tags

Figure 5. Cache tag state transitions
Cache Tags

Dual Tags are used with Snooping Signals independent of data transfers

Cache Tags (MOESI) represent actual data state
Dual Tags

- **Shared**
  - Line is valid and clean
- **Owned**
  - Line is valid and potentially dirty
  - Represents MOE states
- **Temporary**
  - Line is valid and clean and exclusive
  - Waiting on Snoop input for possible Shared state
- **Invalid**
Cache Transfer with Single Domain

Figure 6. Read to share operation within a snooping coherence domain
Mtags

- Only used when there are more than 24 processors (set to Modified always in smaller systems)
- Stored in the ECC bytes in Memory for each 64-byte block
- Information is also cached in each group of 24 processors
Mtags

- Modified
  - Line is valid, exclusive, and possibly dirty
- Shared
  - Line is valid and clean in this domain and possibly others
- Invalid
Mtags Usage

To access non-local memory, a request is made to the SSM agent residing over that memory block. The agent maintains the Mtags and checks to see if a given domain is allowed access and provides the data.

A small set of requests exists for getting access to data when the Mtags prohibit it.
sync.cs.rochester.edu Specs

- SunFire V880
- SunOS 5.8
- 8 900 Mhz UltraSparc-III Processors
- 64 byte Cache lines
- 64 KB L1D Cache (Per Processor)
- 32 KB L1I Cache (Per Processor)
- 8 MB L2 Cache (Per Processor)
- 16 GB Main Memory
Where did they go from here?

- Server focused market
  - Concurrency and large thread count for web servers etc.
- “Niagara” Processor (UltraSPARC T1)
  - First Sun microprocessor to be both multicore and multithreaded (UltraSPARC-III was single core and single threaded)
  - Available with 4, 6, or 8 cores, each with 4 threads
  - Small pipeline, different thread at each stage of the pipeline, reduces cost of cache misses
  - Lower power consumption than comparable machines
Where did they go from here?

- Niagara 2 (UltraSPARC T2)
  - 8 threads per core each with its own FPU
- Niagara 3 - currently in development