

## Project Summary

### SHF:Small: Three-dimensional Systems-on-a-Chip

**Lead PI:** Yiming Gan, Computer Science Department, University of Rochester

The improvement on technology of size of transistors have been through an unavoidable slow down because of third reasons. First, with the shrink of the transistor size, the complexity of designing a chip will increase. The validation of the whole chip will become an impossible mission. Second, the size of a transistor now has become small as several nano-meters, keep shrinking will face multiple physical problems. Third, keep building smaller transistors will cause countless increase of cost. However, the slow down of technology doesn't mean the failure of Moore' law. People have been trying to make three-dimensional circuits for a long time. This projects aims to develop a more powerful three-dimensional Systems-on-a-Chip(SoC) to efficiently address the problem of slow down of transistor technology and explore the method of building a two or even more layer SoC with existing technology.

**Intellectual Merit:** Our proposal is of strong interest to the VLSI and architecture community. Although the idea of extending the direction of a chip from z-axis has been explored a long time ago, it has not been fully utilized and brought into traditional chip design. The first experimental three-dimensional chips was developed by IBM in 2005. The most mature use of three-dimensional circuit is in memory vendors. High Bandwidth Memory(HBM) is a 3D-stacked DRAM technology from Samsung, AMD and Hynix. Hybird Memory Cube(HMC) is another technology brought by Micron. Our proposal is of strong interest to the VLSI and architecture community. However, none of the approach have been used on make a three-dimensional SoCs.

Our proposal will be answering the following questions by establishing both principle and mechanisms.

- Whether it is possible to make a SoC three dimension chip and how should we organize the architecture of the architecture. Since the technology used in memory part and logic part is different, a general idea is separate memory and logic circuits into two parts and build them one on the top of another to build three dimensional chips. The key problem is to put which die on the top and how to manage the logic parts routing.
- How to solve the heating problem. The main concern of putting one die on the top another is heating problem. Usually the cooling system is placed under the die to make sure the temperature of the chip won't go beyond the limitation. However if we put one die on the top of another, cooling may become a problem of the upper one. Our proposal are planning to solve the heating problem of the upper layer.
- How to address the communication problem of logic die and memory die. Since memory part has been moved to the bottom of logic part, the old communication method of using a bus or some Direct Memory Access(DMA) become useless. A new communication method will be proposed to improve both communication latency and bandwidth.
- Is there any way of integrating part of logic circuits and memory circuits into one die? By making two logic IPs one beyond another will open up new design methodology of data flow.

**Broader Impacts:** This interdisciplinary project will enable a very broad impact. First, the developed three-dimensional SoCs will be the first attempt of building vertical SoCs and it will certainly start a new trend of making things multi-dimensional. Secondly, the three-dimensional will open up many chances in the following community: VLSI, computer architecture. Plenty of new topics including new architecture design, new circuit design, new solutions to the thermal problems of the chips will be opened up.

**Keywords:** 3D IC, Systems-on-a-Chip

### **Results from Prior NSF support**

**The PI Gan** has never received any NSF awards.

**Lead PI** Yiming Gan, Ph.D student of Computer and Science Department; **Affiliation:** University of Rochester, Rochester, NY; **E-mail:** ygan10@ur.rochester.edu