Technological advances have resulted in increasing levels of on-chip functionality. Multi-core architectures pervade all levels of computing platforms, from smart phones to servers and high-performance computers. Extraction of parallelism from mainstream applications is thus even more imperative than in the past.

This seminar will examine new developments in the concurrency space - common (and new) programming platforms (languages and runtimes), scalable architectures that support concurrency, support for heterogeneous computing, energy and power-aware concurrency, and performance in the presence heterogeneity and imperfect reliability.

Prerequisites: CSC 2/458, CSC 254, and CSC 256, or equivalent, and/or instructor’s permission. In other words, basic knowledge about parallel and distributed systems will be assumed.

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CSB 717, 275-5647
Office hours by appointment, but don’t be afraid to stop by. If you want to be sure I’m in my office, use e-mail to contact me.

Web site: http://www.cs.rochester.edu/~sandhya/csc572 — I will make all material and links available here.

Class time: To be determined based on class participants’ schedules. First meeting on Wednesday January 18th at 4.50 in CSB 703.

Workload: Class participation and presentation is required. Those officially taking the course will be required to do a term project, along with brief paper summaries.

Initial/tentative list of papers we will discuss in class (and that will be presented by class participants) -

Composability

Thread pools and task parallelism
- “Intel Threading Building Blocks 4.0”, Intel, September 2011.

Heterogeneity
• “Programming Model for a Heterogeneous x86 Platform”, Saha et al., In *Proceedings of the International Conference on Programming Language Design and Implementation (PLDI)*, 2009.


• “Enabling Legacy Applications on Heterogeneous Platforms”, Becchi et al., In *HotPar*, 2010.

• “An OpenCL Framework for Heterogeneous Multicores with Local Memory”, Lee et al., in *Proceedings of the International Conference on Parallel Architectures and Compilation Techniques (PACT)*, September 2010.

### Synchronization


### Parallel Algorithms/Concurrent Data Structures


### Domain-Specific Languages


### Architectural Support


• “An OS-Based Alternative to Full Hardware Coherence on Tiled CMPs”, C. Fensch and M. Cintra, in *HPCA*, 2008.

• “Atomic Coherence: Leveraging Nanophotonics to Build Race-Free Cache Coherence Protocols”, Dana Vantrease (Wisconsin), Mikko H. Lipasti (Wisconsin), and Nathan Binkert (HP), *HPCA*, 2011.

• “HAQu: Hardware Accelerated Queueing For Fine-Grained Threading on a Chip Multiprocessor”, Sanghoon Lee (NCSU), Devesh Tiwari (NCSU), Yan Solihin (NCSU), and James Tuck (NCSU), *HPCA*, 2011.

### Operating Systems Support