

Hemayet Hossain

209 Conant Road Apt. D
Rochester, NY 14623, USA
Cell: 585-269-4847 Work: 585-275-2527
E-mail: hossain@cs.rochester.edu

PhD Candidate
Department of Computer Science
University of Rochester, Rochester, NY 14627, USA
<http://www.cs.rochester.edu/u/hossain>

Current Research

❖ *Chip Multiprocessor, Memory Hierarchies, and Cache Coherence Protocols.*

Working with two professors. We are targeting cache coherence protocol enhancements by applying different optimization techniques such as prediction, migration, and selective replication of data at the L1 cache level. We have proposed a novel cache organization too that provides faster cache coherence and extra effective cache capacity resulting faster program execution, reduced power consumption and reduced bandwidth requirement. Using GEMS and SIMICS as the underlying framework for performance evaluation. Data access patterns (like migratory, producer-consumer, read-read shared, and read-write shared) in real life softwares are detected adaptively and corresponding performance efficient actions are taken for L1-L2 cache transactions. C++ and SLICC are used for coding the new protocol.

We are also working on “Utilizing under-utilized private caches in CMPs” which applies some heuristics to determine under-utilization of certain private caches and used by more cache demanding adjacent cores and “Dynamic L2 bank mapping in CMPs” which keeps the data at a L2 bank which is optimally located with respect to data sharer(s).

❖ *Adaptive Cache Replacement Policy.*

Usually in multi-threaded applications running on a chip multiprocessor system, shared data consume a small percentage of the cache capacity at a shared cache level (may be the last level); whereas shared data serve major portion of the requests. Evicting a shared line will incur higher indirect penalties as that line is going to be used more often. As the traditional cache replacement policies, like true LRU or one-bit LRU, do not distinguish between shared or non-shared cache lines, these policies are vulnerable to the shared line eviction penalties. By providing higher priorities to the shared lines to be alive while finding a victim for eviction in cache replacement policies, the penalties for shared line eviction can be reduced. The ShARP adaptively determines the priority level for the shared lines by tracking past cache access behavior and penalty incurred. In general, we are working on replacement policies for shared caches where cache lines might be shared or not among multiple threads.

Research Area

CMP memory hierarchies, cache coherence protocols, cache replacement policies, network-on-chip, transactional memory (TM), and multi-threaded/multi-programmed workload analysis.

Education

- ❖ *PhD in Computer Science* 2005-present
University of Rochester, Rochester, NY 14623, USA
Expected graduation : Spring 2010
Advisor: Prof. Sandhya Dwarkadas
- ❖ *MS in Computer Science* 2005-2006
University of Rochester, Rochester, NY 14623, USA
Advisor: Prof. Sandhya Dwarkadas
- ❖ *M. Sc. in Computer Science & Engineering* 2002 – 2005
Bangladesh University of Engineering & Technology (BUET)
- ❖ *B. Sc. in Computer Science & Engineering* 1995-2001
Bangladesh University of Engineering & Technology (BUET)

Publications

1. **Hemayet Hossain**, Sandhya Dwarkadas, and Michael C. Huang: Improving Support for Locality and Fine-Grain Sharing in Chip Multiprocessors, in *17th International Conference on Parallel Architectures and Compilation Techniques (PACT)*, October 2008.

2. Arrvindh Shriraman, Michael F. Spear, **Hemayet Hossain**, Virendra J. Marathe, Sandhya Dwarkadas, and Michael L. Scott: An Integrated Hardware-Software Approach to Flexible Transactional Memory, *in 34th International Symposium on Computer Architecture (ISCA)*, June 2007.
3. Michael F. Spear, Arrvindh Shriraman, **Hemayet Hossain**, Sandhya Dwarkadas, and Michael L. Scott: Alert-on-Update: A Communication Aid for Shared Memory Multiprocessors, *poster at Principles and Practice of Parallel Programming (PPoPP)*, March 2007.
4. **Hemayet Hossain**, Mostak Ahmed, Abdullah Al-Nayeem, Tanzima Zerine Islam, and Md. Mostofa Akbar: gpNoCsim – A General Purpose Simulator for Network-on-Chip, *International Conference on Information and Communication Technology (ICICT)*, March 2007.
5. Arrvindh Shriraman, Michael F. Spear, **Hemayet Hossain**, Virendra J. Marathe, Sandhya Dwarkadas, and Michael L. Scott: An Integrated Hardware-Software Approach to Flexible Transactional Memory: *Tech Report: TR910, Computer Science Department, University of Rochester, December 2006.*
<http://www.cs.rochester.edu/trs/systems-trs.html>
6. **Hemayet Hossain**, Md. Mostofa Akbar, and Md. Monirul Islam: Extended-butterfly Fat Tree Interconnection (EFTI) Architecture for Network on Chip: *IEEE Pacrim Conference on Communications, Computers and Signal Processing (PACRIM) University of Victoria, Canada, August 2005.*
7. Md. Monirul Islam, Md. Mostofa Akbar, **Hemayet Hossain**, and Eric G. Manning: Admission Control of Multimedia Sessions to a set of Multimedia Servers connected by an Enterprise Network, *IEEE Pacrim Conference on Communications, Computers and Signal Processing (PACRIM) University of Victoria, Canada, August 2005.*
8. **Hemayet Hossain**: A General purpose Simulator for Network on Chip, *M. Sc. Engineering Thesis, July 2005*
9. **Hemayet Hossain**: Optimal Algorithm for star chromatic number of planar and non-planar graphs, *B. Sc. Engineering Thesis, July 2001*

Work Experiences

- ❖ **Architecture Intern @ NVIDIA Corporation, Santa Clara, CA** May 2008 – Aug 2008
 1. Designing and writing various functional tests for verification of the memory subsystems for the NVIDIA's next generation GPU. Used in-house developed functional model simulator.
 2. Designing and writing various multi-engine tests for verification of multiple engines in the NVIDIA's next generation GPU. Used in-house developed functional model simulator.
 3. Modifying performance model simulator for collecting various memory subsystem performance parameters. And some other works.
- ❖ **Graduate Intern @ VSSAD, Intel Corporation, Hudson, MA** June 2007 – Aug 2007
 1. Porting CMP\$im, a PinTool to model CMP cache configurations, to Windows (Visual Studio 2005); Windows workload characterization by CMP\$im; Further enhancement of CMP\$im including supporting variable number of threads and supporting magic instructions to provide handles during simulation. Also helped in becoming "Pin for Windows" more robust by recovering half a dozen of bugs while collaborating with Pin for Windows team at Intel lab at Israel.
 2. Developed a share-aware adaptive cache replacement policy.
- ❖ **Research Assistant** Sept. 2005 – Dec 2008

With Prof. Sandhya Dwarkadas, Prof. Michael Scott, and Prof. Michael Huang
Design and evaluation of memory hierarchies and interconnects with a particular focus on coherence protocols for chip multiprocessors (CMPs) and transactional memory (TM).
- ❖ **Teaching Assistant** Fall 07(Prof. S. Dwarkadas)
Spring 07(Prof. Kai Shen)

For Operating Systems in two semesters.
Department of Computer Science, University of Rochester
- ❖ **Teaching Assistant** Sept. 2006– Dec. 2006

For Computer Programming taught by Prof. Ted Pawlicki
Department of Computer Science, University of Rochester
- ❖ **Faculty member** May 2002 – Aug 2005

Department of Computer Science and Engineering
Bangladesh University of Engineering & Technology
- ❖ **Software Engineer (part-time)** April 2002 – August 2003

Millennium Information Solutions Ltd. (Best Software House in Bangladesh)
- ❖ **Team leader (6-person team), one of the designers, and main developer of CnS (clearing and settlement) 3-tier**

web application project for all sorts of internal activities and communications among Dhaka Stock Exchange (DSE), DSE brokers, and Central Depository Bangladesh Ltd. (CDBL). Operations includes retrieving raw transactions from TANDEM, invalidation of illegal transactions, perform settlement calculations of money and shares for all the brokers (when and how much to pay or will receive), instruct bank for automated transfer, check printing, lots of online configurable reports, handling expected/unexpected holidays, add/delete/modify settlement rules, add/delete/update company info, instruct CDBL for electronic shares, instruct Security Exchange Commission, imposing circuit breaker, user management, customized menu for different user groups, and so. Tools: Oracle 9i Server/Client, J2EE, Struts, Tomcat, hear-beat server, and Linux Advanced Server. Around 35-40% of the code was developed by me.

- ❖ **Team leader (3-person team) and main developer of fat client program and server program for PicAr** software project. The project was done for the German government and completed jointly by Afinion AG (Germany) and Millennium Information Solutions Ltd. (Bangladesh). PicAr is like windows explorer from GUI point of view but having a lot of other functionalities. It manages different information including many images of various Resorts and Tourist spots of Germany. Information and high quality Images from various client ends can be uploaded to the server and the client is also up-to-dated by getting data from server by sync operations. The project was completed using Microsoft SQL Server and Microsoft Visual Basic. Around 90% of the code was developed by me.
- ❖ **Member of design and development team of the Sunflower** banking software solution. The project was completed for Al-Arafah Islami Bank, Bangladesh and Islami Bank, Bangladesh by Millennium Information Solutions Ltd. The software performs all sorts of bank transactions, day-end, month-end and year-end processes. Around 10% of the code was developed by me. The project was completed using Oracle 8i Server/Client and Microsoft Visual C#.
- ❖ **Designer and developer of School** software project for a famous school “The Message” in Bangladesh for all clerical, accounting, result processing, inventory control, and some other activities of the school. The project was completed using Microsoft SQL Server and Microsoft Visual Basic. I am the one and only member of the project.

Simulation Skills

- ❖ Experienced in **GEMS** and **SIMICS** (full execution-driven computer system simulator). Simulated various commercial and scientific workloads.
- ❖ Experienced in **CMP\$im** - a pin-based CMP cache simulator (also ported **CMP\$im** for Linux into Windows for simulating windows workloads).
- ❖ User level experience with **SimpleScalar**.
- ❖ Designed and developed open-source General Purpose Simulator for Network on Chip (**gpNoCSim**).

Parallel Programming Skill

- ❖ Experienced in pThreads, Solaris threads, MPI and java threads and also on all sorts locks/barriers and atomic operations.

Selected Course Projects

- ❖ **Linux kernel modification:** Adding system calls, synchronization in kernel, threads in user space, CPU scheduling, and memory management. This was done as part of the Operating Systems course at University of Rochester.
- ❖ Design and implementation of a **4-bit microcomputer** using LSI and MSI ICs. We (4-member team) designed and implemented a microcomputer that has variable length instructions and variable length execution cycle. It was capable of performing 27 instructions including recursive function call. This was done as part of the Digital System Design course at Bangladesh University of Engineering and Technology (**BUET**).
- ❖ Implemented of the different layers of **TCP/IP protocol** to communicate among multiple computers connected via serial port. Visual C++ was used for coding. This was done as part of the Computer Networks course at BUET.
- ❖ Design and implementation of **Radio Tuning through Computer LPT1** port programming (Hardware and Software). This was done as part of the Computer Interfacing course at BUET.
- ❖ Complete **Result Processing for BUET** was implemented using SQL SERVER and Visual Basic. This was done as part of Database Course at BUET.

Awards & Honors

- ❖ Champion, Compiler Optimization Contest, CS Department, University of Rochester, 2005.
- ❖ 3 times dean’s award in BUET for academic excellence in B. Sc. Program.
- ❖ Ranked 10th among 48 students in the B. Sc. class who were selected through state-of-the-art rigorous test from the top 4000 students among 0.2 million successful students in HSC of that year.
- ❖ Distinction in HSC and SSC (12th and 10th grade) Certification Exams, 1994 and 1992 respectively.
- ❖ Ranked among top 25 in the ACM University of Valladolid problem solving (till my last submission in 1999).
- ❖ 2nd and 7th positions in national level computer programming contests in 1999 and 2000.

- ❖ Talent pool scholarships in 12th , 10th , 8th , and 5th grade public examinations.
- ❖ Common Wealth graduate scholarship selection from University Grant Commission of Bangladesh.

References

- ❖ Prof. Sandhya Dwarkadas,
Department of Computer Science, University of Rochester, Rochester, NY 14627-0226
email: sandhya@cs.rochester.edu phone: 585-275-5647
- ❖ Prof. Chen Ding
Department of Computer Science, University of Rochester, Rochester, NY 14627-0226
email: cding@cs.rochester.edu phone: 585-275-1373
- ❖ Aamer Jaleel
VSSAD, Intel Massachusetts, Inc.
email: aamer.jaleel@intel.com phone: 240-535-2881