

Research Interests

Computer architecture; high-performance microprocessors and memory systems; emerging memory technologies; architecture-circuit interaction; and energy-efficient computing.

Education

- Ph.D. in Electrical and Computer Engineering**, Cornell University 2008
Dissertation: “Reconfigurable and Self-Optimizing Multicore Architectures.”
(Nominated for the 2008 ACM Doctoral Dissertation Award by Cornell University.)
- M.S. in Electrical and Computer Engineering**, Cornell University 2007
Thesis: “Efficiently Exploring Architectural Design Spaces via Predictive Modeling.”
- B.S. in Electrical and Computer Engineering**, Cornell University 2003

Honors and Awards

- IEEE MICRO Top Picks in Computer Architecture 2017
- HPCA 2016 Distinguished Paper Award 2016
- IEEE Computer Society TCCA Young Computer Architect Award 2014
- IEEE MICRO Top Picks in Computer Architecture 2013
- National Science Foundation CAREER Award 2011
- ASPLOS 2010 Best Paper Award 2010
- IEEE MICRO Top Picks in Computer Architecture 2009
- Communications of the ACM Research Highlight 2009

Work Experience

- Associate Professor of ECE & CS, University of Rochester 6/15 – present
- Assistant Professor of ECE & CS, University of Rochester 9/09 – 6/15
- Researcher, Computer Architecture Group, Microsoft Research 9/07 – 8/09
- Intern, Computer Architecture Group, Microsoft Research 5/07 – 8/07
- Intern, Architecture Research Lab, Intel Corporation 6/05 – 8/05
- Intern, Center for Advanced Scientific Computing, LLNL 5/04 – 8/05
- Undergraduate Intern, TriQuint Semiconductor 6/01 – 01/02

Fully Refereed Archival Publications

B. Feinberg, U. Vengalam, N. Whitehair, S. Wang, and E. Ipek, “Enabling Scientific Computing on Memristive Accelerators”, *International Symposium on Computer Architecture (ISCA)*, 2018.

X. Guo, M. Bojnordi, Q. Guo, and E. Ipek, “Sanitizer: Mitigating the Impact of Expensive ECC Checks on STT-MRAM based Main Memories”, *IEEE Transactions on Computers (IEEE TC)*, 2018.

- B. Feinberg, S. Wang, and E. Ipek, "Making Memristive Neural Network Accelerators Reliable", *International Symposium on High Performance Computer Architecture (HPCA)*, 2018.
- M. Marinella, S. Agarwal, A. Hsia, I. Richter, R. Jacobs-Gedrim, J. Niroula, S. Plimpton, E. Ipek, and C. James, "Multiscale Co-design Analysis of Energy, Latency, Area, and Accuracy of a ReRAM Analog Neural Training Accelerator", *IEEE Journal on Emerging and Selected Topics in Circuits and Systems (IEEE JETCAS)*, 2018.
- E. Ipek, F. Longnos, S. Xiao, and W. Yang, "Vertical Writes: Closing the Throughput Gap Between Scaled STT-MRAM and DRAM", *IEEE Computer Architecture Letters (IEEE CAL)*, 2017.
- M. N. Bojnordi and E. Ipek, "The Memristive Boltzmann Machines", *IEEE Micro Special Issue: Top Picks from 2016 Computer Architecture Conferences (IEEE MICRO)*, 2017.
- E. Ipek, F. Longnos, S. Xiao, and W. Yang, "Bit-Level Load Balancing: A New Technique to Improve the Write Throughput of Deeply Scaled STT-MRAM", *IEEE Computer Architecture Letters (IEEE CAL)*, 2017.
- Y. Bai, V. W. Lee, and E. Ipek, "Voltage Regulator Efficiency Aware DVFS Power Management", *International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS)*, 2017.
- S. Wang and E. Ipek, "Reducing Data Movement Energy via Online Data Clustering and Encoding", *International Symposium on Microarchitecture (MICRO)*, 2016.
- M. N. Bojnordi and E. Ipek, "Memristive Boltzmann Machine: A Hardware Accelerator for Combinatorial Optimization and Deep Learning", *International Symposium on High Performance Computer Architecture (HPCA)*, 2016.
- Y. Song and E. Ipek, "More is Less: Improving the Energy Efficiency of Data Movement via Opportunistic Use of Sparse Codes", *International Symposium on Microarchitecture (MICRO)*, 2015.
- M. Kazemi, E. Ipek, and E. G. Friedman, "Compact Model for Spin-Orbit Magnetic Tunnel Junctions", *IEEE Transactions on Electron Devices (IEEE TED)*, accepted in 2015.
- Y. Bai, Y. Song, M. N. Bojnordi, A. Shapiro, E. Ipek, and E. G. Friedman, "Architecting a MOS Current Mode Logic (MCML) Processor for Fast, Low Noise and Energy-Efficient Computing in the Near-Threshold Regime", *International Conference on Computer Design (ICCD)*, 2015.
- Y. Song, M. N. Bojnordi, and E. Ipek, "Energy-Efficient Data Movement with Sparse Transition Encoding", *International Conference on Computer Design (ICCD)*, 2015.
- Q. Guo, X. Guo, E. Ipek, Y. Bai, R. Patel, and E. G. Friedman, "Resistive TCAM Systems for Data-Intensive Computing", *IEEE Micro Special Issue: Alternative Computing Designs and Technologies (IEEE MICRO)*, 2015.
- M. Kazemi, E. Ipek, and E. G. Friedman, "Energy Efficient Nonvolatile Flip Flop with Subnanosecond Data Backup for Fine Grain Power Gating", *IEEE Transactions on Circuits and Systems – II (IEEE TCAS-II)*, accepted 2015.
- Y. Bai, Y. Song, M. N. Bojnordi, A. Shapiro, E. G. Friedman, and E. Ipek, "Back to the Future: Current Mode Processors in the Era of Deeply Scaled CMOS", *IEEE Transactions on Very Large Scale Integration Systems (IEEE TVLSI)*, accepted 2015.

- S. Wang, Y. Song, M. N. Bojnordi, and E. Ipek, "Enabling Energy Efficient Hybrid Memory Cube Systems with Erasure Codes", *International Symposium on Low Power Electronics and Design (ISLPED)*, 2015.
- R. Patel, X. Guo, Q. Guo, E. Ipek, and E. G. Friedman, "Reducing Switching Latency and Energy in STT-MRAM Caches with Field-Assisted Writing", *IEEE Transactions on Very Large Scale Integration Systems (IEEE TVLSI)*, accepted 2015.
- I. Richter, K. Pas, X. Guo, R. Patel, J. Liu, E. Ipek, and E. G. Friedman, "Memristive Accelerator for Extreme Scale Linear Solvers", *Government Microcircuit Applications & Critical Technology Conference (GOMACTech)*, 2015.
- M. Kazemi, E. Ipek, and E. G. Friedman, "Adaptive Compact Magnetic Tunnel Junction Model", *IEEE Transactions on Electron Devices (IEEE TED)*, Vol. 61, No. 11, pp. 3883-3891, 2014.
- R. Patel, E. Ipek, and E. G. Friedman. "Field Driven STT-MRAM Cell for Reduced Switching Latency and Energy", *IEEE Symposium on Circuits and Systems (ISCAS)*, 2014.
- E. Ipek and E. G. Friedman. "Resistive Memory Based Acceleration of Data Intensive Computing", *Government Microcircuit Applications & Critical Technology Conference (GOMACTech)*, 2014.
- R. Patel, E. Ipek, and E. G. Friedman. "2T-1R STT-MRAM Memory Cells for Enhanced On/Off Current Ratio", *Microelectronics Journal (MEJ)*, 2014.
- M. N. Bojnordi and E. Ipek, "DESC: Energy Efficient Data Exchange using Synchronized Counters", *International Symposium on Microarchitecture (MICRO)*, 2013.
- M. N. Bojnordi and E. Ipek, "A Programmable Memory Controller for the DDRx Interfacing Standards", *ACM Transactions on Computer Systems (ACM TOCS)*, accepted 2013.
- M. N. Bojnordi and E. Ipek, "Programmable DDRx Controllers," *IEEE Micro Special Issue: Top Picks from 2012 Computer Architecture Conferences (IEEE MICRO)*, 2013.
- Q. Guo, X. Guo, R. Patel, E. Ipek, and E. G. Friedman. "AC-DIMM: Associative Computing with STT-MRAM," *International Symposium on Computer Architecture (ISCA)*, 2013.
- R. Patel, E. Ipek, and E. Friedman. "STT-MRAM Memory Cells with Enhanced On/Off Ratio," *International System-on-Chip Conference (SOCC)*, 2012.
- M. N. Bojnordi and E. Ipek. "PARDIS: A Programmable Memory Controller for the DDRx Interfacing Standards," *International Symposium on Computer Architecture (ISCA)*, 2012.
- J. Mukundan, S. Ghose, R. Karmazin, E. Ipek, and J. F. Martinez. "Overcoming Single-Thread Performance Hurdles in the Core Fusion Reconfigurable Multicore Architecture," *International Symposium on Supercomputing (ICS)*, 2012.
- G. Guo, X. Guo, Y. Bai, and E. Ipek. "A Resistive TCAM Accelerator for Data Intensive Computing," *International Symposium on Microarchitecture (MICRO)*, 2011.
- X. Guo, E. Ipek, and T. Soyata. "Resistive Computation: Avoiding the Power Wall with Low-Leakage STT-MRAM Based Computing," *International Symposium on Computer Architecture (ISCA)*, 2010.
- E. Ipek, J. Condit, E. Nightingale, D. Burger, and T. Moscibroda. "Dynamically Replicated Memory: Building Reliable Systems from Nanoscale Resistive Memories," *International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS)*, 2010.

B. Lee, E. Ipek, O. Mutlu, and D. Burger. “Phase Change Memory Architecture and the Quest for Scalability,” *Communications of the ACM (CACM)*, 2010.

B. Lee, P. Zhou, E. Ipek, O. Mutlu, J. Yang, Y. Zhang, B. Zhao, and D. Burger. “Phase Change Technology and the Future of Main Memory,” *IEEE Micro Special Issue: Top Picks from 2009 Computer Architecture Conferences (IEEE MICRO)*, 2010.

J. Condit, E. Nightingale, C. Frost, E. Ipek, D. Burger, B. Lee, and D. Coetzee, “Better I/O Through Byte-Addressable, Persistent Memory,” *Symposium on Operating Systems Principles (SOSP)*, 2009.

J. F. Martínez and E. Ipek, “Dynamic Multicore Resource Management: A Machine Learning Approach,” *IEEE Micro, Vol. 29, No. 5 (IEEE MICRO)*, 2009.

B. Lee, E. Ipek, O. Mutlu, and D. Burger, “Architecting Phase-Change Memory as a Scalable DRAM Alternative,” *International Symposium on Computer Architecture (ISCA)*, 2009.

R. Bitirgen, E. Ipek, and J.F. Martínez, “Coordinated Management of Multiple Interacting Resources in Chip Multiprocessors: A Machine Learning Approach,” *International Symposium on Microarchitecture (MICRO)*, 2008.

E. Ipek, O. Mutlu, J.F. Martínez, and R. Caruana, “Self-Optimizing Memory Controllers: A Reinforcement Learning Approach,” *International Symposium on Computer Architecture (ISCA)*, 2008.

E. Ipek, S. A. McKee, K. Singh, R. Caruana, B. R. de Supinski, and M. Schulz, “Efficient Architectural Design Space Exploration via Predictive Modeling,” *ACM Transactions on Architecture and Code Optimization (TACO)*, 2008.

C. LaFrieda, E. Ipek, J.F. Martínez, and R. Manohar, “Utilizing Dynamically Coupled Cores to Form a Resilient Chip Multiprocessor,” *International Symposium on Dependable Systems and Networks (DSN)*, 2007.

E. Ipek, M. Kirman, N. Kirman, and J.F. Martínez, “Core Fusion: Accommodating Software Diversity in Chip Multiprocessors,” *International Symposium on Computer Architecture (ISCA)*, 2007.

E. Ipek, S. A. McKee, B. R. de Supinski, M. Schulz, and R. Caruana, “Efficiently Exploring Architectural Design Spaces via Predictive Modeling,” *International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS)*, 2006.

E. Ipek, J.F. Martínez, B. R. de Supinski, S. A. McKee, and M. Schulz, “Dynamic Program Phase Detection in Distributed Shared-Memory Multiprocessors,” *International Parallel and Distributed Processing Symposium (IPDPS)*, 2006.

E. Ipek, B. R. de Supinski, M. Schulz, and S. A. McKee, “An Approach to Performance Prediction for Parallel Applications,” *European Conference on Parallel Computing (EURO-PAR)*, 2005.

Book Chapters

G. Guo, X. Guo, Y. Bai, and **E. Ipek**. “Resistive Memories in Associative Computing,” *Emerging Memory Technologies: Design, Architecture, and Applications*, Y. Xie (Editor), Springer, July 2013.

Patents

E. Friedman, I. Richter, X. Guo, M. Kazemi, K. Pas, R. Patel, **E. Ipek**, and J. Liu. “Resistive Memory Accelerator,” US patent 9,847,125, February 9, 2017.

J. P. Condit, E. B. Nightingale, B. Lee, **E. Ipek**, C. Frost, and D. C. Burger. “Hardware and Operating System Support for Persistent Memory on a Memory Bus,” US patent 8,984,239, January 2, 2014.

M. N. Bojnordi, **E. Ipek**, and Arun Jagatheesan. “Programmable Memory Controller,” US patent 9,256,369, October 24, 2013.

E. Ipek, T. Moscibroda, D. C. Burger, E. B. Nightingale, and J. P. Condit. “Efficiency of Hardware Memory Access using Dynamically Replicated Memory,” US patent 8,543,863, September 24, 2013.

E. Ipek, J. P. Condit, E. B. Nightingale, D. C. Burger, and T. Moscibroda. “Dynamically Replicated Memory,” US patent 8,255,742, May 19, 2011.

J. P. Condit, E. B. Nightingale, B. Lee, **E. Ipek**, C. Frost, and D. C. Burger. “Hardware and Operating System Support for Persistent Memory on a Memory Bus,” US patent 8,533,404, April 29, 2010.

J. P. Condit, **E. Ipek**, E. B. Nightingale, B. Lee, C. Frost, and D. Burger. “Hardware and Operating System Support for Persistent Memory on a Memory Bus,” US patent 8,219,741, April 29, 2010.

J.F. Martínez, **E. Ipek**, M. Kirman, and N. Kirman. “Systems and Methods for Reconfiguring On-Chip Multiprocessors,” US patent 7,809,926, May 8, 2008.

A. Nguyen, **E. Ipek**, V. Lee, D. Kim, and M. Smelyanskiy, “Virtual Vector Processing,” US patent 9,870,267, September 27, 2007.

Grants

- Intelligence Advanced Research Projects Activity award, “Spin Transfer, Energy-Efficient 64-bit Memory (STEM64).” \$50,000 to **PI E. Ipek** and Co-PI E. G. Friedman. 2017-2018
- Sandia National Laboratories Grant, “Energy Efficient Neural Network Training with Memristors.” \$28,000 to **PI E. Ipek**. 2017
- Intelligence Advanced Research Projects Activity award, “EDA Development for Cryogenic Memory.” \$190,000 to **Co-PIs E. Ipek** and E. G. Friedman. 2017-2018
- National Science Foundation XPS award, “A Memristive Hardware Platform for Large Scale Combinatorial Optimization.” \$298,283 to **PI E. Ipek**. 2016 - 2018
- National Science Foundation CNS EAGER award, “Memristive Accelerator for Extreme Scale Linear Solvers.” \$125,000 to **PI E. Ipek**; Co-PIs E. Friedman, J. Liu, and J. Dongarra. 2015 - 2016
- Intelligence Advanced Research Projects Activity award, “Spin Transfer, Energy-Efficient 64-bit Memory (STEM64).” \$845,000 to **PI E. Ipek** and Co-PI E. G. Friedman. 2014 - 2017
- National Science Foundation SHF award, “Application-Specific Memory System Optimizations using Programmable Memory Controllers.” \$300,000 to **PI E. Ipek**. 2012 - 2015
- Samsung grant, “Programmable Memory Controllers.” \$51,300 to **PI E. Ipek**. 2012
- National Science Foundation CAREER award, “Overcoming the Many-Core Power Wall with Resistive Computation.” \$489,053 to **PI E. Ipek**. 2011 - 2016

- Samsung grant, “Flexible Memory Systems.” \$47,321 to **PI E. Ipek.** 2011
- Qualcomm grant, “STT-MRAM based Resistive Computing Microarchitecture for Mobile Applications.” \$75,000 to **PI E. Ipek.** 2010

Teaching

- ECE 402: Computer Architecture
- CSC 573: Memory Systems
- CSC 293: Analytical and Stochastic Modeling of Computer Systems
- CSC 252: Computer Organization

Current Ph.D. Students

- Benjamin Feinberg (ECE)
- Darya Mikhailenko (ECE)

Ph.D. Graduates

- Xiaochen Guo, Ph.D.’15 (ECE)
First Job: Assistant Professor of ECE, Lehigh University
IBM Ph.D. Fellow, 2012-2013, 2014-2015
- Qing Guo, Ph.D.’15 (CS)
First Job: Senior Architect, NVidia
- Yanwei Song, Ph.D.’16 (ECE)
First Job: Software Developer, Tower Research Capital
- Yuxin Bai, Ph.D.’16 (ECE)
First Job: Power and Performance Software Engineer, Apple
- Mahdi Nazm Bojnordi, Ph.D.’16 (ECE)
First Job: Assistant Professor of CS, University of Utah
- Shibo Wang, Ph.D.’17 (CS)
First Job: Software Engineer, Google

M.S. Graduates

- Sean Wang, ECE, M.S. 2017
- Chinmai Panibathe, ECE, M.S. 2017
- Dan Snyder, ECE, M.S. 2011
- Peter McLoone, ECE, M.S. 2011
- Guanghui Zhou, ECE, M.S. 2011
- Zihe Liu, ECE, M.S. 2011

Past MSR Interns

- Biplab Deka (IIT Kanpur), Summer 2009
- Janani Mukundan (Cornell), Spring 2009
- Ramazan Bitirgen (Cornell), Spring 2008

Professional Activities

- **IEEE Computer Society Technical Committee on Computer Architecture (TCCA):** Member of the executive committee (2015-2017), communications chair (2010-2017)
- **Conference Program Committee:** MICRO'18, Top Picks'18, HPCA'18, MICRO'17, DAC'17, HPCA'17, ICS'16, DAC'16, ISCA'16, HPCA'16, ISCA'15, DAC'15, HPCA'15, CF'14, MICRO'13, ICCD'13, MICRO'12, IISWC'12, ICCD'12, ISPASS'12, IPDPS'12, IPDPS'11, ICCD'11, ICCD'10, MICRO'09, ICCD'09
- **Conference Organizing Committee:** HPCA'12, ISCA'11, HPCA'11, IISWC'11, IISWC'10, IISWC'08
- **Workshop Program Committee:** MSPC'14, HotPower'13, MSC'12, DCA'11, SMART'11, SMART'10
- **Workshop Co-organizer:** EAMA'10, NDCA'09, EAMA'09
- **Panels:** National Science Foundation, Department of Energy, Microsoft Research Fellowship

Service

- Participant at the “IARPA Cryogenic Computing Complexity” workshop, sponsored by the Intelligence Advanced Research Projects Activity (IARPA), 03/12/2013.
- Participant at the “Energy-Efficient Cryogenic Memory” workshop (**invitation only**), sponsored by the National Security Agency, 7/19/2011.
- Participant at the “Cross-layer Power Optimization and Management” workshop (**invitation only**), sponsored by the National Science Foundation, 2/11/2012.
- Participant at the workshop on “a Community Supported Computer Architecture Design and Evaluation” (**invitation only**), sponsored by the National Science Foundation, 5/31/2012.

Presentations

“Memristive Accelerators for Data Intensive Computing: From Machine Learning to High Performance Linear Algebra”

- USC Computer Engineering Seminar, University of Southern California, Invited talk, 11/30/2017.
- 5th Berkeley Symposium on Energy Efficient Electronics and Steep Transistor Workshop, Invited talk, 10/19/2017.
- IEEE IRDS Beyond Moore Workshop, Sandia National Laboratory, Invited Talk. 07/06/2017.
- Seiden Frontiers in Engineering and Science Workshop. Technion, Israel Institute of Technology. Invited Talk, 06/05/2017.

“Content Aware Memory Systems for High-Performance, Energy Efficient Data Movement”

- IBM Architecture Seminar. Invited talk. 6/13/2017.

“Accelerator Design with Emerging Memory Technologies”

- AMD, 11/14/2016.
- In-Memory and In-Storage Computing with Emerging Technologies Workshop (co-located with PACT 2016), Keynote Talk, 09/11/2016.

“Computer Architecture Design Utilizing Novel Memories”

- University of Wisconsin, Architecture Seminar, 04/08/2014.
- ISQED (invited tutorial), 03/04/2013.

“Associative Computing with Emerging Nonvolatile Memories”

- University of Rochester, Laboratory for Laser Energetics, 11/30/2012.
- IBM, 10/25/2012.
- Qualcomm, 7/21/2011.

“Resistive Memories and the Future of Memory Systems Architecture”

- Qualcomm, 10/15/2010.
- University of Rochester, ECE Colloquium, 9/29/2010.

“Dynamically Replicated Memory”

- 1st UCSD Nonvolatile Memories Workshop, 4/13/2010
- 15th Intl. Conf. on Architectural Support for Programming Languages and Operating Systems, 3/15/2010

“Reconfigurable and Self-Optimizing Multicore Architectures” (February – April 2009)

- Northwestern University
- University of California, Santa Barbara
- Massachusetts Institute of Technology
- University of Texas at Austin
- Georgia Institute of Technology
- Purdue University
- University of Rochester
- NC State University
- Rutgers State University of New Jersey

“Coordinated Management of Multiple Interacting Resources in CMPs: A Machine Learning Approach”

- 41st International Symposium on Microarchitecture (MICRO), 11/11/2008.

“Self-Optimizing Memory Controllers: A Reinforcement Learning Approach”

- Princeton University, Computer Engineering Seminar, 10/16/2008.
- Georgia Institute of Technology, Architecture Seminar, 10/10/2008.
- 35th International Symposium on Computer Architecture (ISCA), 06.23.2008.
- 4th Annual IBM P=ac2 Conference, 04/01/2008.
- University of Illinois, Urbana-Champaign, Architecture Seminar, 03/07/2008.

“Core Fusion: Accommodating Software Diversity in Chip Multiprocessors”

- 34th International Symposium on Computer Architecture (ISCA), 06/23/2007.

“Efficiently Exploring Architectural Design Spaces via Predictive Modeling”

- 12th Intl. Conf. on Architectural Support for Programming Languages and Operating Systems, 10/23/2006.
- Intel Innovative Platform Architecture Group, Architecture Research Lab, 06/01/2005.