

Research Interests

Computer architecture, novel memory technologies, high-performance memory systems, architecture-circuit interaction, and energy-efficient computing.

Education

- Ph.D. in Electrical and Computer Engineering**, Cornell University 2008
Adviser: Professor José F. Martínez.
Dissertation: “Reconfigurable and Self-Optimizing Multicore Architectures.”
(Nominated for the 2008 ACM Doctoral Dissertation Award by Cornell University.)
- M.S. in Electrical and Computer Engineering**, Cornell University 2007
Thesis: “Efficiently Exploring Architectural Design Spaces via Predictive Modeling.”
- B.S. in Electrical and Computer Engineering**, Cornell University 2003

Awards

- National Science Foundation CAREER Award 2011
- ASPLOS 2010 Best Paper Award 2010
- IEEE Micro Top Picks in Computer Architecture 2009
- Communications of the ACM Research Highlight 2009

Work Experience

- Assistant Professor of ECE & CS, University of Rochester 9/09 - present
- Researcher, Computer Architecture Group, Microsoft Research 9/07 – 8/09
- Intern, Computer Architecture Group, Microsoft Research 5/07 – 8/07
- Intern, Architecture Research Lab, Intel Corporation 6/05 – 8/05
- Intern, Center for Advanced Scientific Computing, LLNL 5/04 – 8/05
- Undergraduate Intern, TriQuint Semiconductor 6/01 – 01/02

Fully Refereed Archival Publications

M. N. Bojnordi and **E. Ipek**. “PARDIS: A Programmable Memory Controller for the DDRx Interfacing Standards,” *International Symposium on Computer Architecture (ISCA)*, Portland, OR, June 2012.

J. Mukundan, S. Ghose, R. Karmazin, **E. Ipek**, and J. F. Martinez. “Overcoming Single-Thread Performance Hurdles in the Core Fusion Reconfigurable Multicore Architecture,” *International Symposium on Supercomputing (ICS)*, Venice, Italy, June 2012.

G. Guo, X. Guo, Y. Bai, and **E. Ipek**. “A Resistive TCAM Accelerator for Data Intensive Computing,” *International Symposium on Microarchitecture (MICRO)*, Porto Alegre, Brazil, November 2011.

X. Guo, **E. Ipek**, and T. Soyata. “Resistive Computation: Avoiding the Power Wall with Low-Leakage LUT-Based Computing,” *International Symposium on Computer Architecture (ISCA)*, Saint-Malo, France, June 2010.

- E. Ipek**, J. Condit, E. Nightingale, D. Burger, and T. Moscibroda. “Dynamically Replicated Memory: Building Reliable Systems from Nanoscale Resistive Memories,” *International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS)*, Pittsburgh, PA, March 2010.
- B. Lee, **E. Ipek**, O. Mutlu, and D. Burger, “Phase Change Memory Architecture and the Quest for Scalability,” *Communications of the ACM (CACM)*, July 2010.
- B. Lee, P. Zhou, **E. Ipek**, O. Mutlu, J. Yang, Y. Zhang, B. Zhao, and D. Burger, “Phase Change Technology and the Future of Main Memory,” *IEEE Micro Special Issue: Top Picks from 2009 Computer Architecture Conferences (IEEE MICRO)*, January 2010.
- J. Condit, E. Nightingale, C. Frost, **E. Ipek**, D. Burger, B. Lee, and D. Coetzee, “Better I/O Through Byte-Addressable, Persistent Memory,” *Symposium on Operating Systems Principles (SOSP)*, Big Sky, MT, October 2009.
- J. F. Martínez and E. Ipek, “Dynamic Multicore Resource Management: A Machine Learning Approach,” *IEEE Micro, Vol. 29, No. 5 (IEEE MICRO)*, September 2009.
- B. Lee, **E. Ipek**, O. Mutlu, and D. Burger, “Architecting Phase-Change Memory as a Scalable DRAM Alternative,” *International Symposium on Computer Architecture (ISCA)*, Austin, TX, June 2009.
- R. Bitirgen, **E. Ipek**, and J.F. Martínez, “Coordinated Management of Multiple Interacting Resources in Chip Multiprocessors: A Machine Learning Approach,” *International Symposium on Microarchitecture (MICRO)*, Lake Como, Italy, November 2008.
- E. Ipek**, O. Mutlu, J.F. Martínez, and R. Caruana, “Self-Optimizing Memory Controllers: A Reinforcement Learning Approach,” *International Symposium on Computer Architecture (ISCA)*, Beijing, China, June 2008.
- E. Ipek**, S. A. McKee, K. Singh, R. Caruana, B. R. de Supinski, and M. Schulz, “Efficient Architectural Design Space Exploration via Predictive Modeling,” *ACM Transactions on Architecture and Code Optimization (TACO)*, January 2008.
- C. LaFrieda, **E. Ipek**, J.F. Martínez, and R. Manohar, “Utilizing Dynamically Coupled Cores to Form a Resilient Chip Multiprocessor,” *International Symposium on Dependable Systems and Networks (DSN)*, Edinburgh, Scotland, June 2007.
- E. Ipek**, M. Kirman, N. Kirman, and J.F. Martínez, “Core Fusion: Accommodating Software Diversity in Chip Multiprocessors,” *International Symposium on Computer Architecture (ISCA)*, San Diego, CA, June 2007.
- E. Ipek**, S. A. McKee, B. R. de Supinski, M. Schulz, and R. Caruana, “Efficiently Exploring Architectural Design Spaces via Predictive Modeling,” *International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS)*, San Jose, CA, October 2006.
- E. Ipek**, B. R. de Supinski, M. Schulz, and S. A. McKee, “An Approach to Performance Prediction for Parallel Applications,” *European Conference on Parallel Computing (EURO-PAR)*, Lisbon, Portugal, August 2005.

Patents

E. Ipek, J. Condit, E. Nightingale, D. Burger, and T. Moscibroda, “Dynamically Replicated Memory,” US patent application filed September 2009.

J. Condit, E. Nightingale, B. Lee, **E. Ipek**, C. Frost, and D. Burger, “Hardware and Operating System Support for Persistent Memory on a Memory Bus,” US patent application filed June 2009.

J.F. Martínez, **E. Ipek**, M. Kirman, and N. Kirman, “Systems and Methods for Reconfigurably Multiprocessing,” US patent number 2010/7,809,926-B2.

Nguyen, **E. Ipek**, V. Lee, and D. Kim, “Virtual Vector Processing,” US Patent Number 2007/0226735.

Teaching

- ECE 402: Computer Architecture Fall 2011
- CSC 573: Memory Systems (*Instructor = 4.5/5, Course = 4/5*) Spring 2011
- ECE 402: Computer Architecture (*Instructor = 5/5, Course = 4.7/5*) Fall 2010
- CSC 573: Memory Systems (*Instructor = 4.42/5, Course = 4.67/5*) Fall 2009

Grants

- National Science Foundation CAREER award, “Overcoming the Many-Core Power Wall with Resistive Computation.” \$489,053. Principal investigator. 2011 - 2016
- Samsung grant, “Flexible Memory Systems.” \$47,321. Principle investigator. 2011
- Qualcomm grant, “STT-MRAM based Resistive Computing Microarchitecture for Mobile Applications.” \$75,000. Principle investigator. 2010

Professional Activities

- **Conference program committee:** MICRO'12, IISWC'12, ICCD'12, ISPASS'12, IPDPS'12, IPDPS'11, ICCD'11, ICCD'10, MICRO'09, ICCD'09
- **Conference organizing committee:** HPCA'12, ISCA'11, HPCA'11, IISWC'11, IISWC'10, IISWC'08
- **Workshop program committee:** NDCA'11, SMART'11, SMART'10
- **Workshop co-organizer:** EAMA'10, NDCA'09, EAMA'09
- **Panels:** National Science Foundation, Department of Energy, Microsoft Research Fellowship

Advising

Ph.D. Students

- Doris Xiaochen Guo, 3rd-year, ECE
- Mahdi Bojnordi, 2nd-year, ECE
- Qing Guo, 2nd-year, CS
- Yuxin Bai, 2nd-year, ECE
- Yanwei Song, 3rd-year, ECE
- Shibo Wang, 1st-year, CS

M.S. Students

- Dan Snyder, ECE, M.S. 2011
- Peter McLoone, ECE, M.S. 2011
- Guanghui Zhou, ECE, M.S. 2011
- Zihe Liu, ECE, M.S. 2011

Microsoft Research Interns

- Biplab Deka (IIT Kanpur), Summer 2009
- Janani Mukundan (Cornell), Spring 2009
- Ramazan Bitirgen (Cornell), Spring 2008

Service

Government

- Participant at the “Energy-Efficient Cryogenic Memory” workshop (invitation only), sponsored by the National Security Agency, 7/19/2011.

University of Rochester

- ECE graduate admissions committee, Fall’09 – present.
- ECE seminar committee, Fall’10 – present.
- ECE strategic planning committee, Summer’11.
- CS web and lab committee, 2009 – 2010.
- CS graduate admissions committee, 2010 – 2011.

Presentations

“Associative Computing with Emerging Nonvolatile Memories”

- Qualcomm, 7/21/2011.

“Resistive Memories and the Future of Memory Systems Architecture”

- University of Rochester, ECE Colloquium, 9/29/2010.
- Qualcomm, 10/15/2010.

“Dynamically Replicated Memory”

- 15th Intl. Conf. on Architectural Support for Prog. Languages and Operating Systems, 3/15/2010
- 1st UCSD Nonvolatile Memories Workshop, 4/13/2010

“Reconfigurable and Self-Optimizing Multicore Architectures” (February – April 2009)

- Northwestern University
- University of California, Santa Barbara
- Massachusetts Institute of Technology
- University of Texas at Austin
- Georgia Institute of Technology
- Purdue University

- University of Rochester
- NC State University
- Rutgers State University of New Jersey

“Coordinated Management of Multiple Interacting Resources in CMPs: A Machine Learning Approach”

- 41st International Symposium on Microarchitecture (MICRO), 11/11/2008.

“Self-Optimizing Memory Controllers: A Reinforcement Learning Approach”

- Princeton University, Computer Engineering Seminar, 10/16/2008.
- Georgia Institute of Technology, Architecture Seminar, 10/10/2008.
- 35th International Symposium on Computer Architecture (ISCA), 06.23.2008.
- 4th Annual IBM P=ac2 Conference, 04/01/2008.
- University of Illinois, Urbana-Champaign, Architecture Seminar, 03/07/2008.

“Core Fusion: Accommodating Software Diversity in Chip Multiprocessors”

- 34th International Symposium on Computer Architecture (ISCA), 06/23/2007.

“Efficiently Exploring Architectural Design Spaces via Predictive Modeling”

- 12th Intl. Conf. on Architectural Support for Prog. Languages and Operating Systems, 10/23/2006.
- Intel Innovative Platform Architecture Group, Architecture Research Lab, 06/01/2005.

Professional Societies

- Member, IEEE
- Member, ACM