CSC 252/452: Computer Organization
Fall 2025: Lecture 11

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University of Rochester

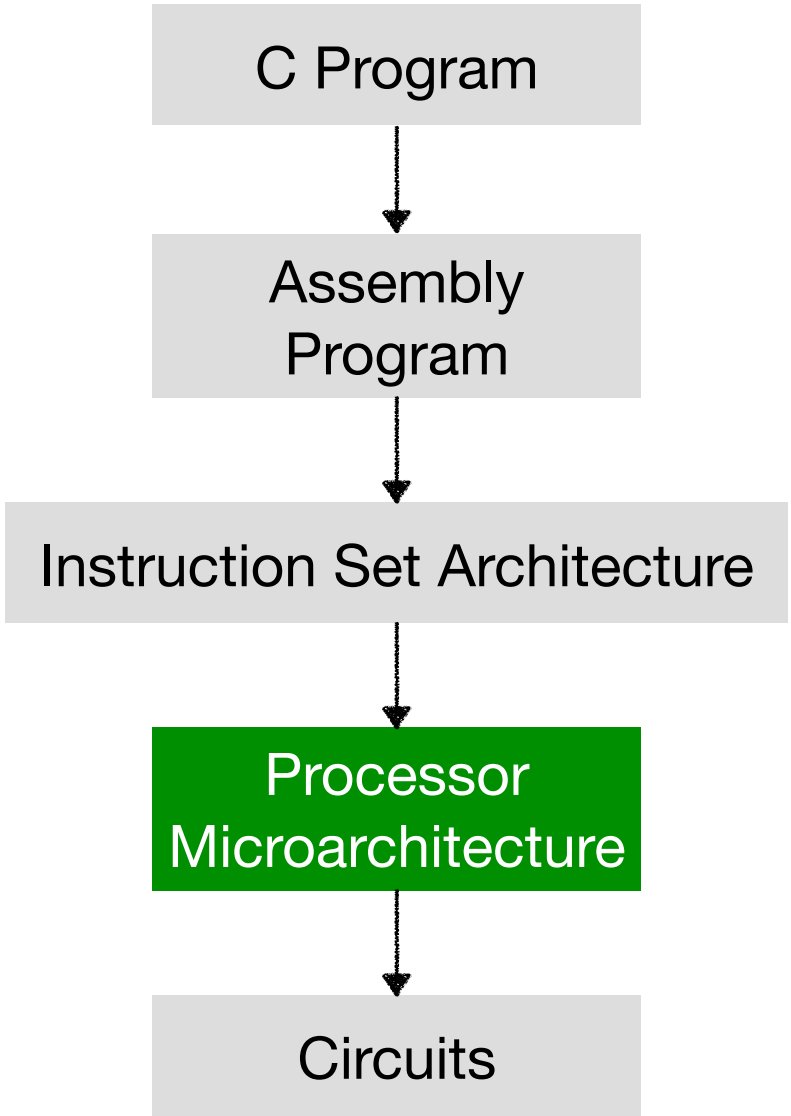
Announcement

- Programming assignment 3 will be out
  - Details: https://www.cs.rochester.edu/courses/252/fall2025/labs/assignment3.html
  - Due on **Oct. 25th**, 11:59 PM
  - You (may still) have 3 slip days

Announcement

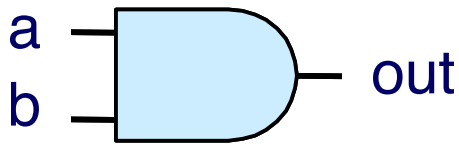
- Programming assignment 3 is in x86 assembly language. Seek help from TAs.
- TAs are best positioned to answer your questions about programming assignments!!!
- Programming assignments do NOT repeat the lecture materials. They ask you to synthesize what you have learned from the lectures and work out something new.

So far in 252…


C Program
Assembly Program
Instruction Set Architecture
Processor Microarchitecture
Circuits

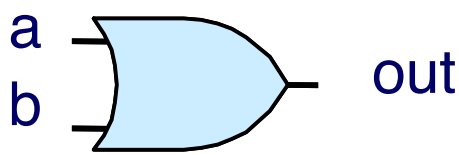
Computing with Logic Gates

And



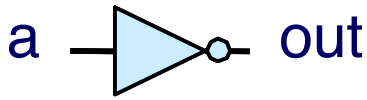
out = a && b

Or



out = a || b

Not

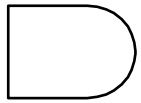


out = !a

Bit Equality

Combinational Circuit: Circuit for computation

Bit Equality



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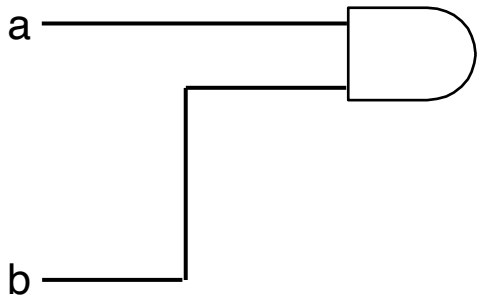

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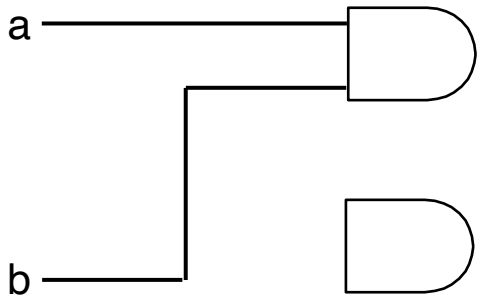

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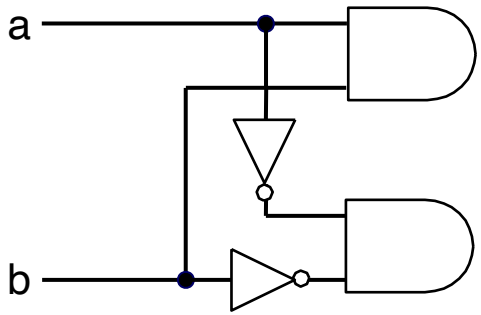

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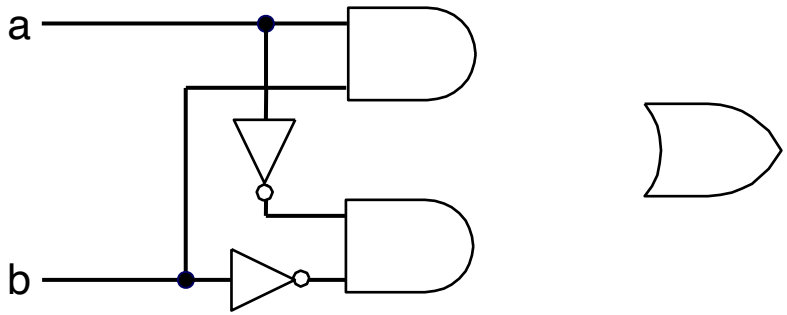

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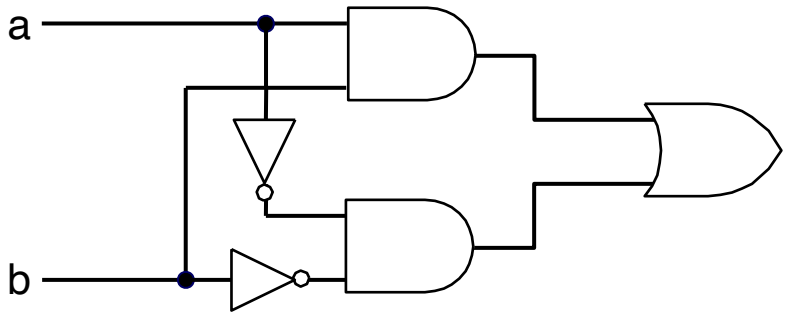

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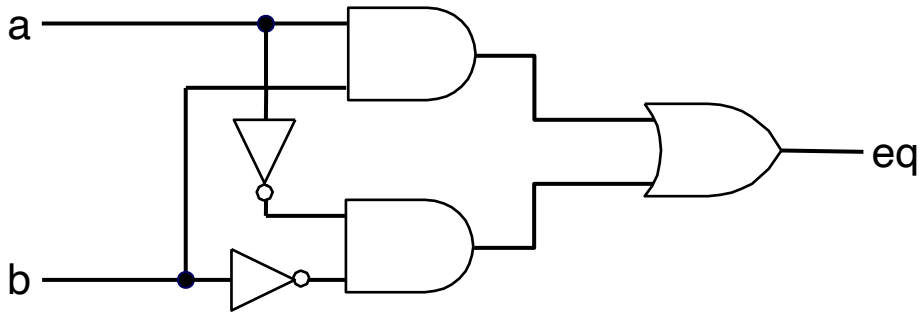

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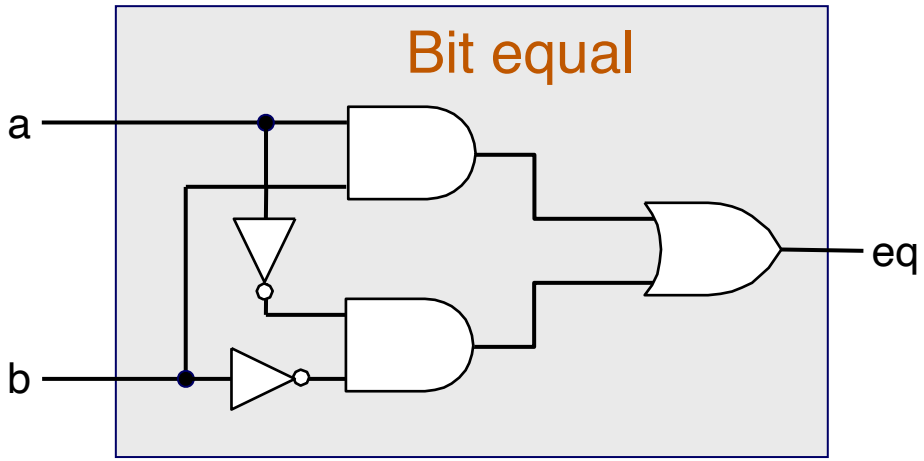

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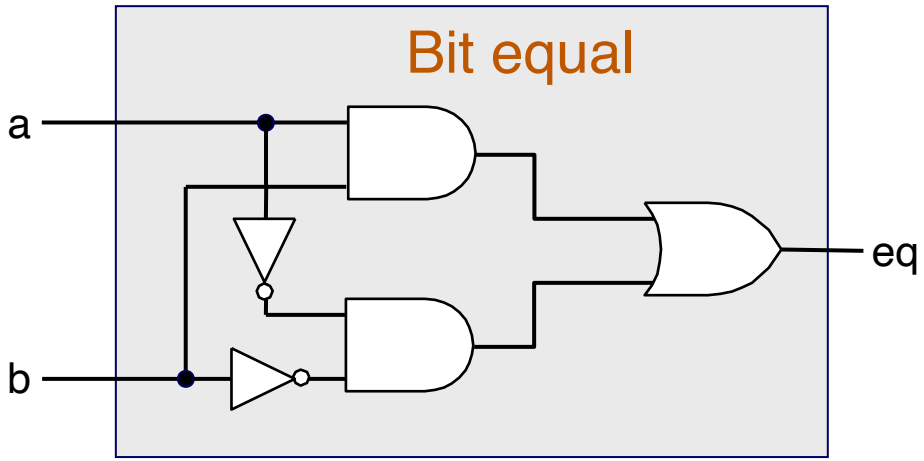
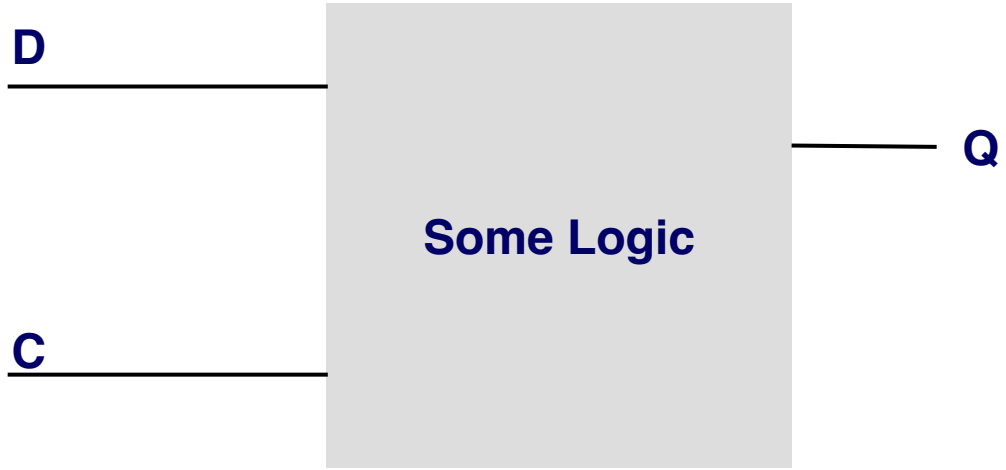


Combinational Circuit: Circuit for computation

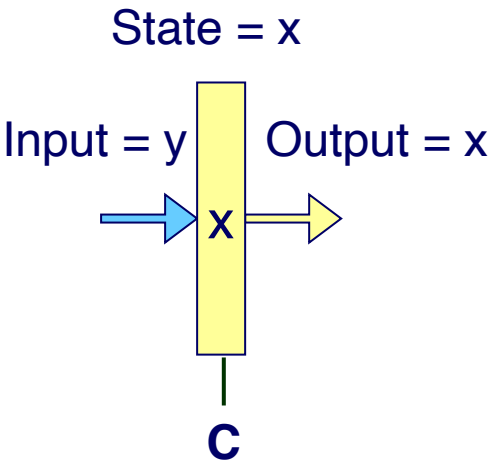
Sequential Circuit: Circuit for storage

Sequential Circuit



- 1-bit storage:
  - D is the data I want to store (0 or 1)
  - C is the control signal
    - When C is 1, Q becomes D (i.e., storing the data)
    - When C is 0, Q doesn't change with D (data stored)

Register Operation



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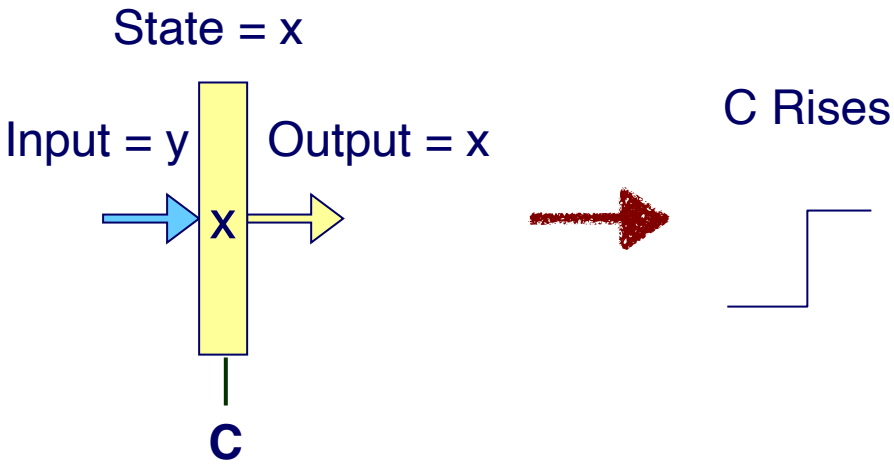

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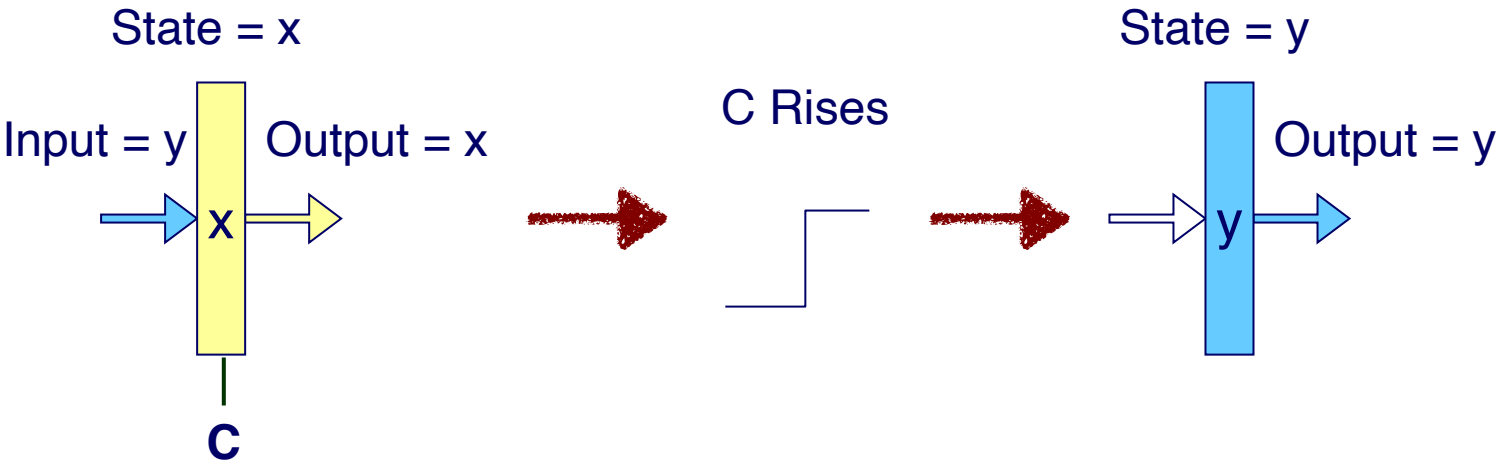

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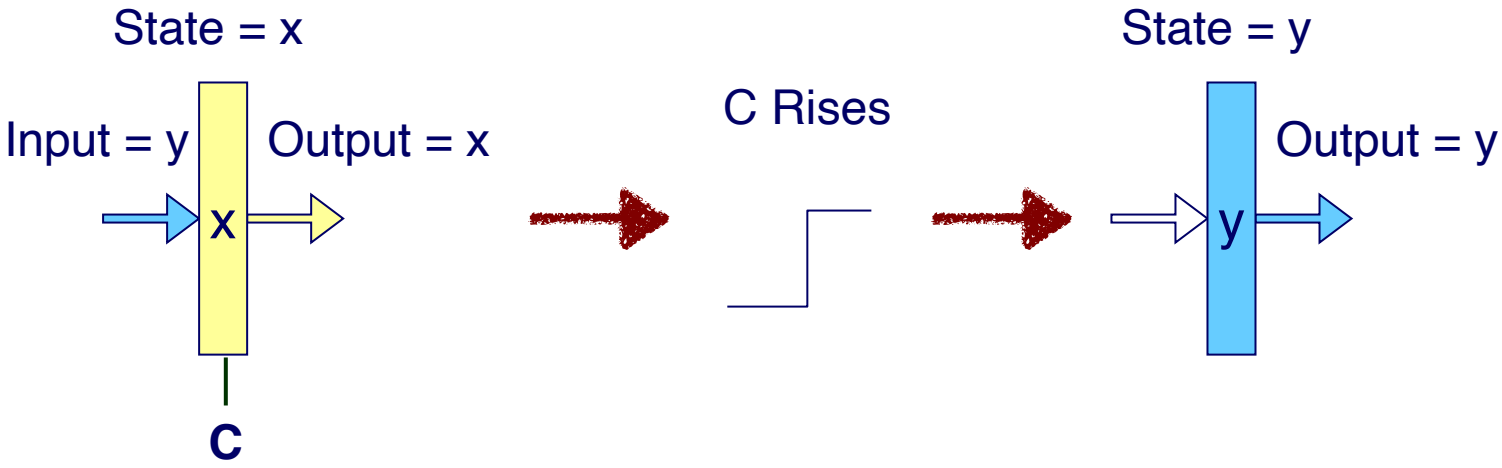

- Stores data bits
- For most of time acts as barrier between input and output
- As C rises, loads input

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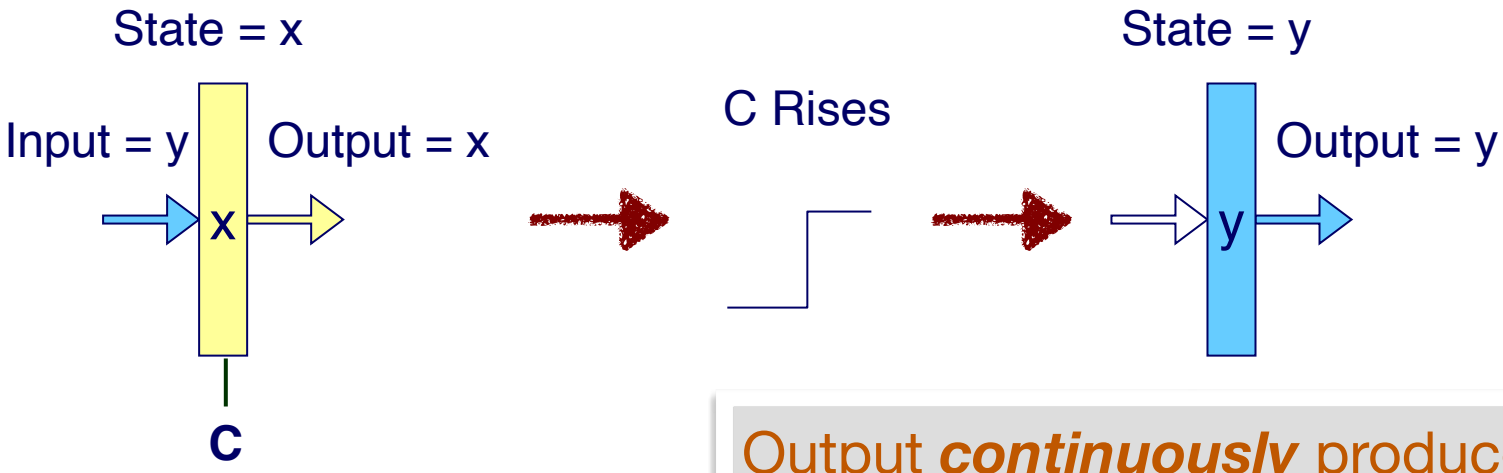

Output ***continuously*** produces y after the rising edge unless you cut off power.

- Stores data bits
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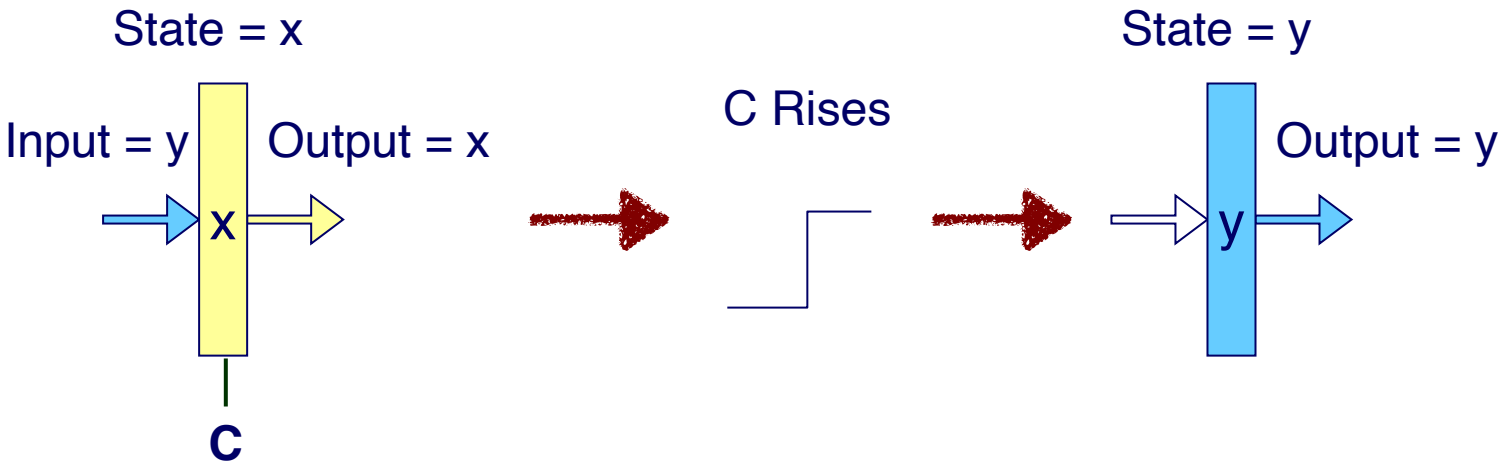
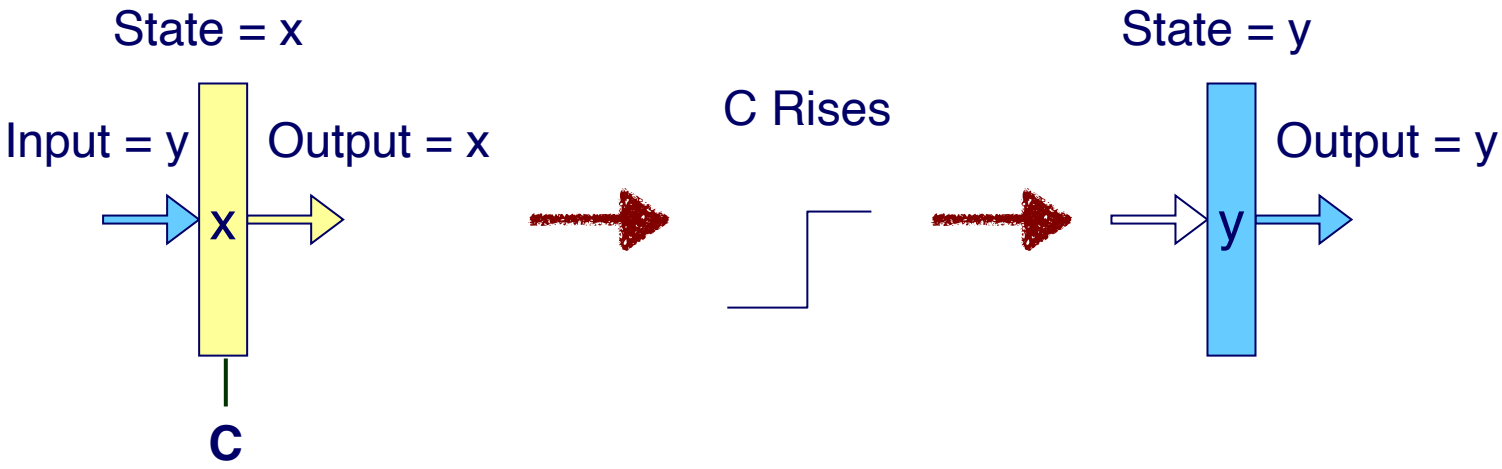
Clock Signal



- A special C: periodically oscillating between 0 and 1
- That's called the **clock** signal. Generated by a crystal oscillator inside your computer.

Clock Signal



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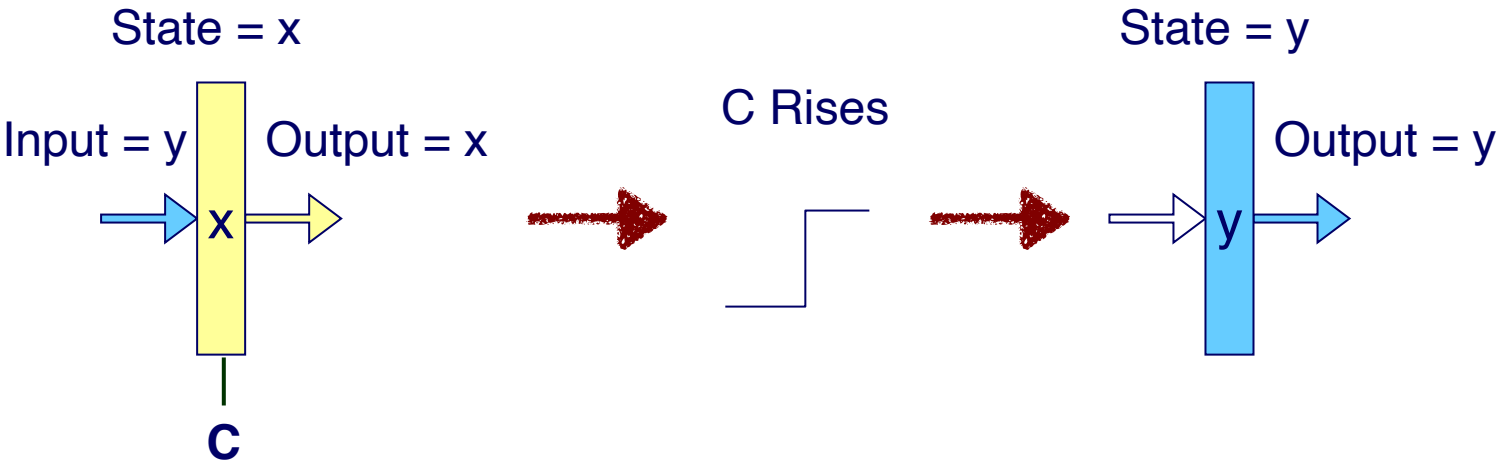

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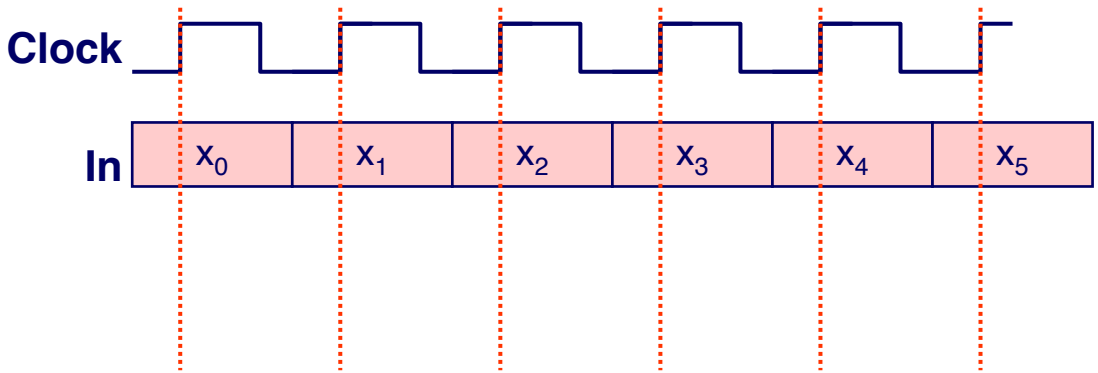

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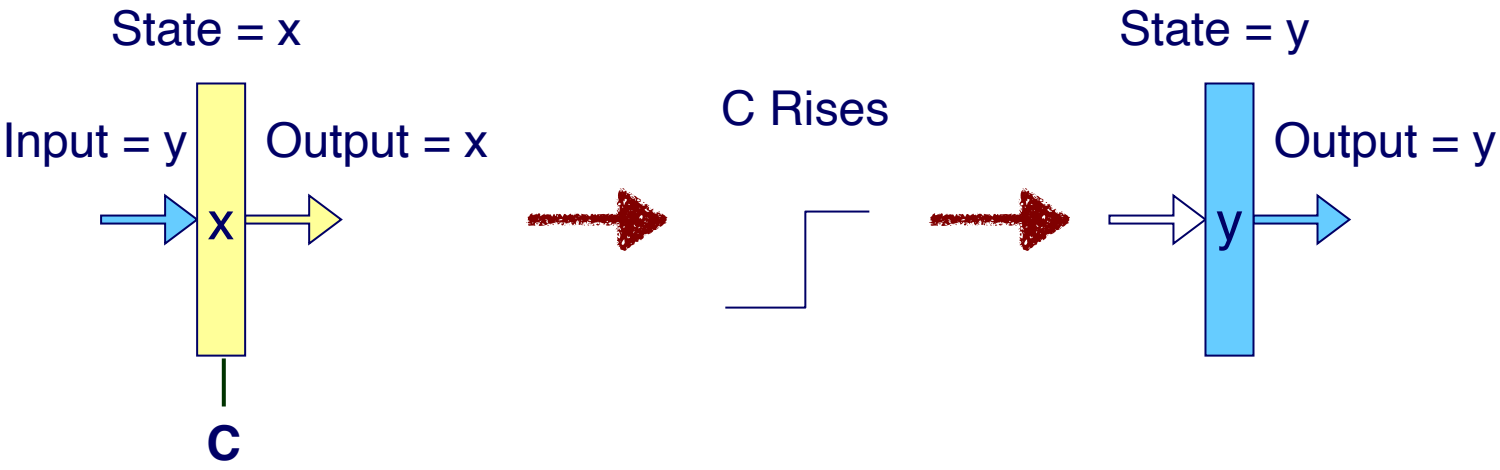

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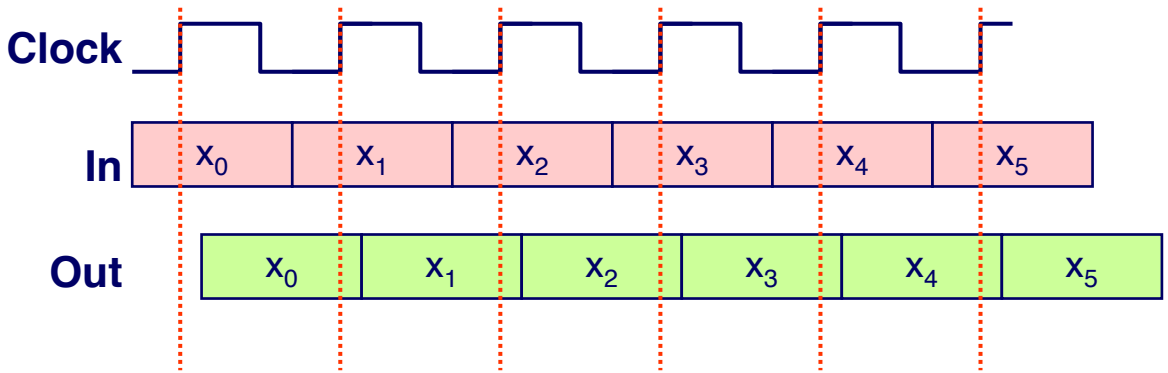

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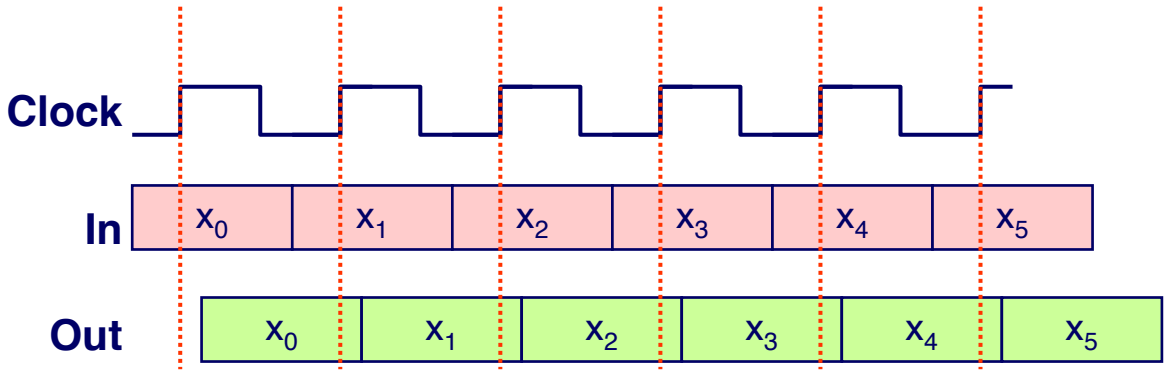
- Cycle time of a clock signal: the time duration between two rising edges.



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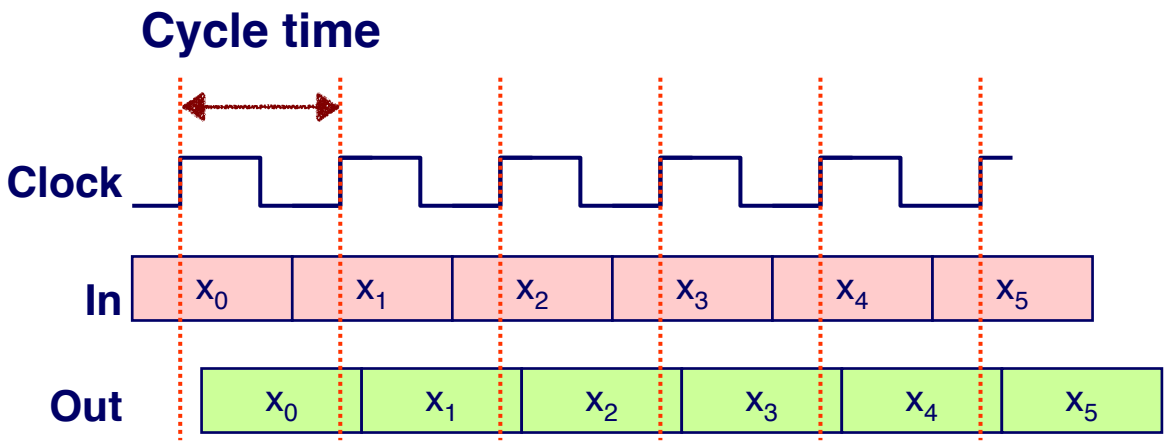
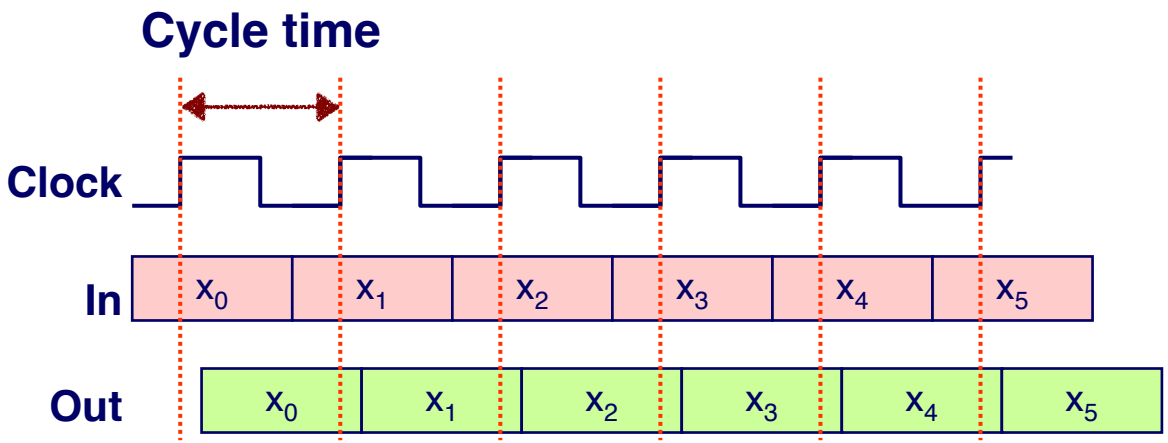


Clock Signal

- Cycle time of a clock signal: the time duration between two rising edges.
- Frequency of a clock signal: how many rising (falling) edges in 1 second.



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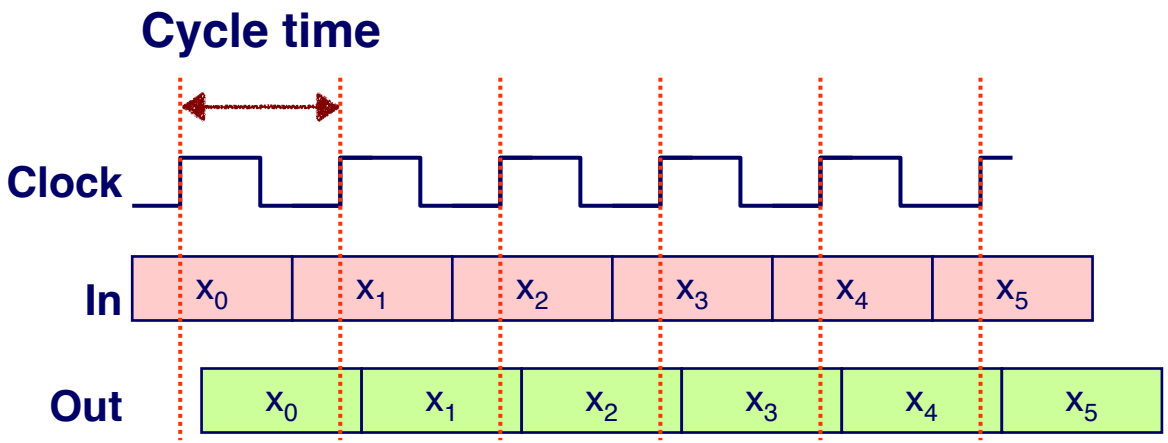
- 1 GHz CPU means the clock frequency is 1 GHz



Clock Signal

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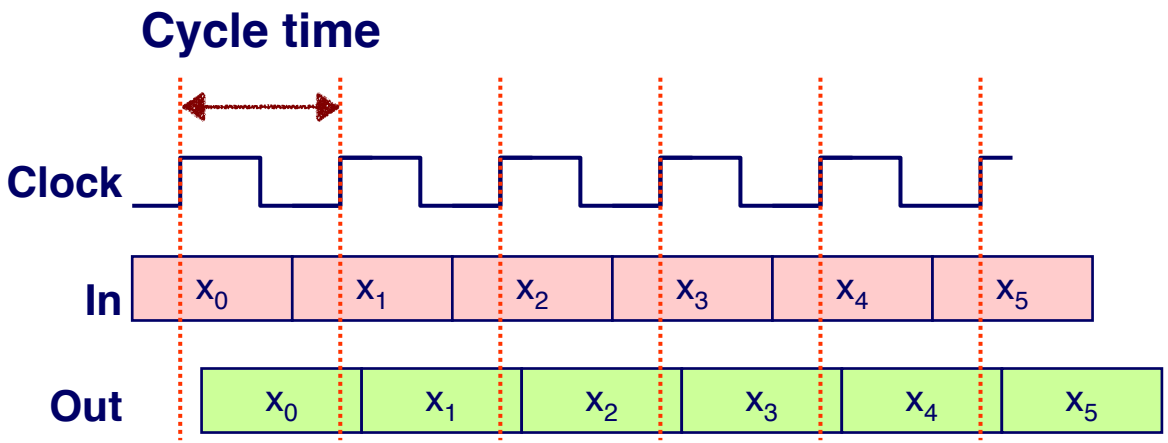
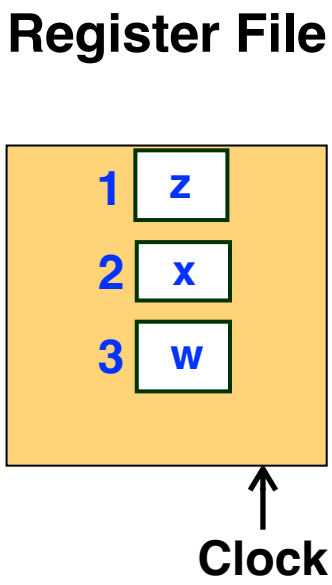
- 1 GHz CPU means the clock frequency is 1 GHz
  - The cycle time is 1/10^9 = 1 ns



Register File

- A register file consists of a set of registers that you can individually read from and write to.



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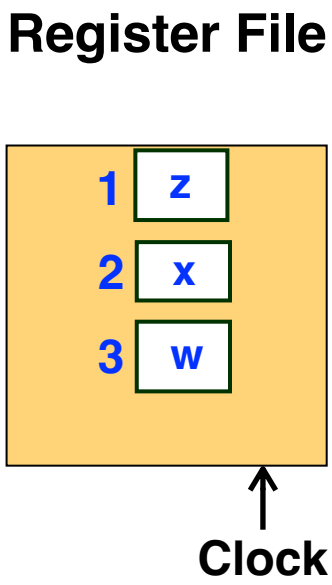

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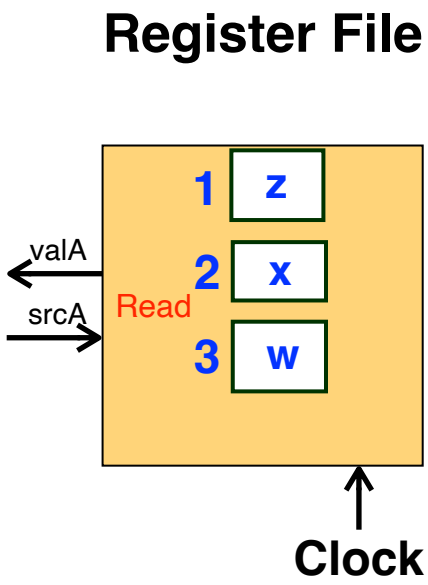

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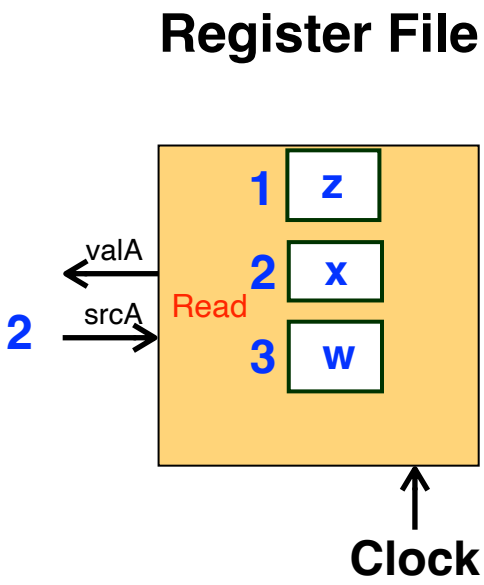

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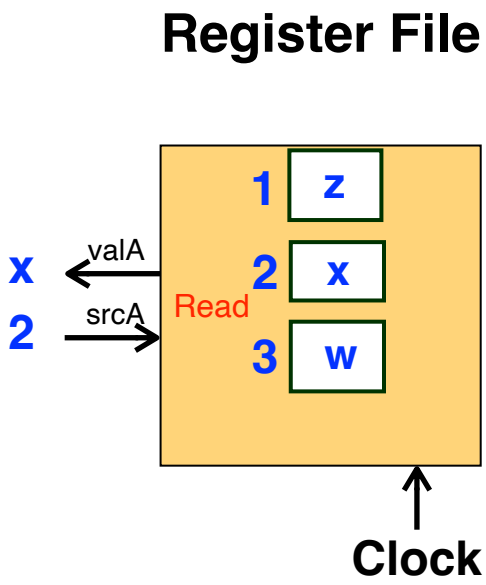

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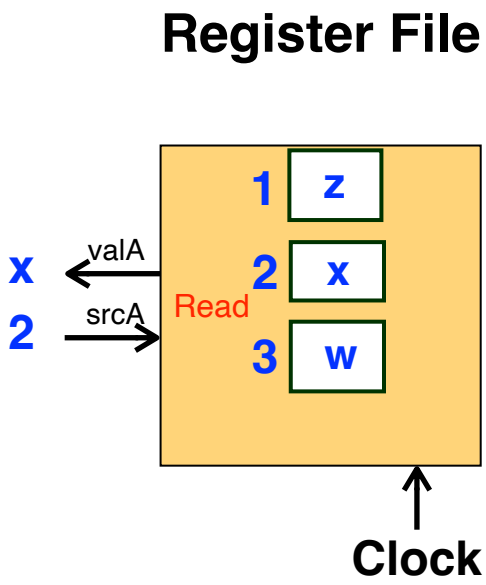

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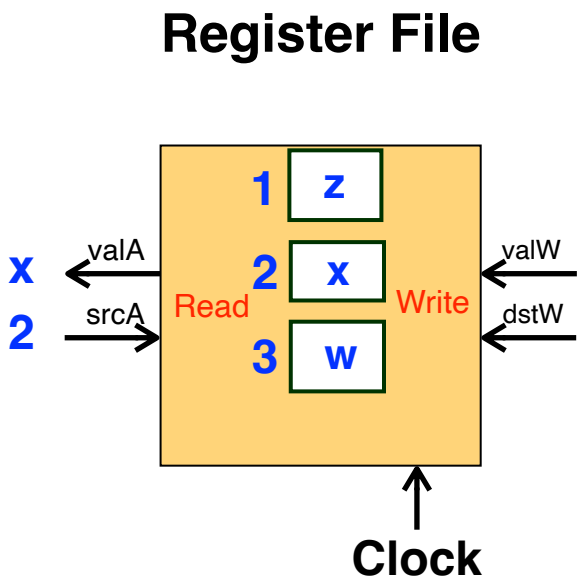

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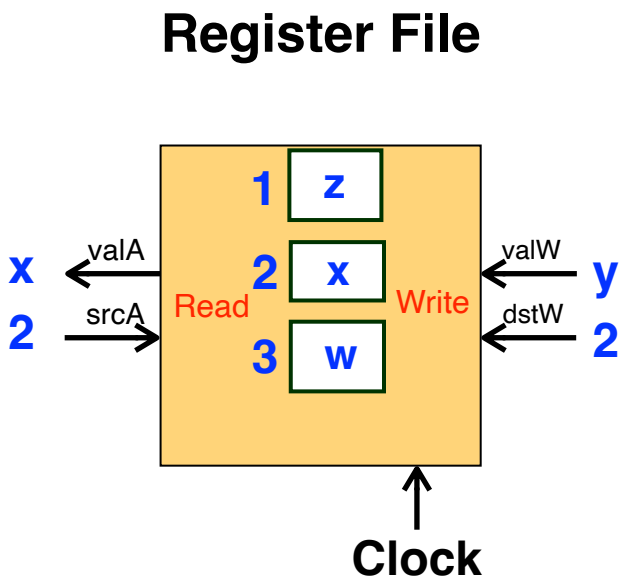

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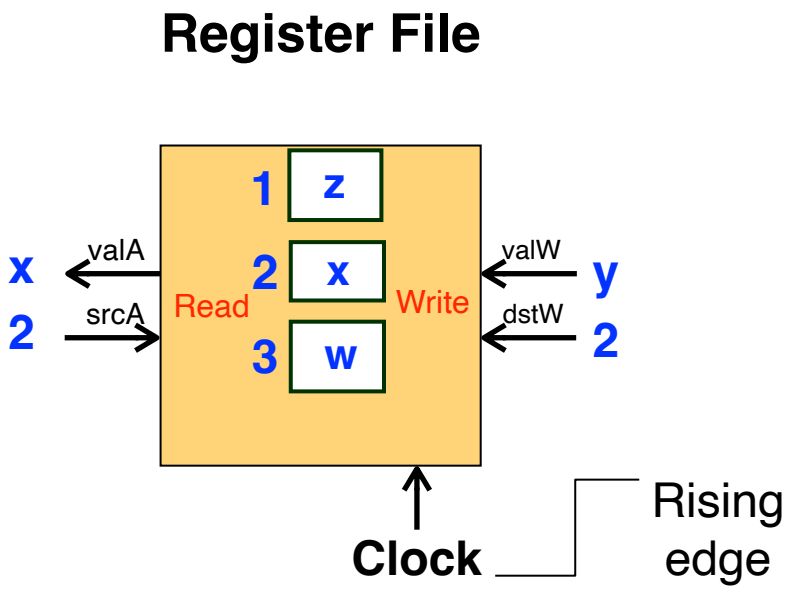

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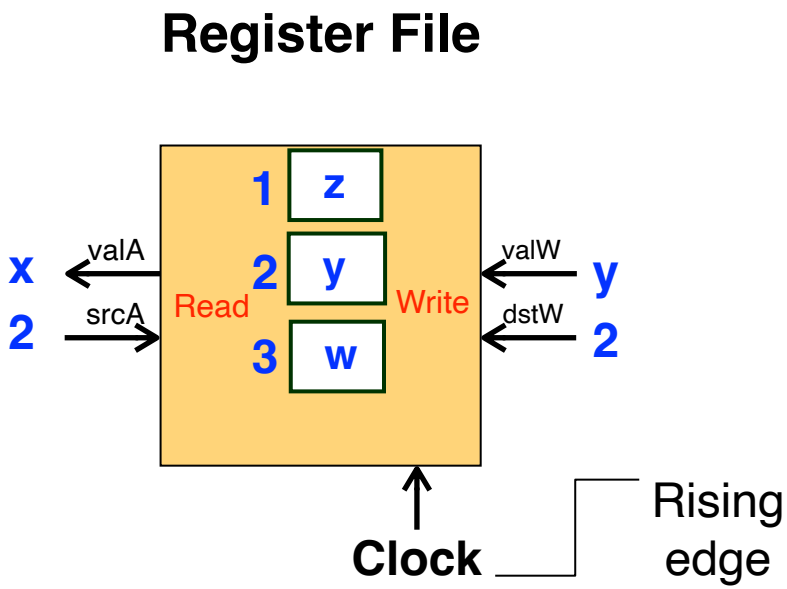

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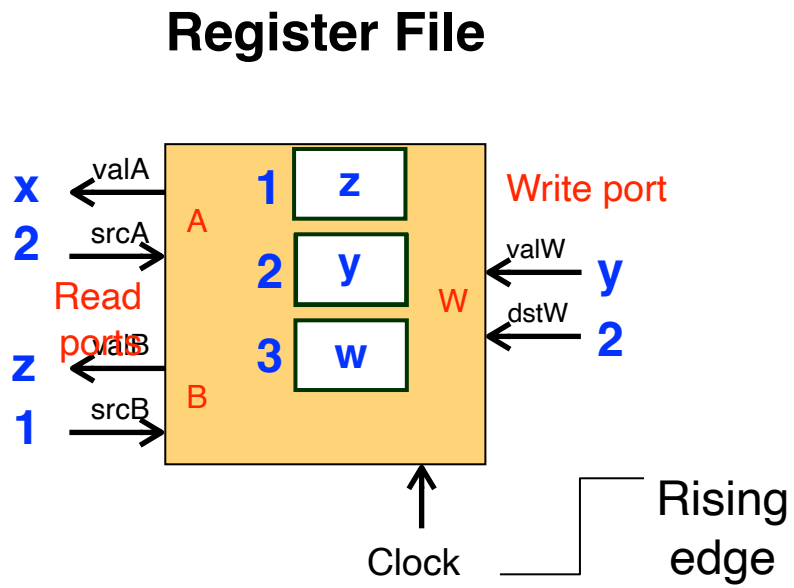


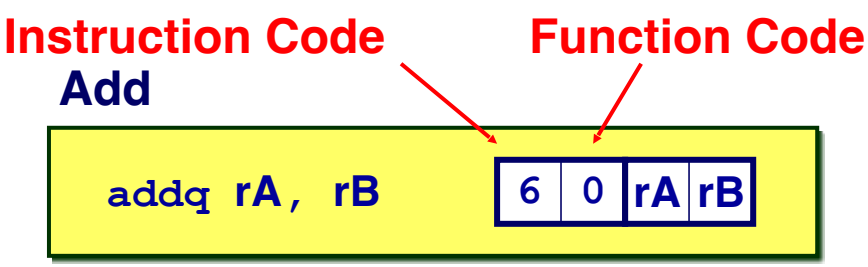
- Stores multiple registers of data
  - Address input specifies which register to read or write
- **Multiple Ports:** Can read and/or write multiple words in one cycle. Each port has separate address and data input/output

Processor Microarchitecture

- Sequential, single-cycle microarchitecture implementation
  - Basic idea
  - Hardware implementation
- Pipelined microarchitecture implementation
  - Basic Principles
  - Difficulties: Control Dependency
  - Difficulties: Data Dependency

Executing an ADD instruction

- How does the processor execute `addq %rax,%rsi`
- The binary encoding is `60 06`



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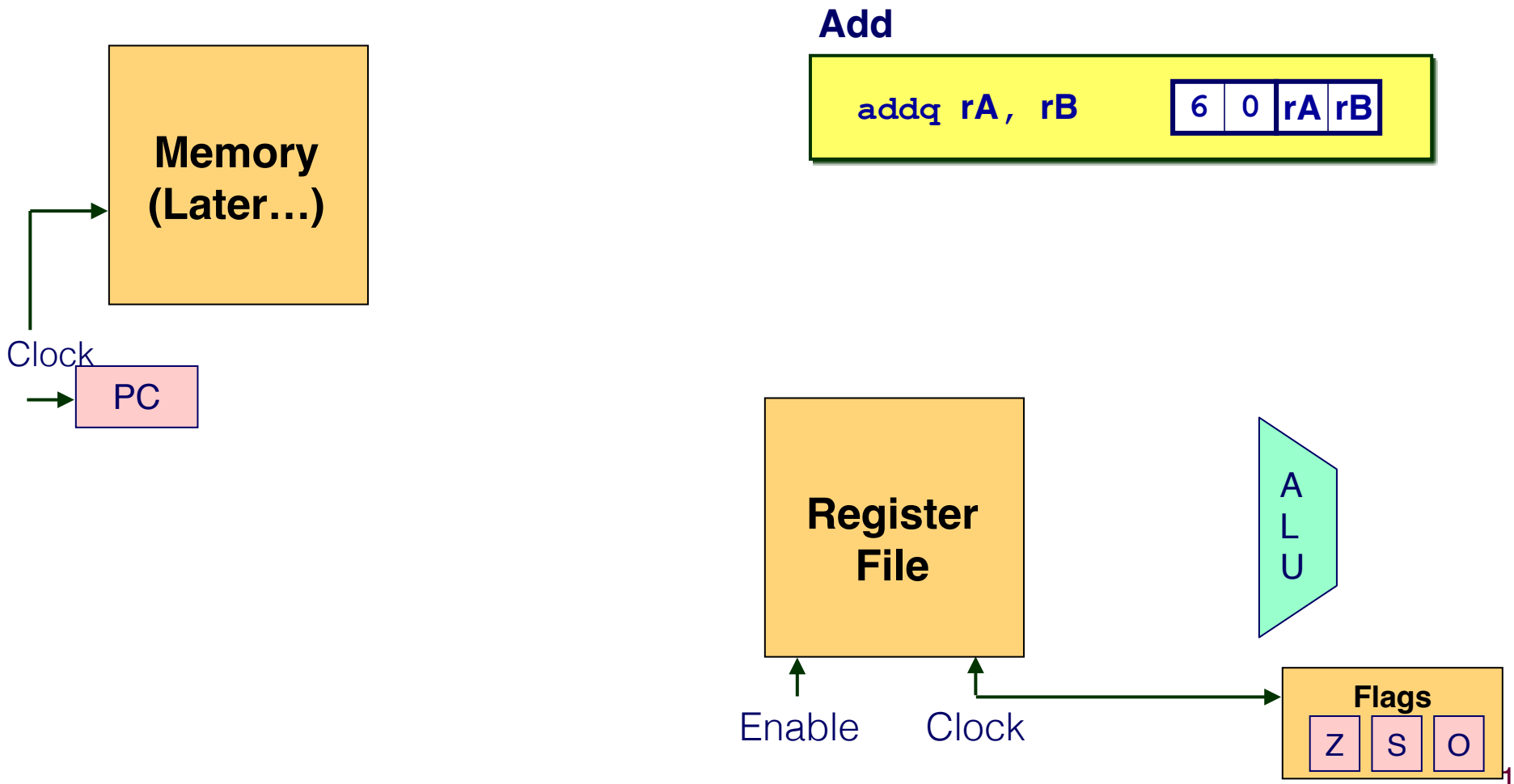

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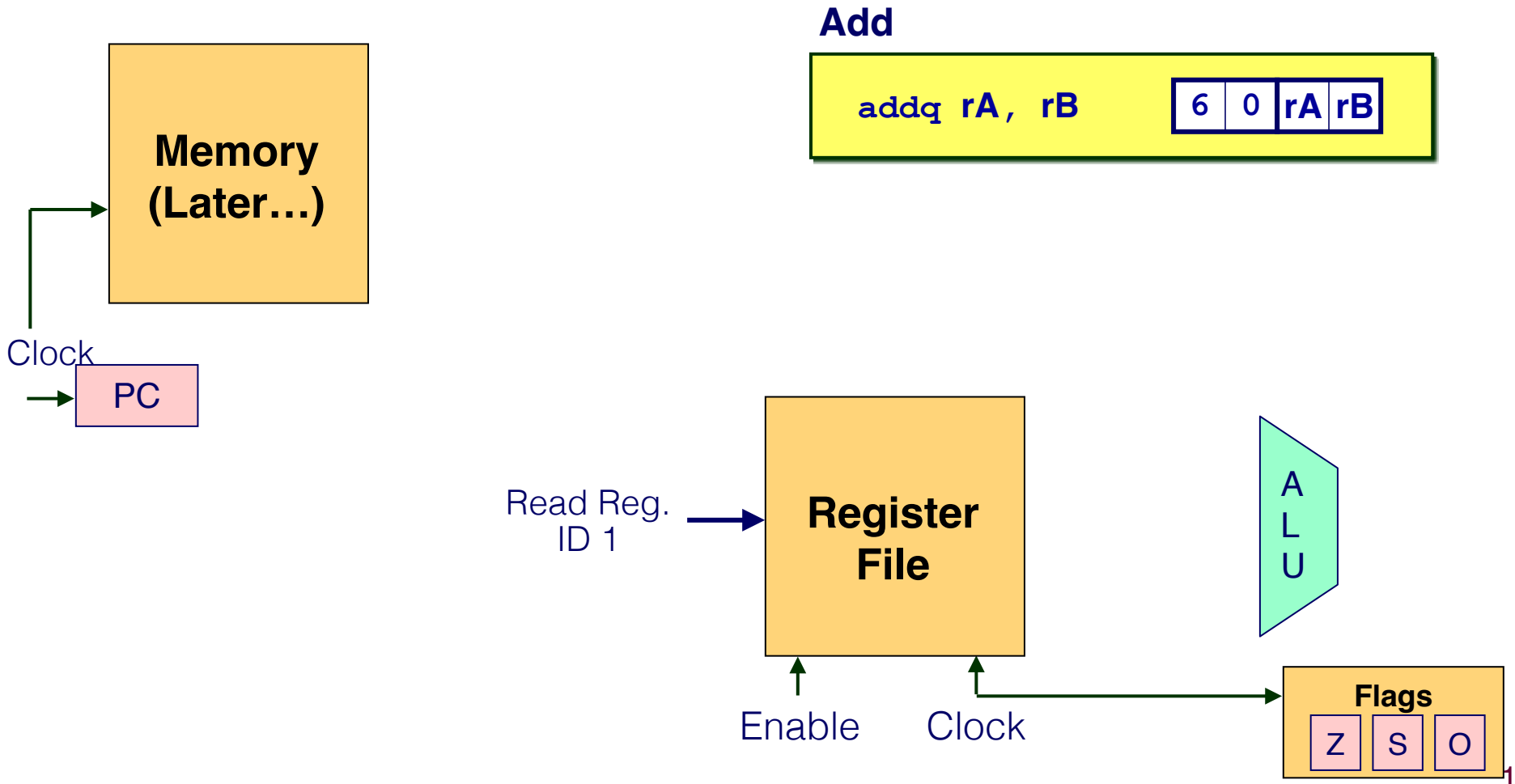

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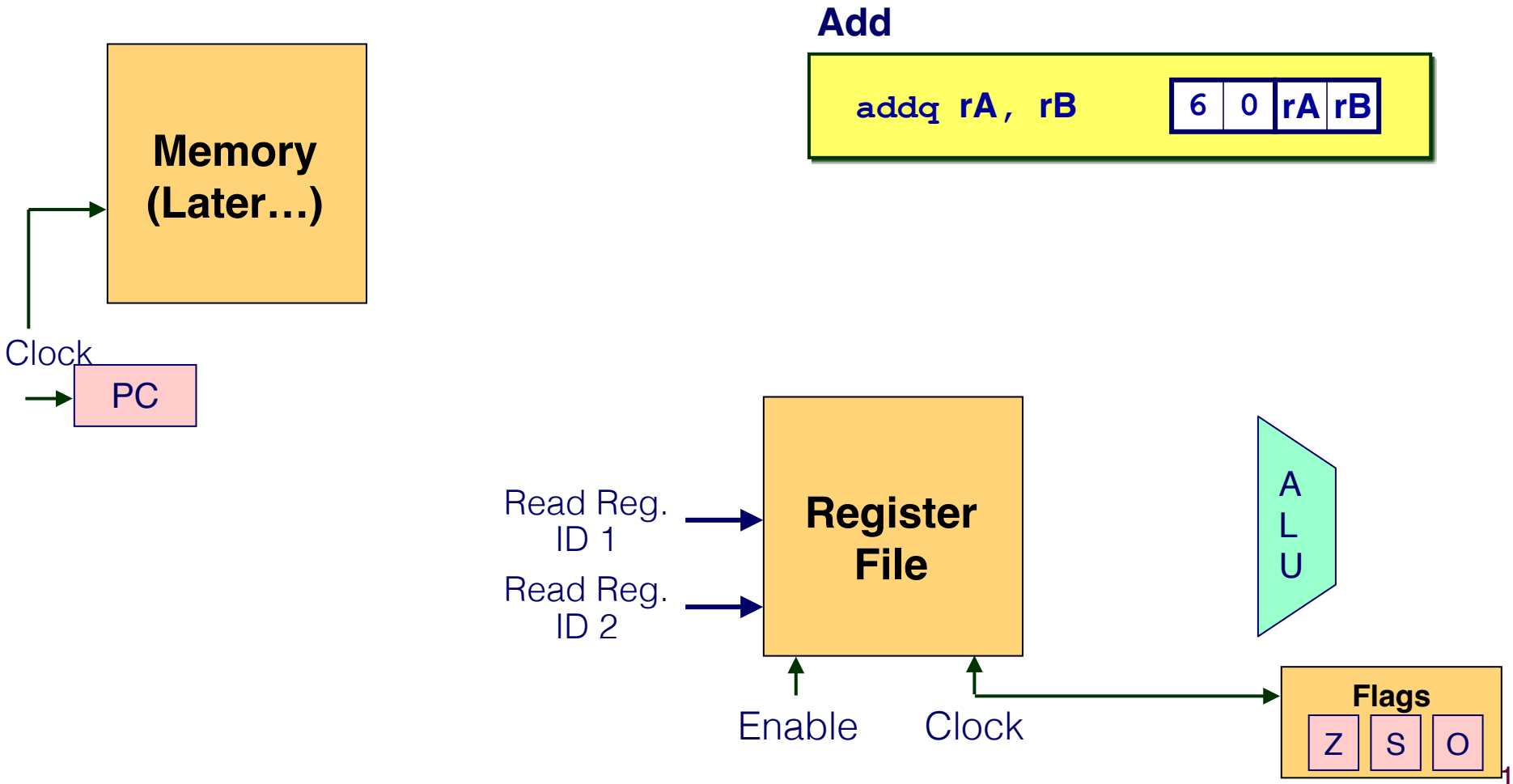

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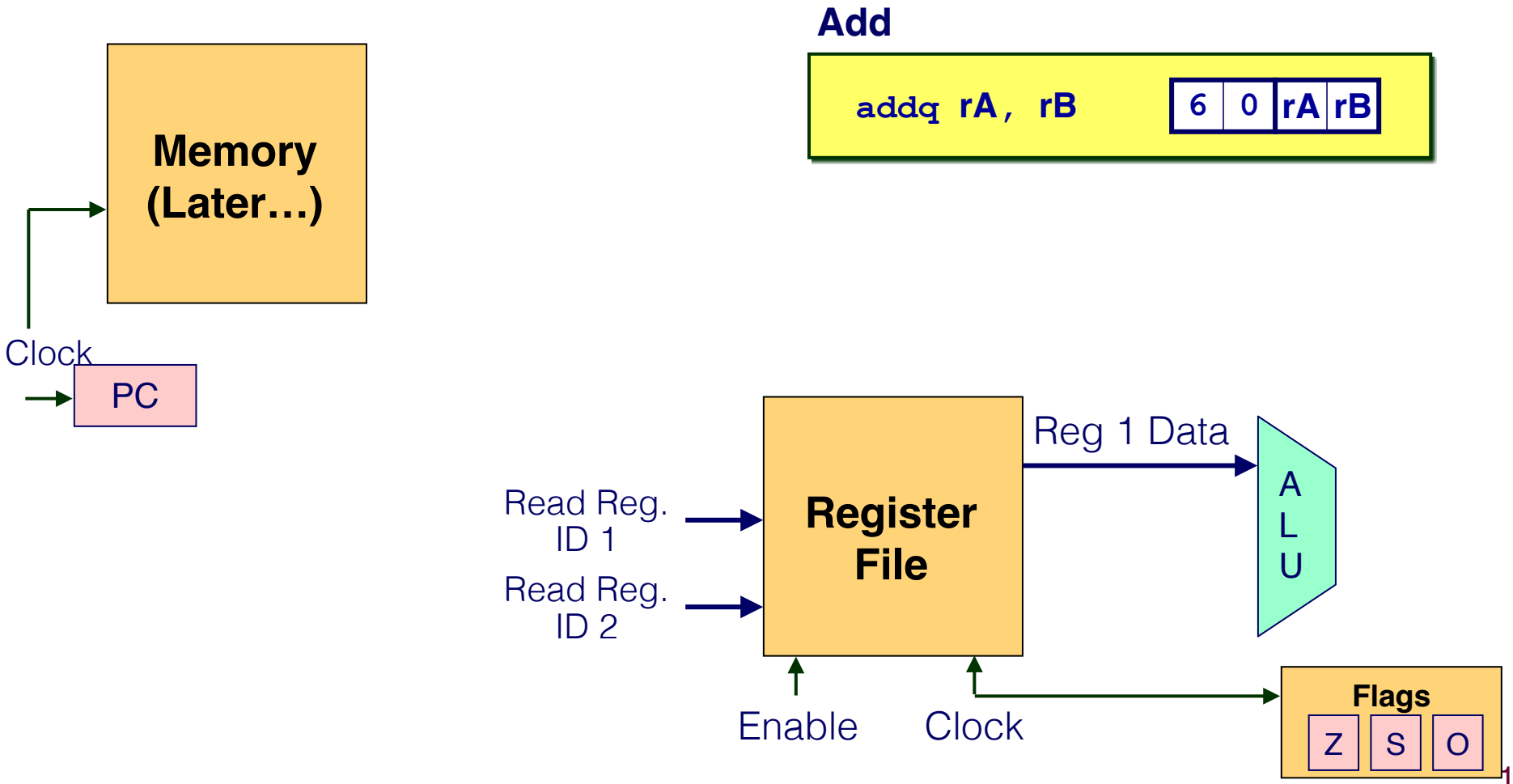

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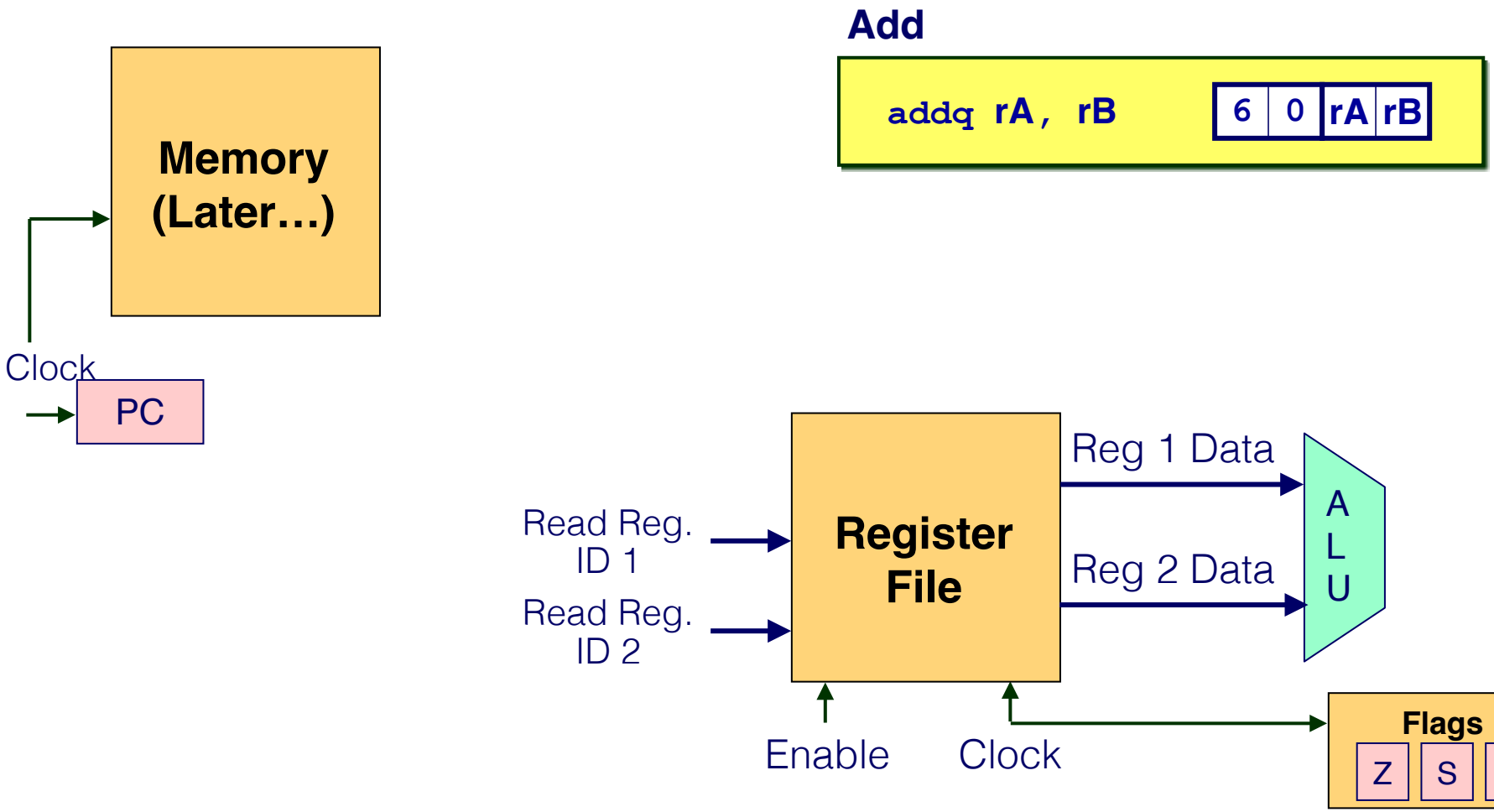

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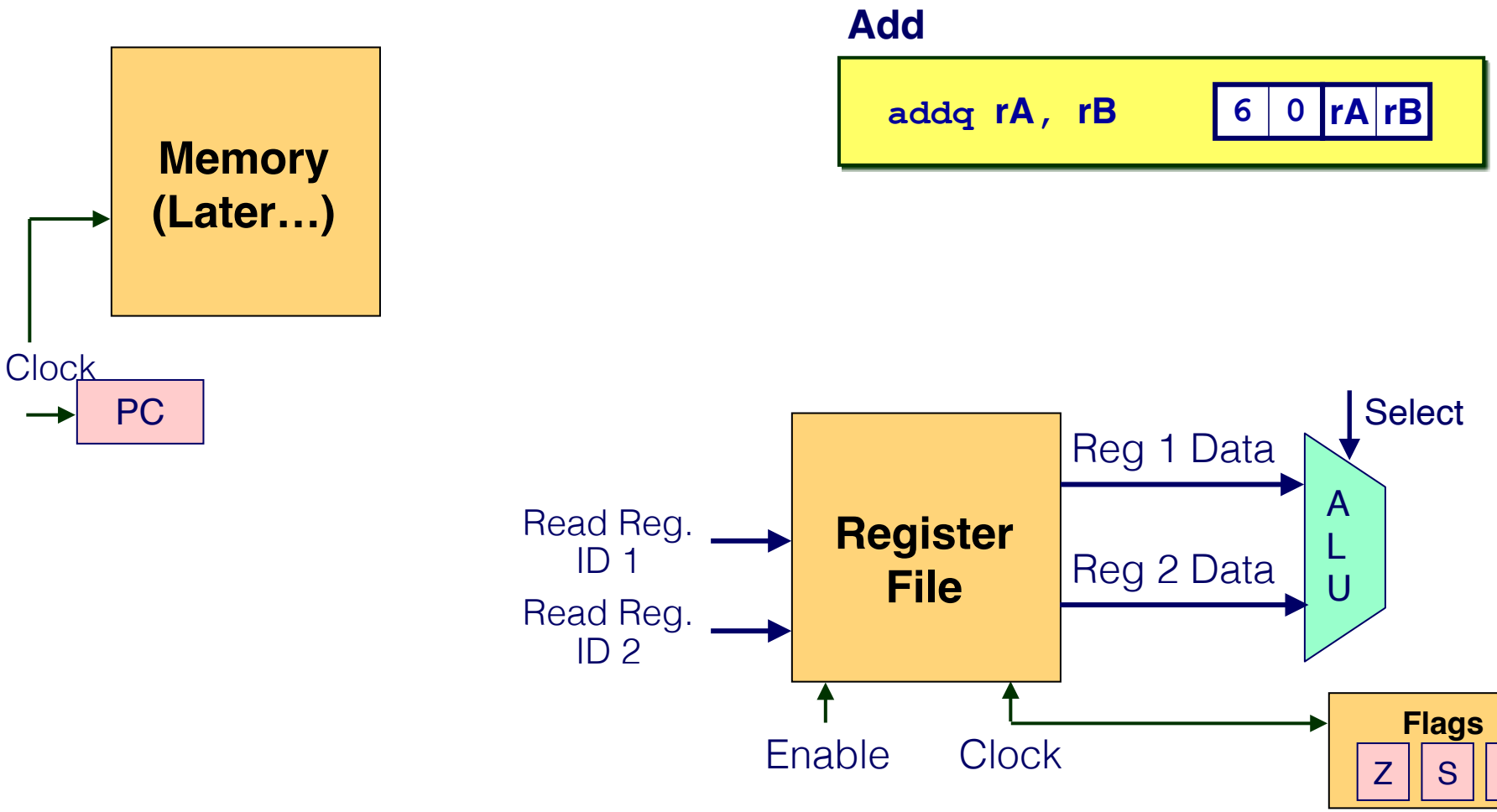

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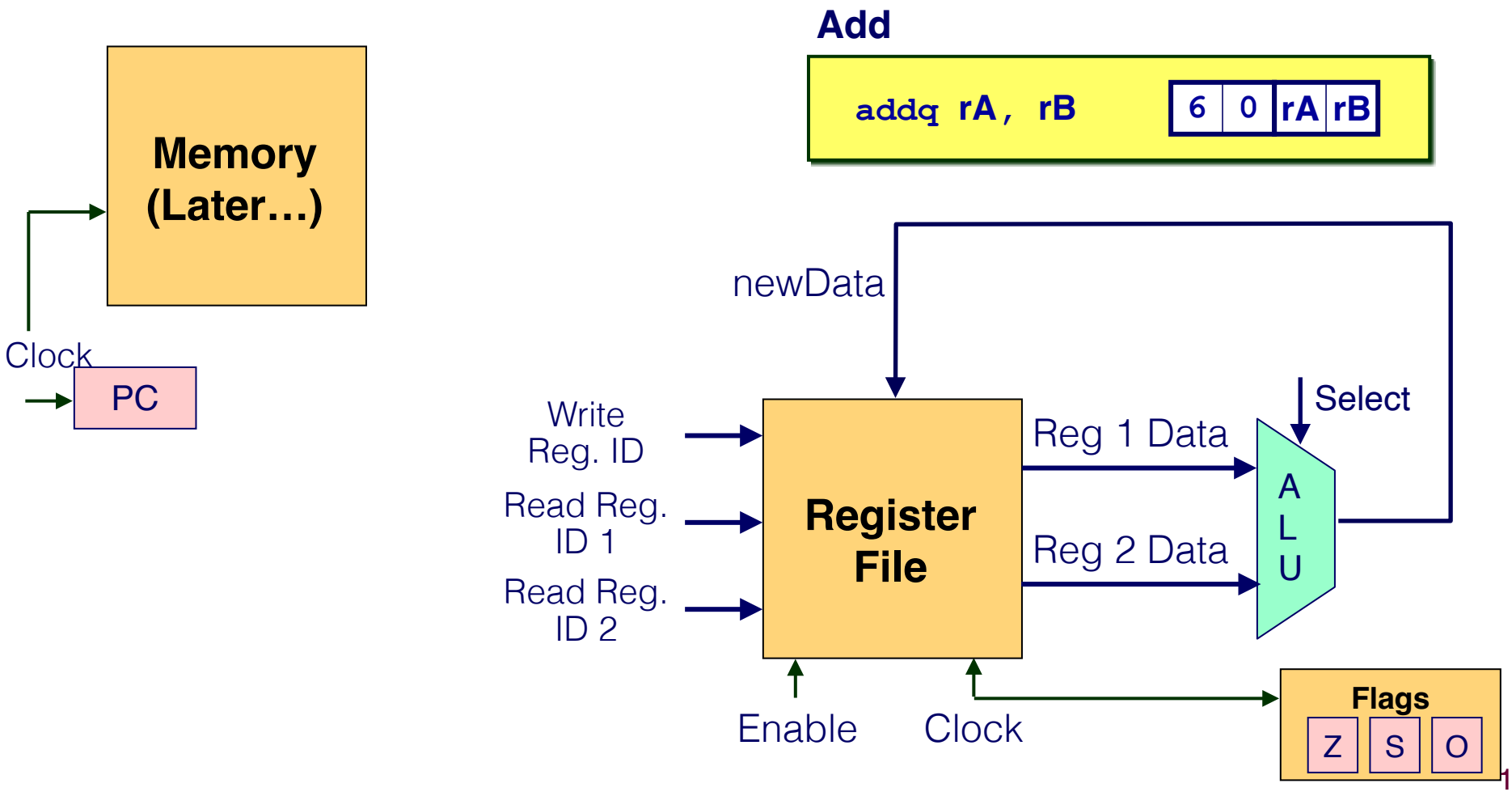

Executing an ADD instruction

- How does the processor execute `addq %rax,%rsi`
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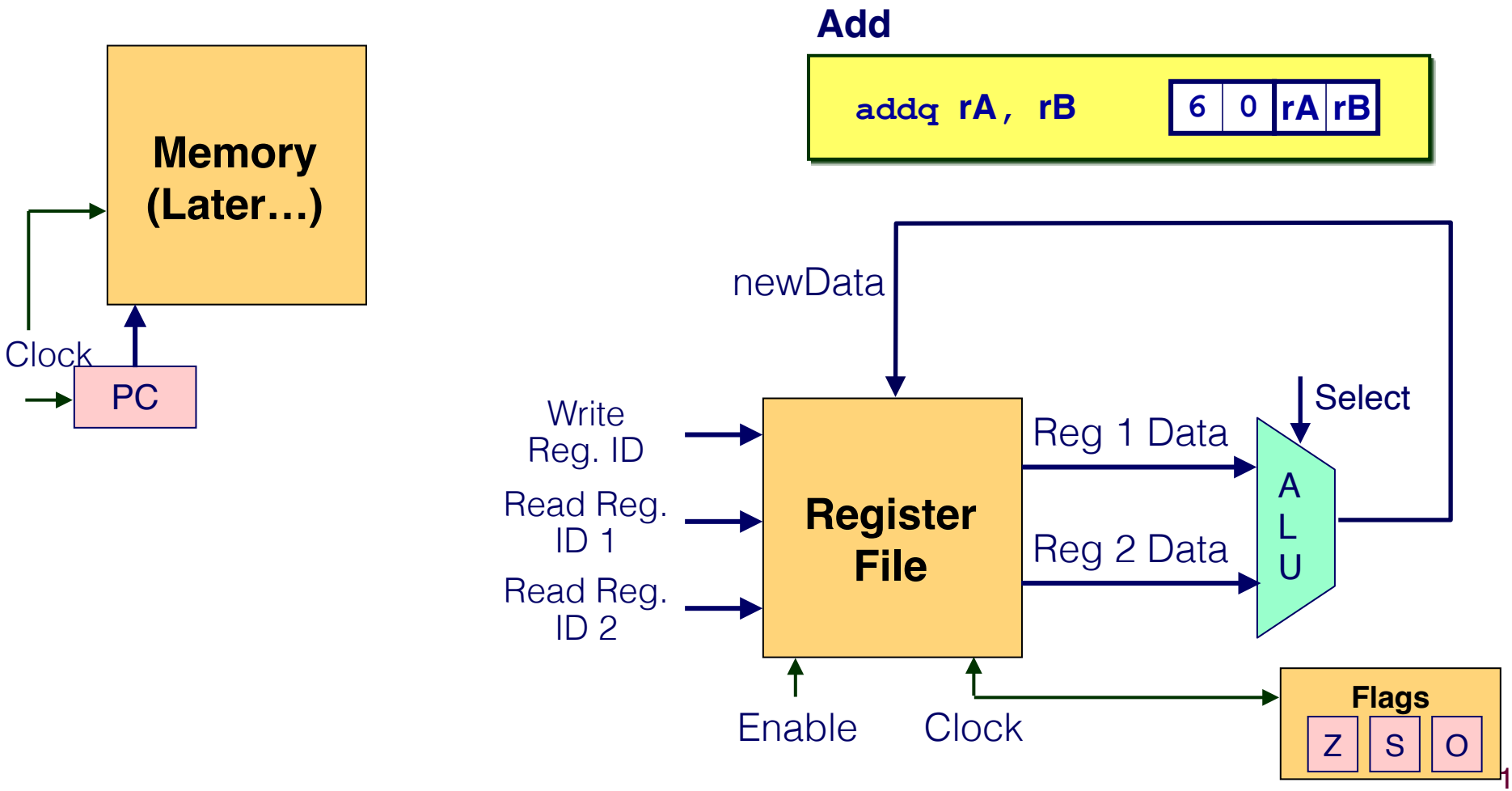

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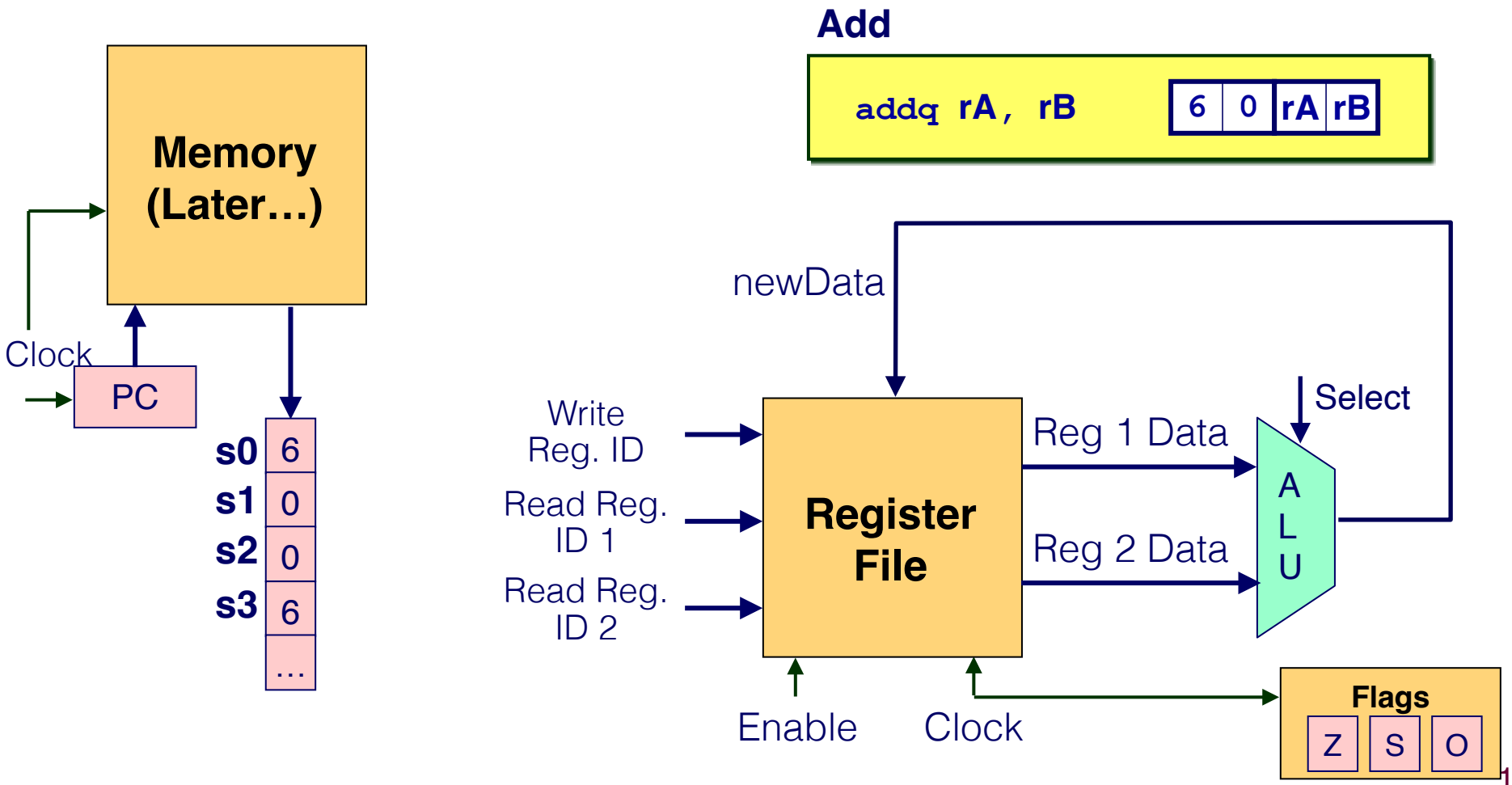

Executing an ADD instruction

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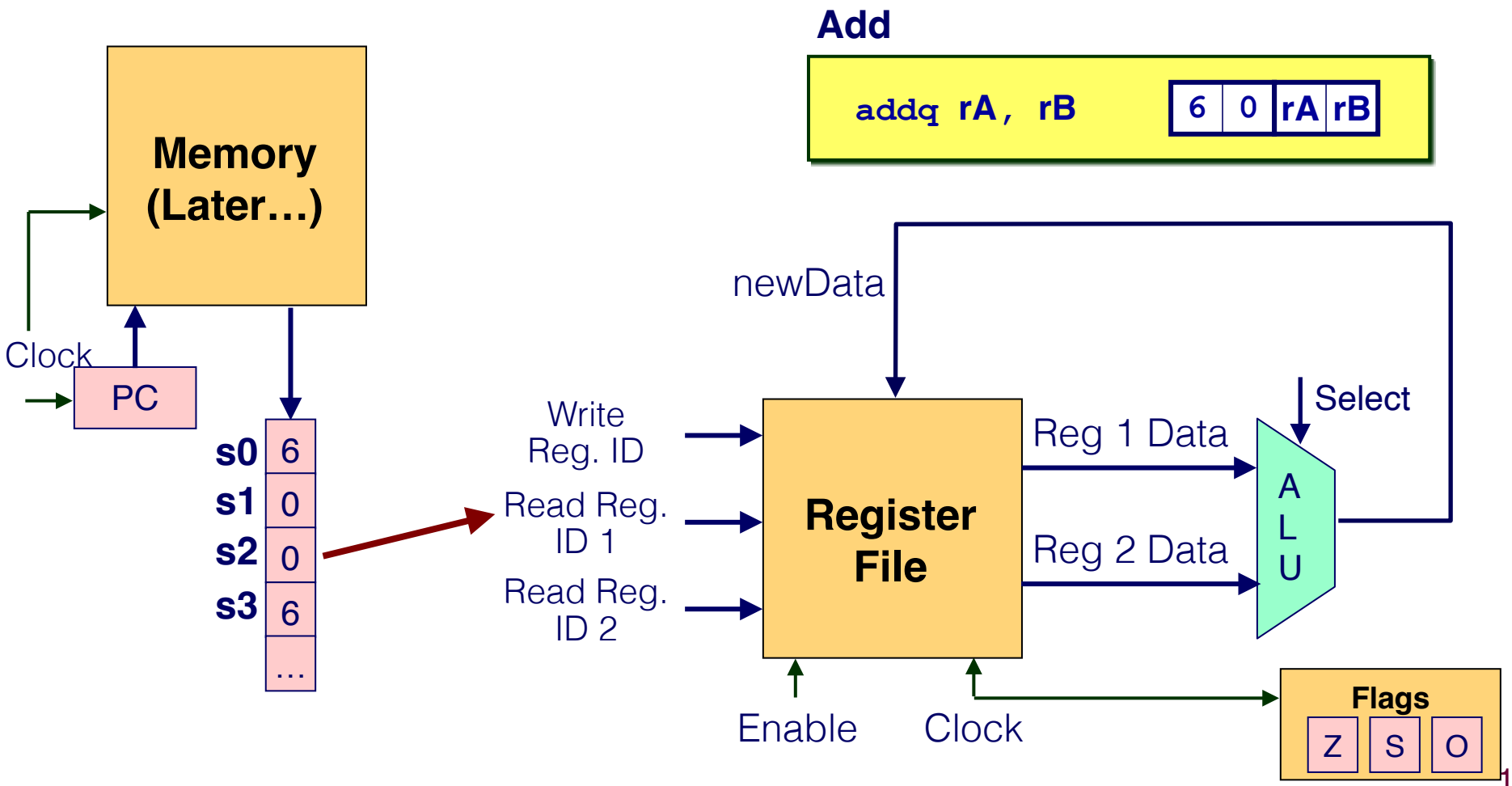

Executing an ADD instruction

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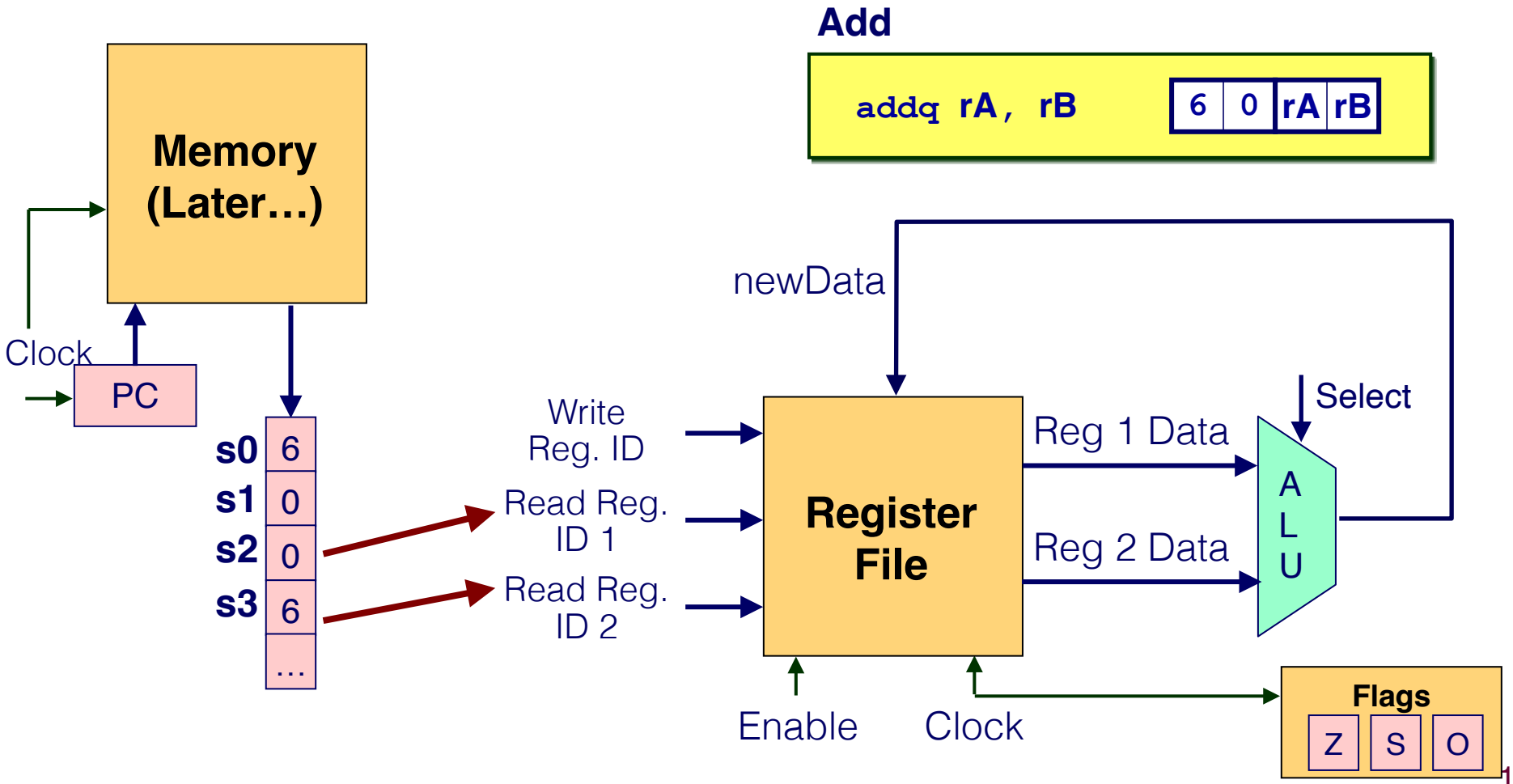

Executing an ADD instruction

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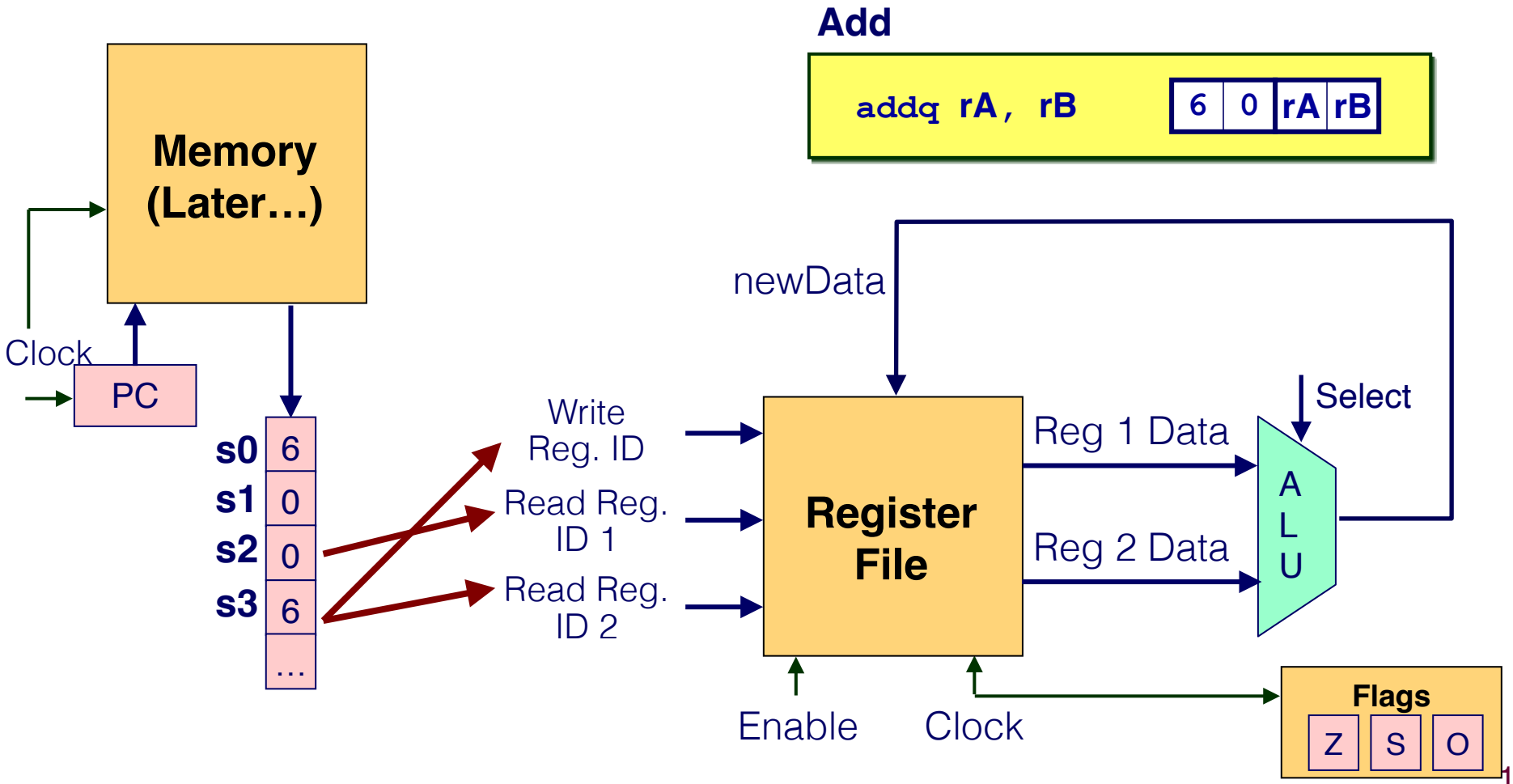

Executing an ADD instruction

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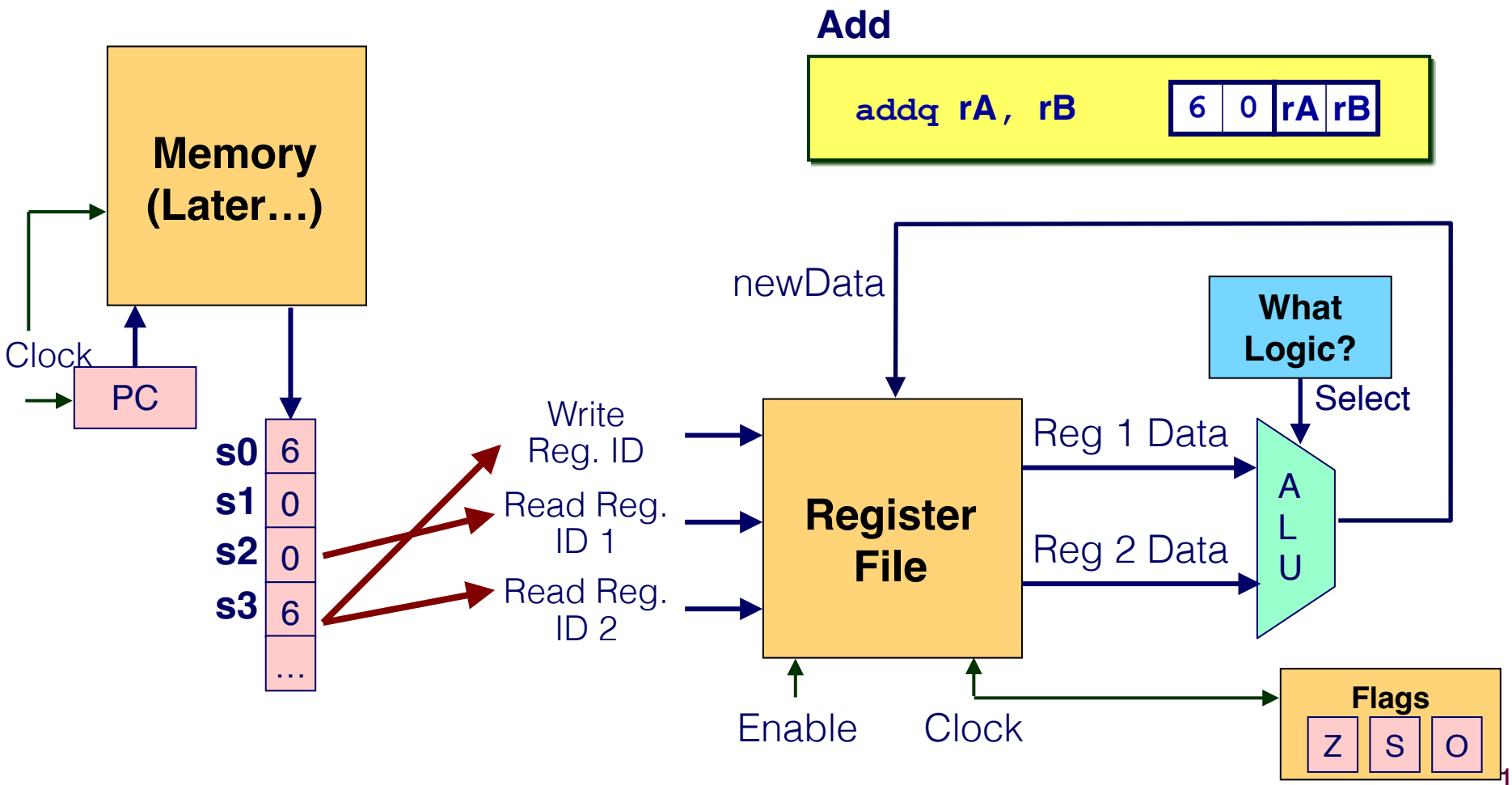

Executing an ADD instruction

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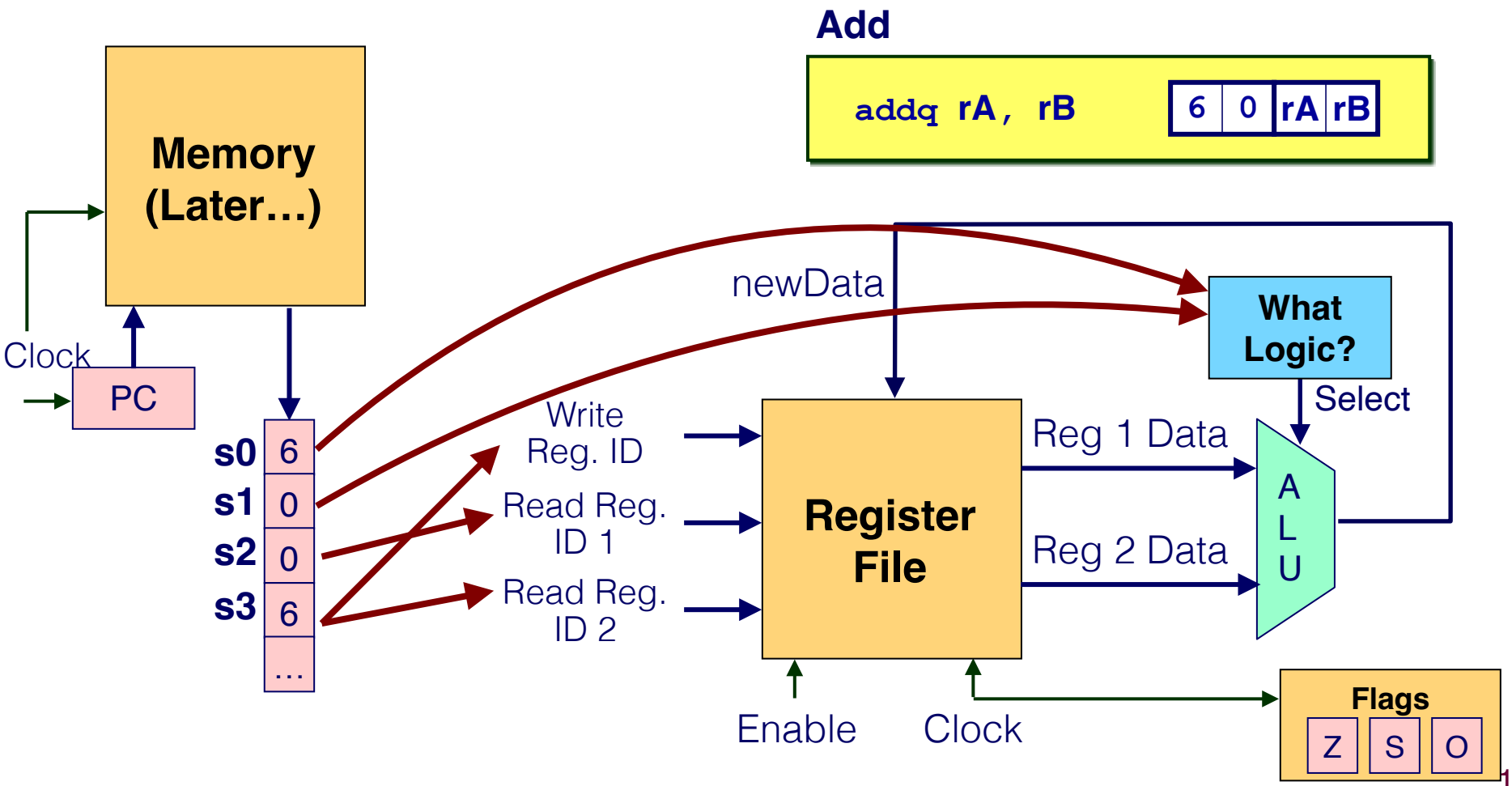
- The binary encoding is `60 06`



Executing an ADD instruction

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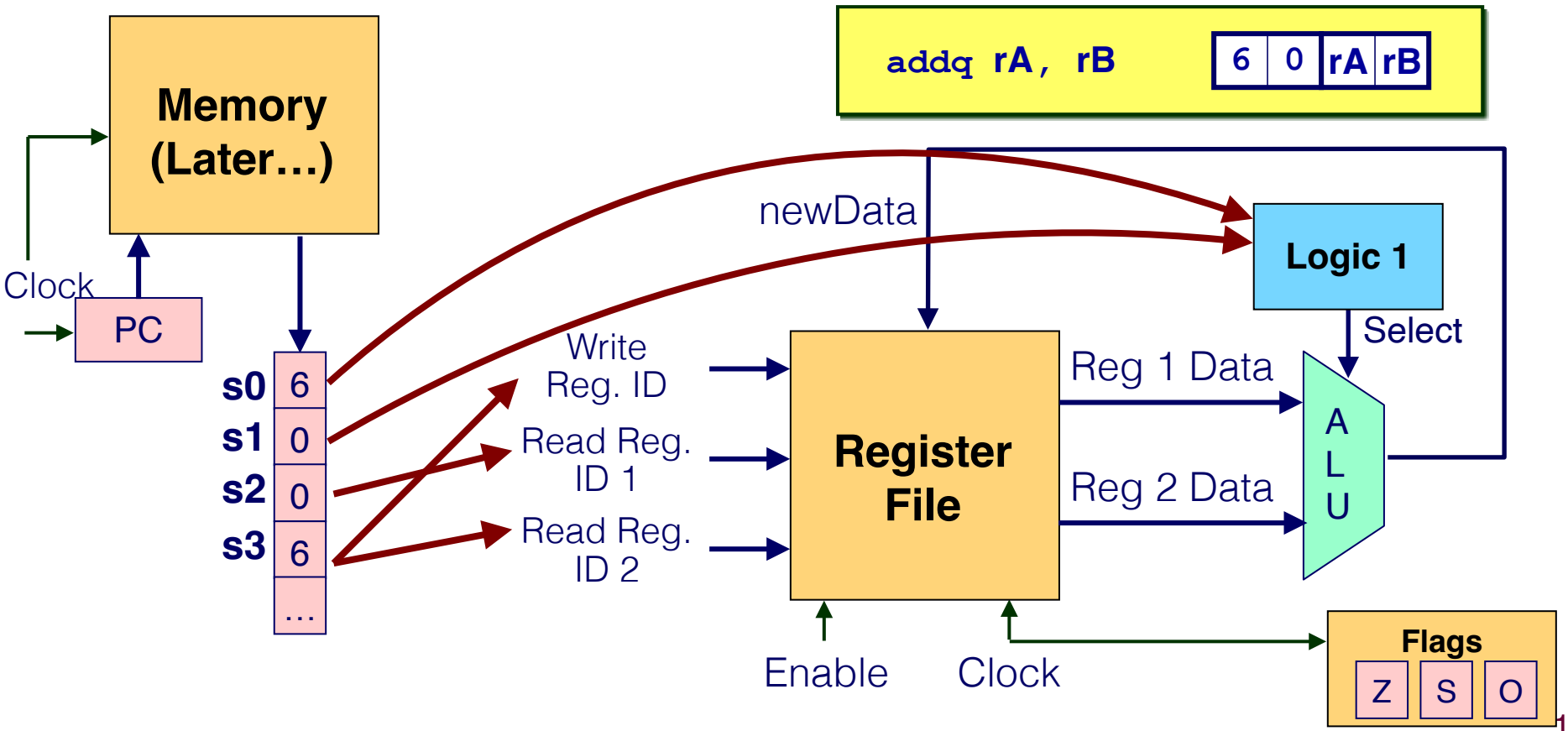

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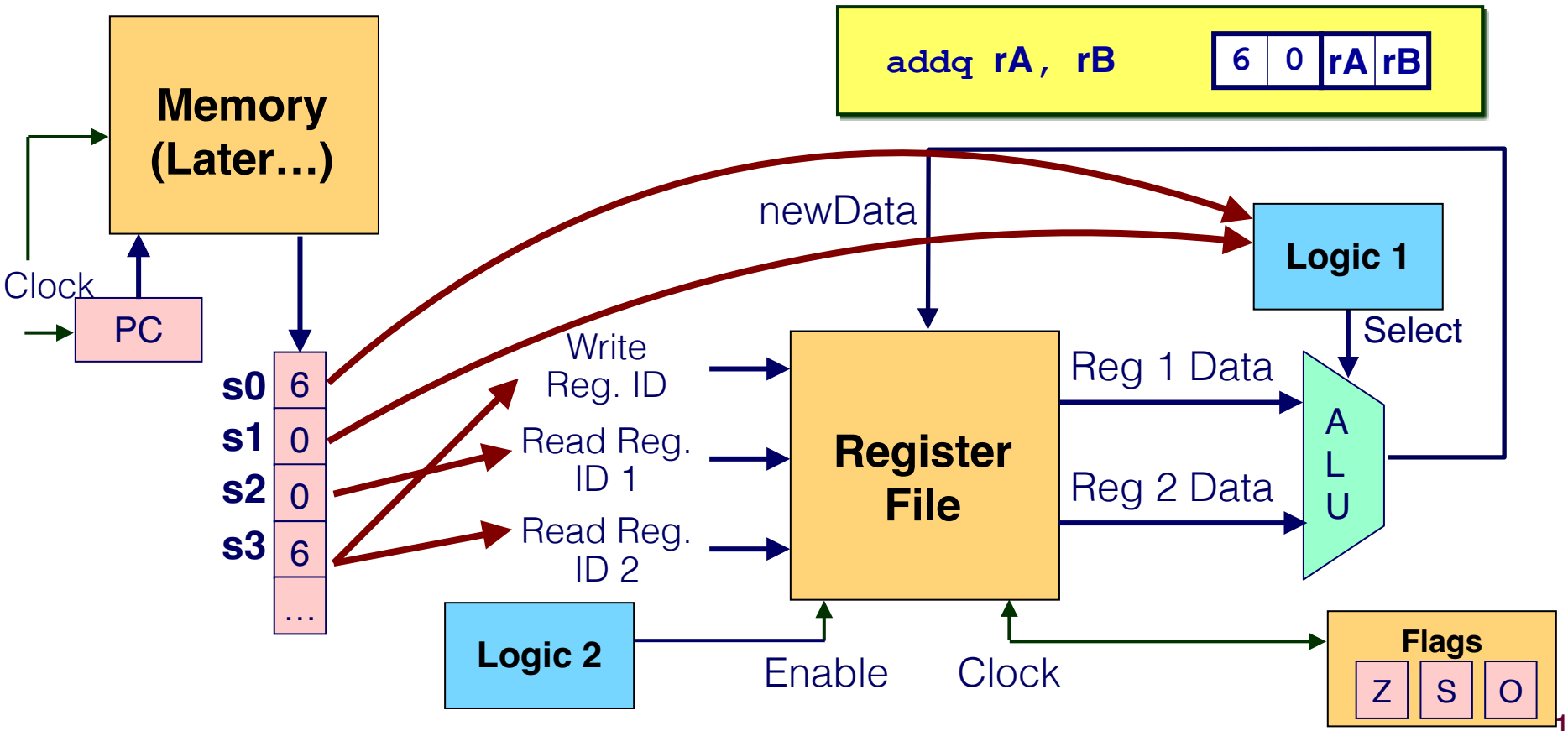

Executing an ADD instruction

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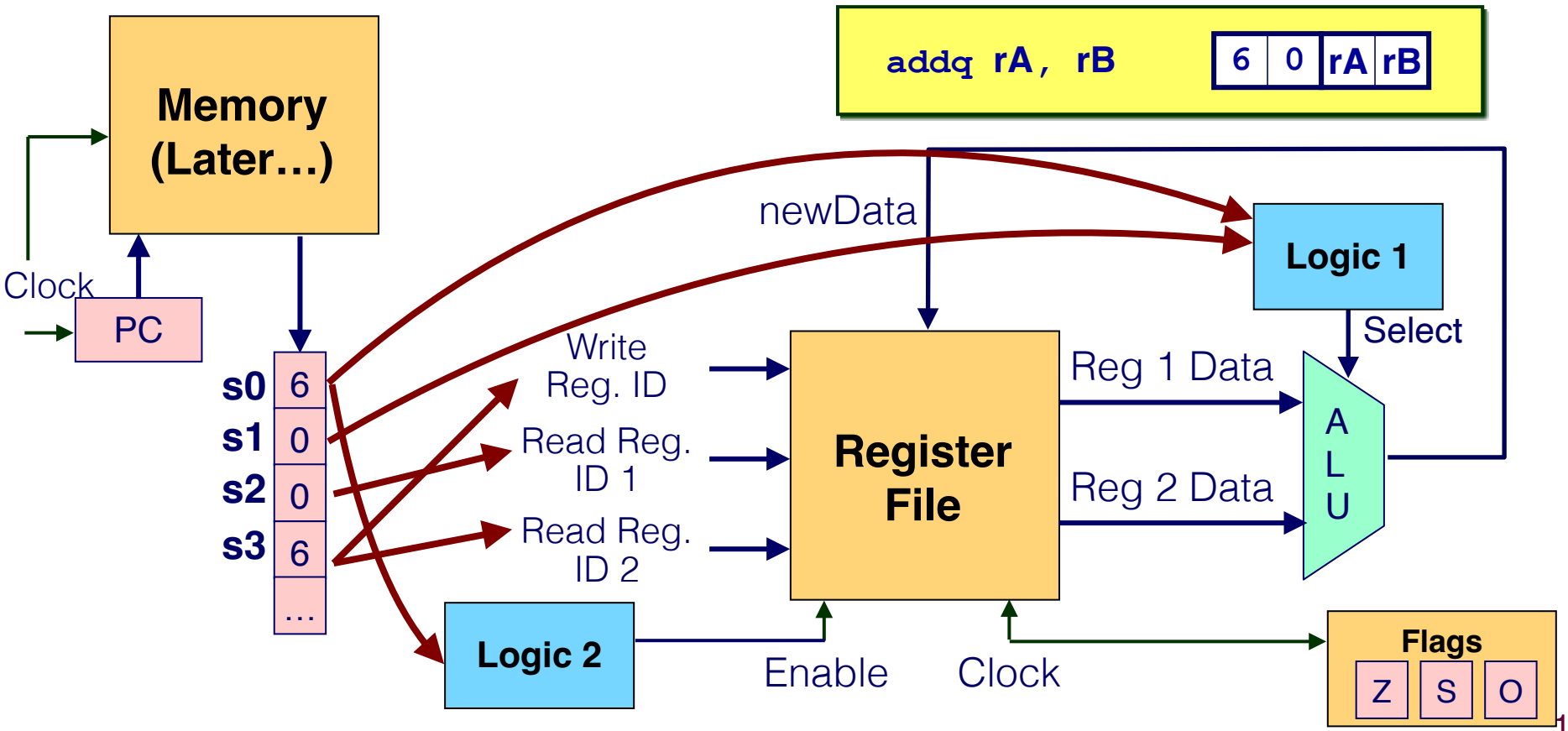
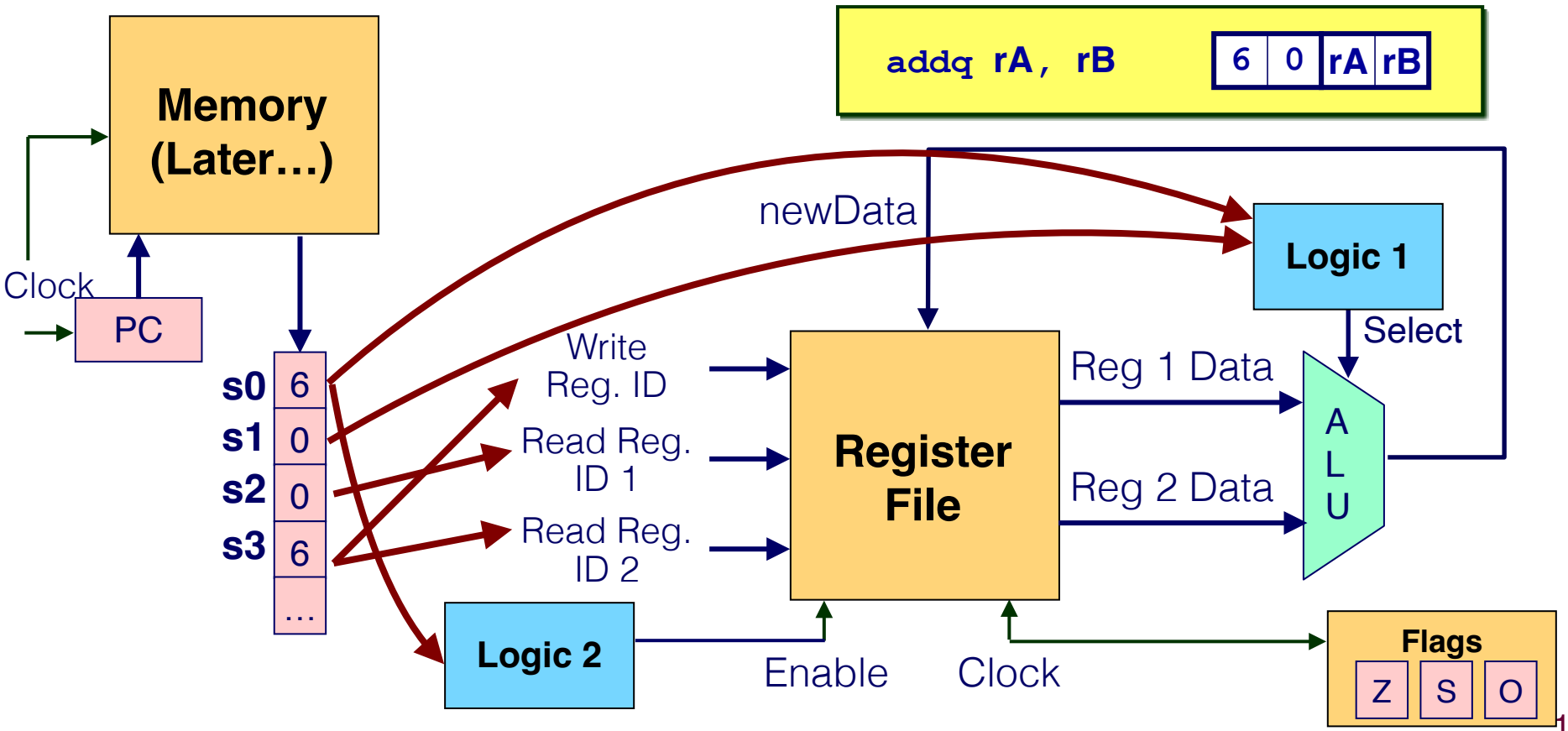


Executing an ADD instruction

- Logic 1: if (s0 == 6) select = s1;
- Logic 2: if (s0 == 6) Enable = 1; else Enable = 0;



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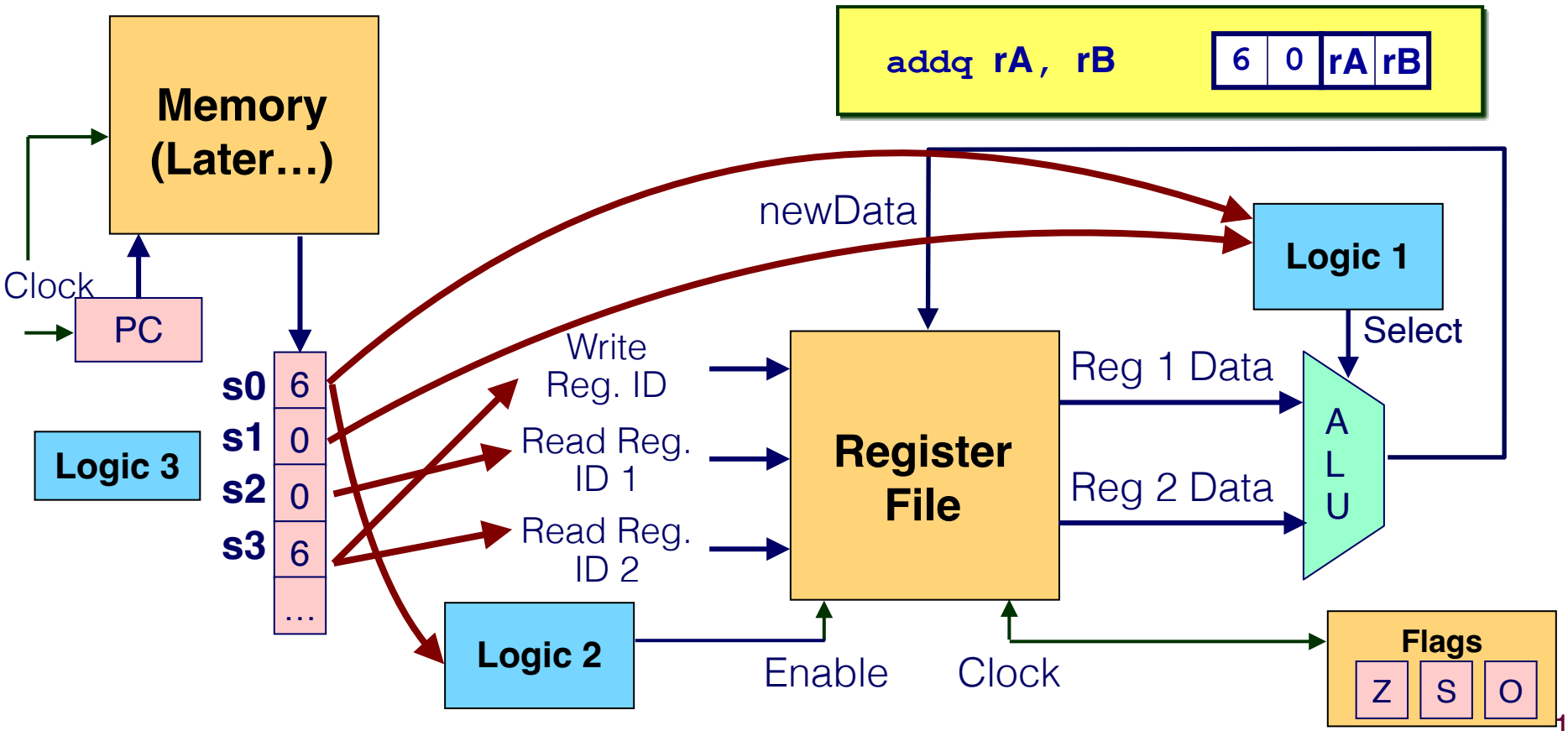

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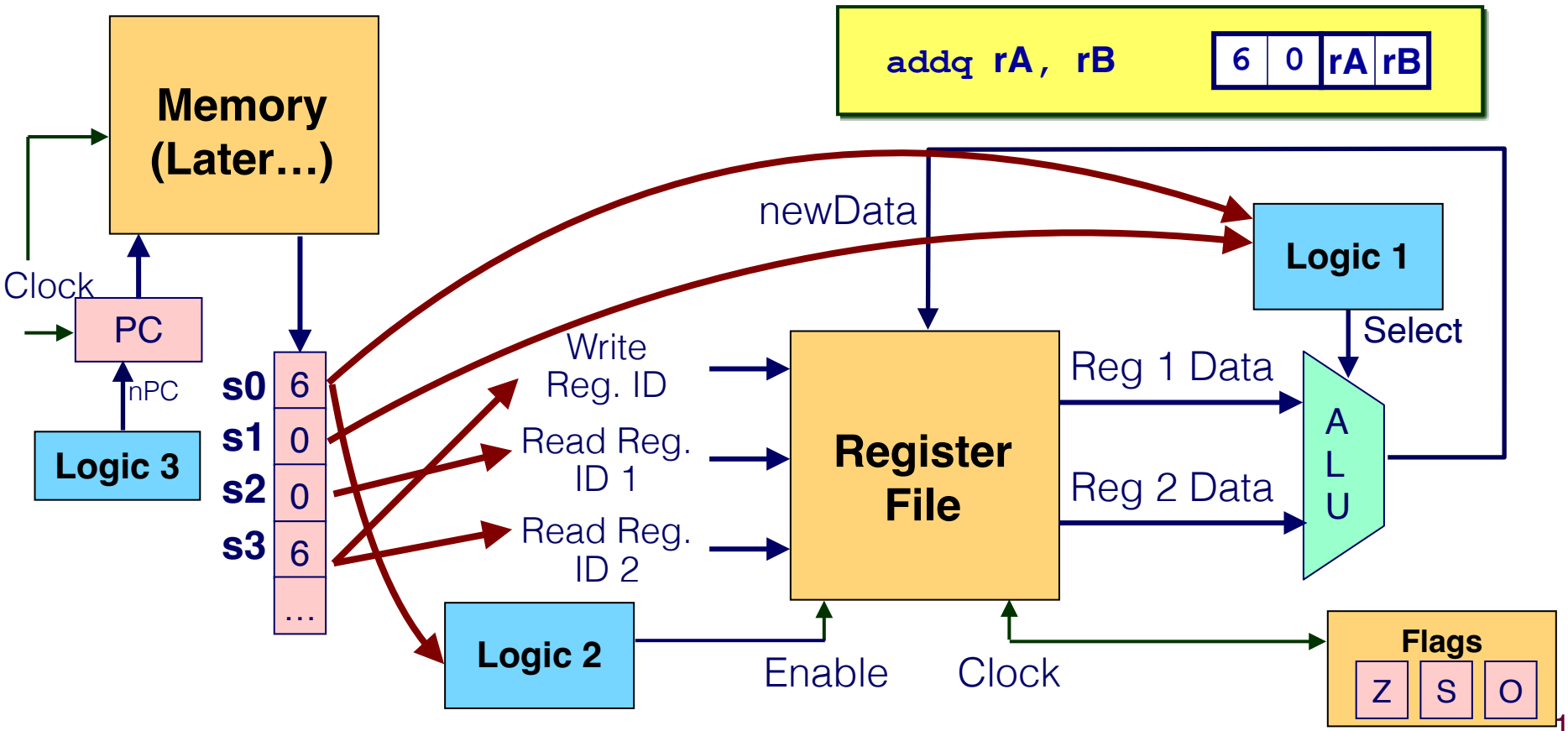

Executing an ADD instruction

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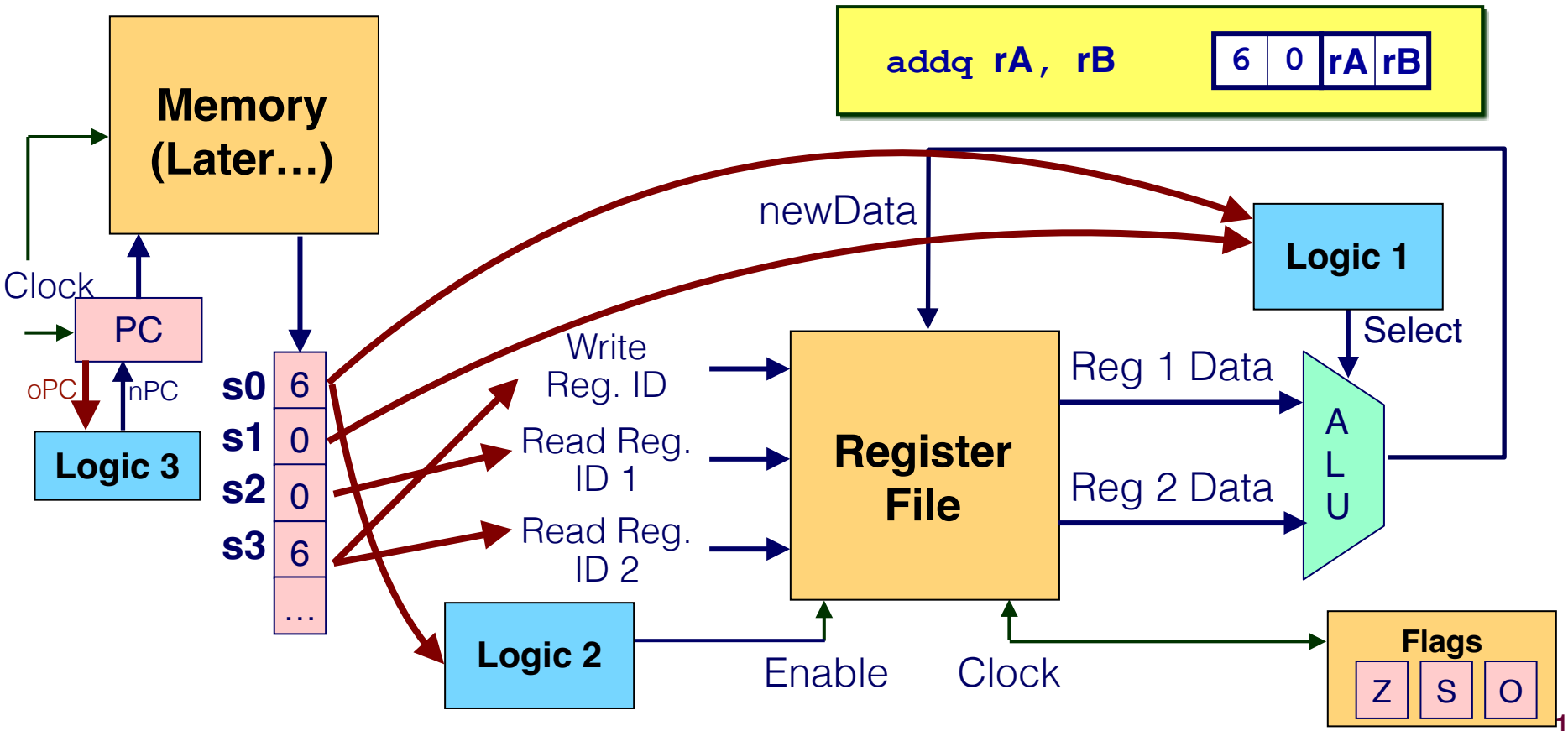

Executing an ADD instruction

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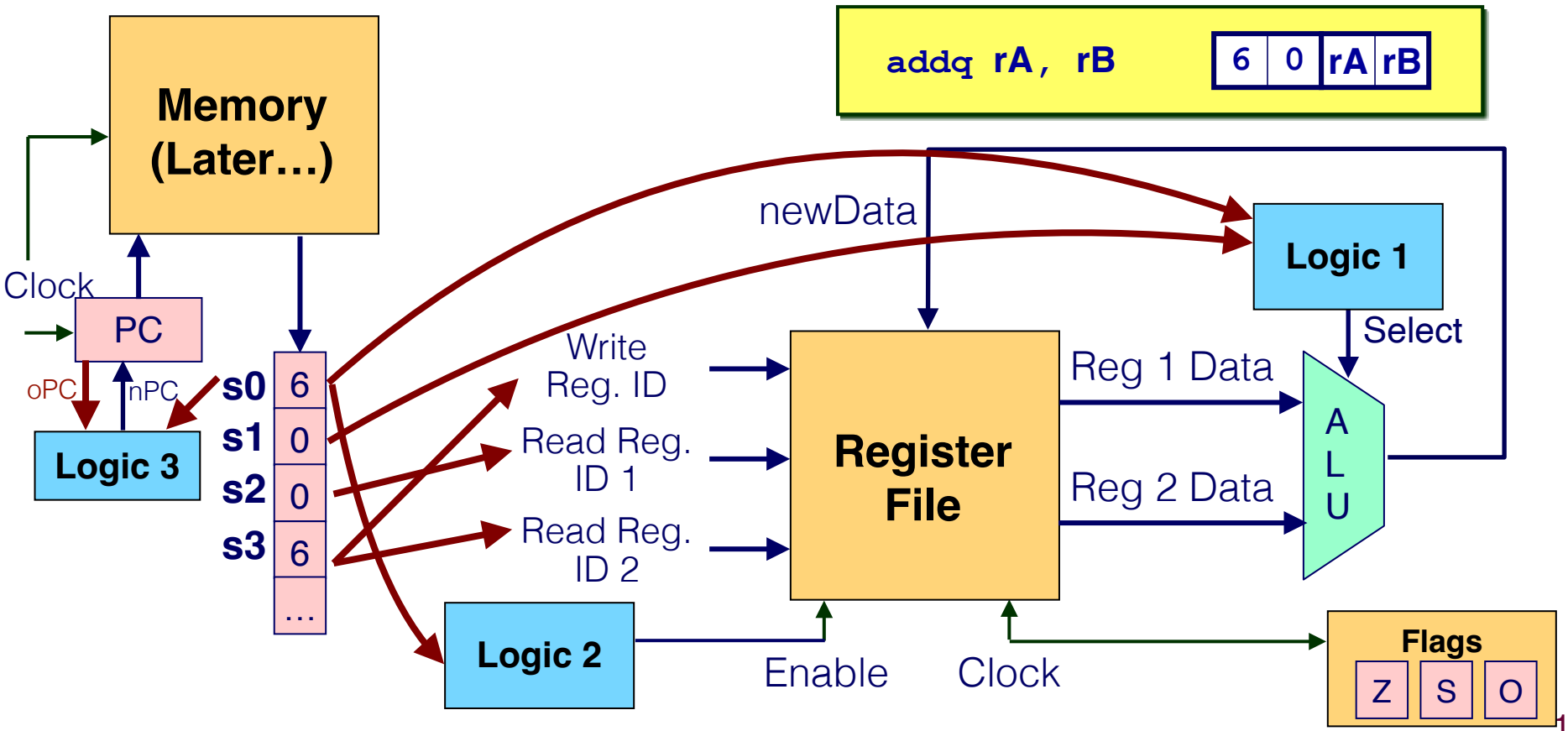
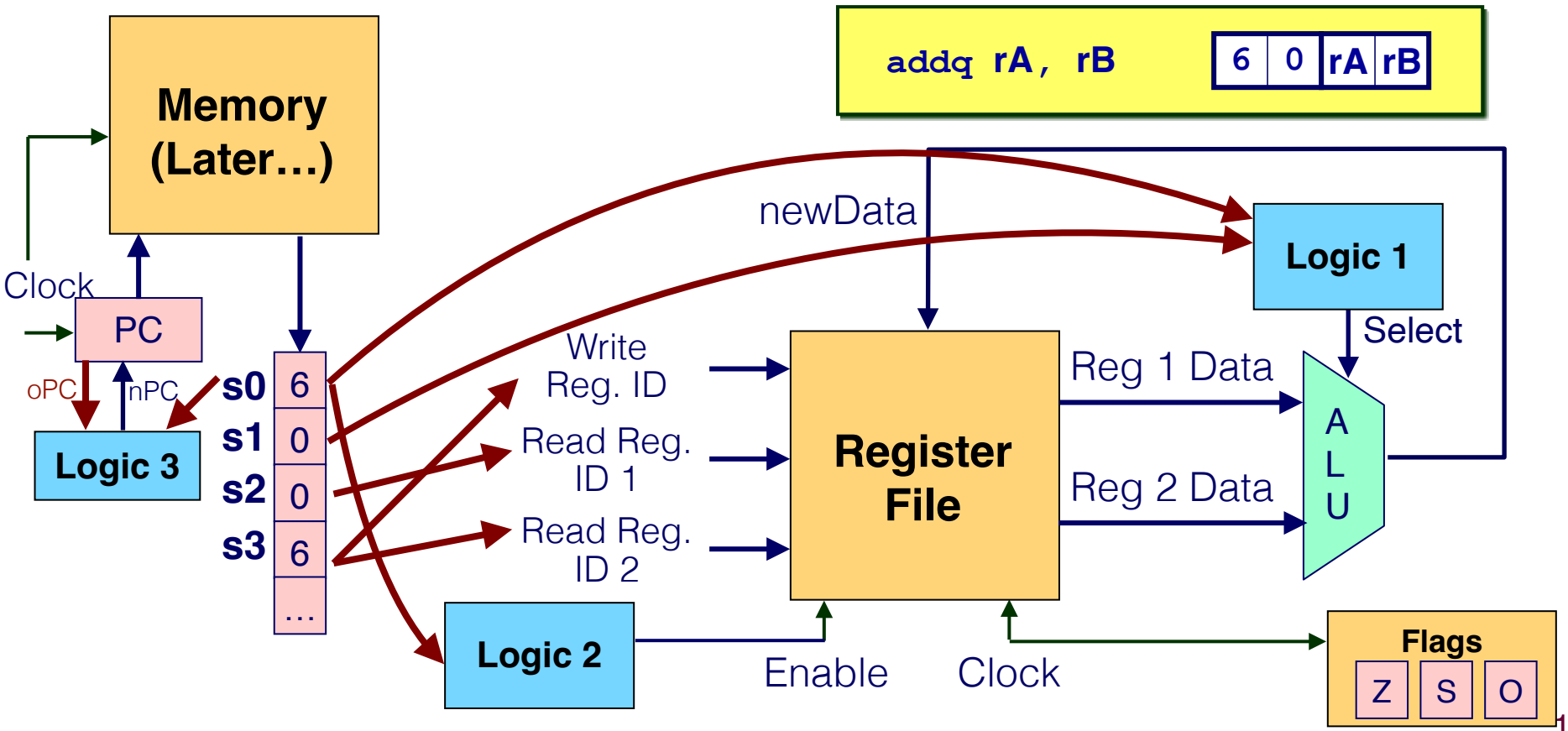


Executing an ADD instruction

- Logic 1: if (s0 == 6) select = s1;
- Logic 2: if (s0 == 6) Enable = 1; else Enable = 0;
- Logic 3: if (s0 == 6) nPC = oPC + 2;



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- Logic 1: if (s0 == 6) select = s1;
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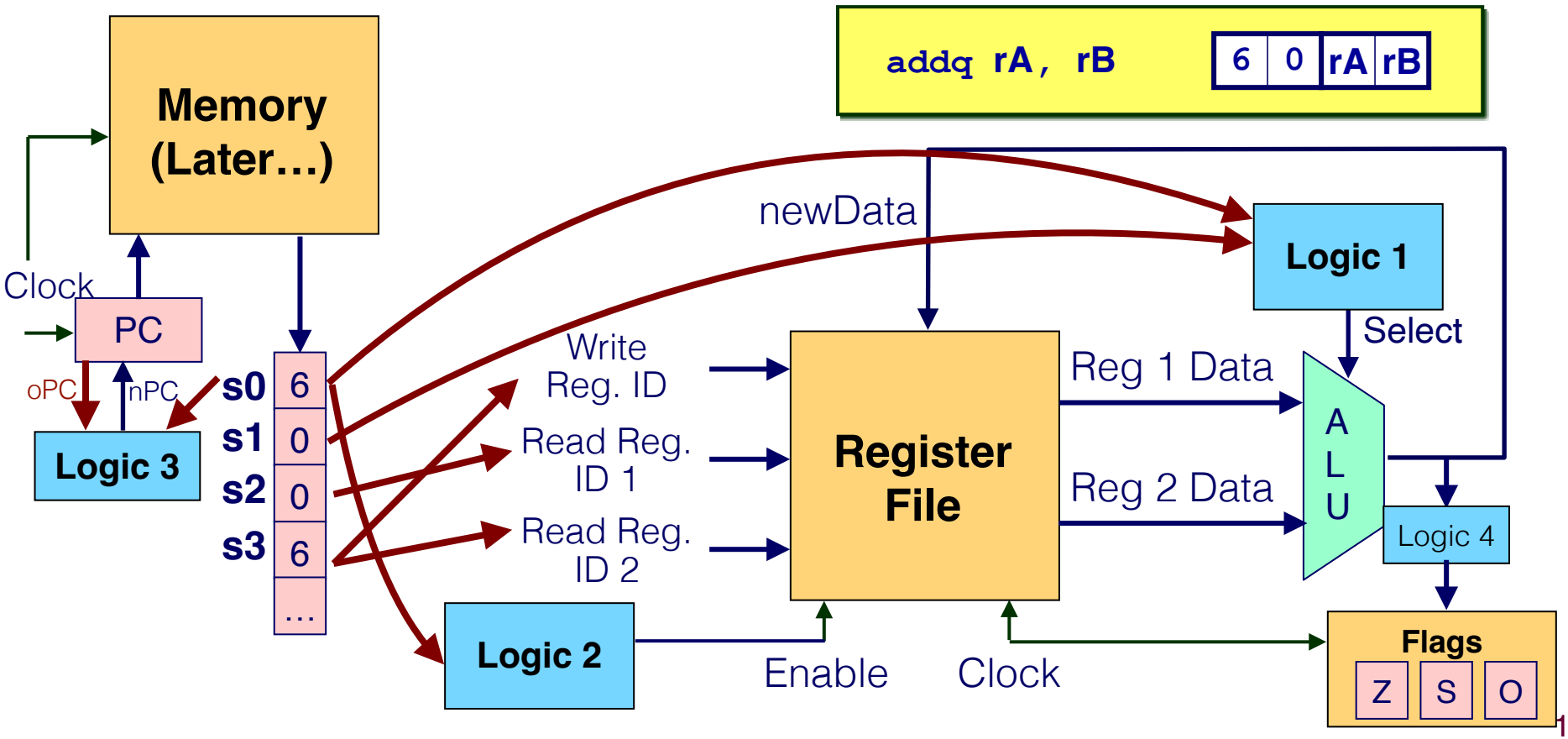
- How about Logic 4?



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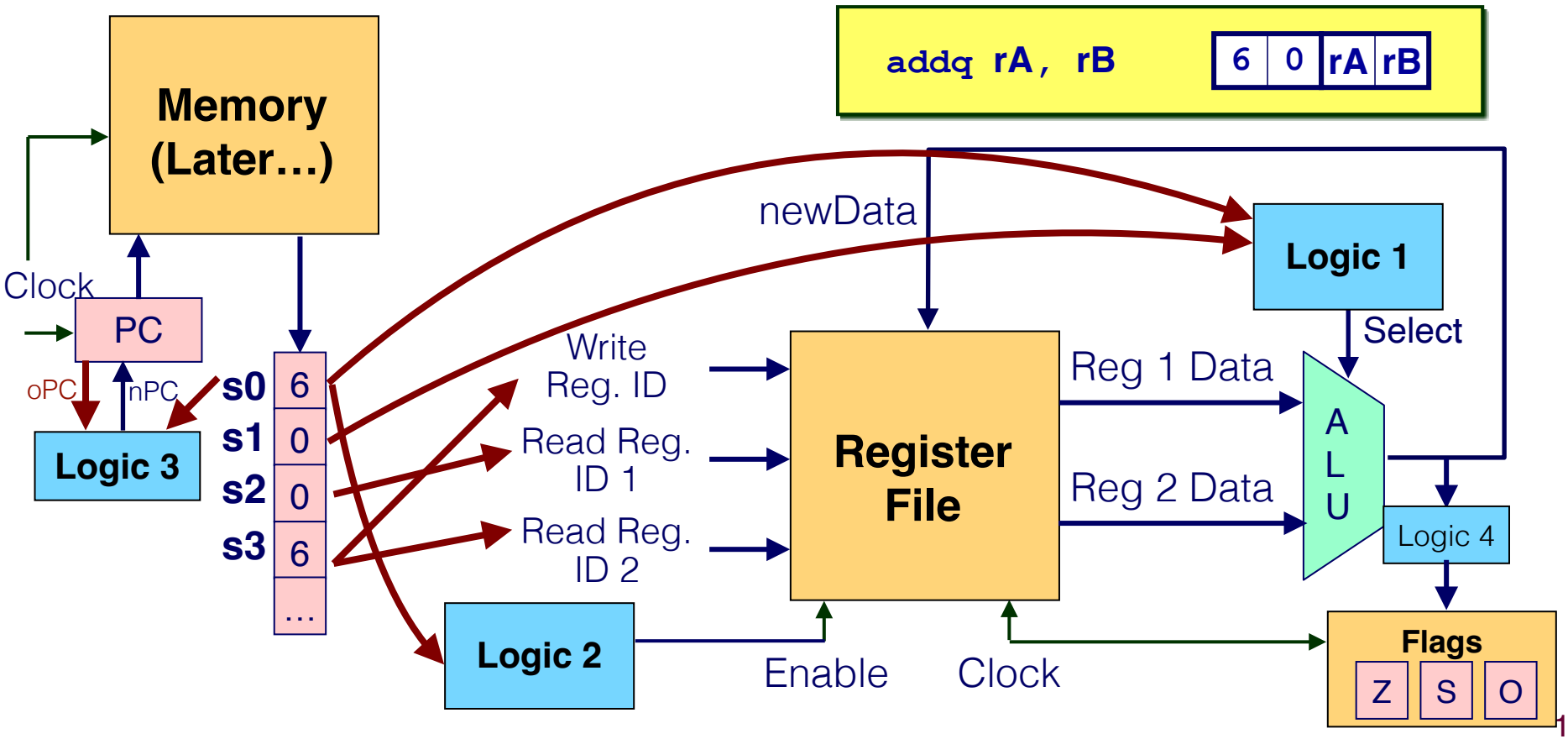
- How about Logic 4?

How do these logics get implemented?



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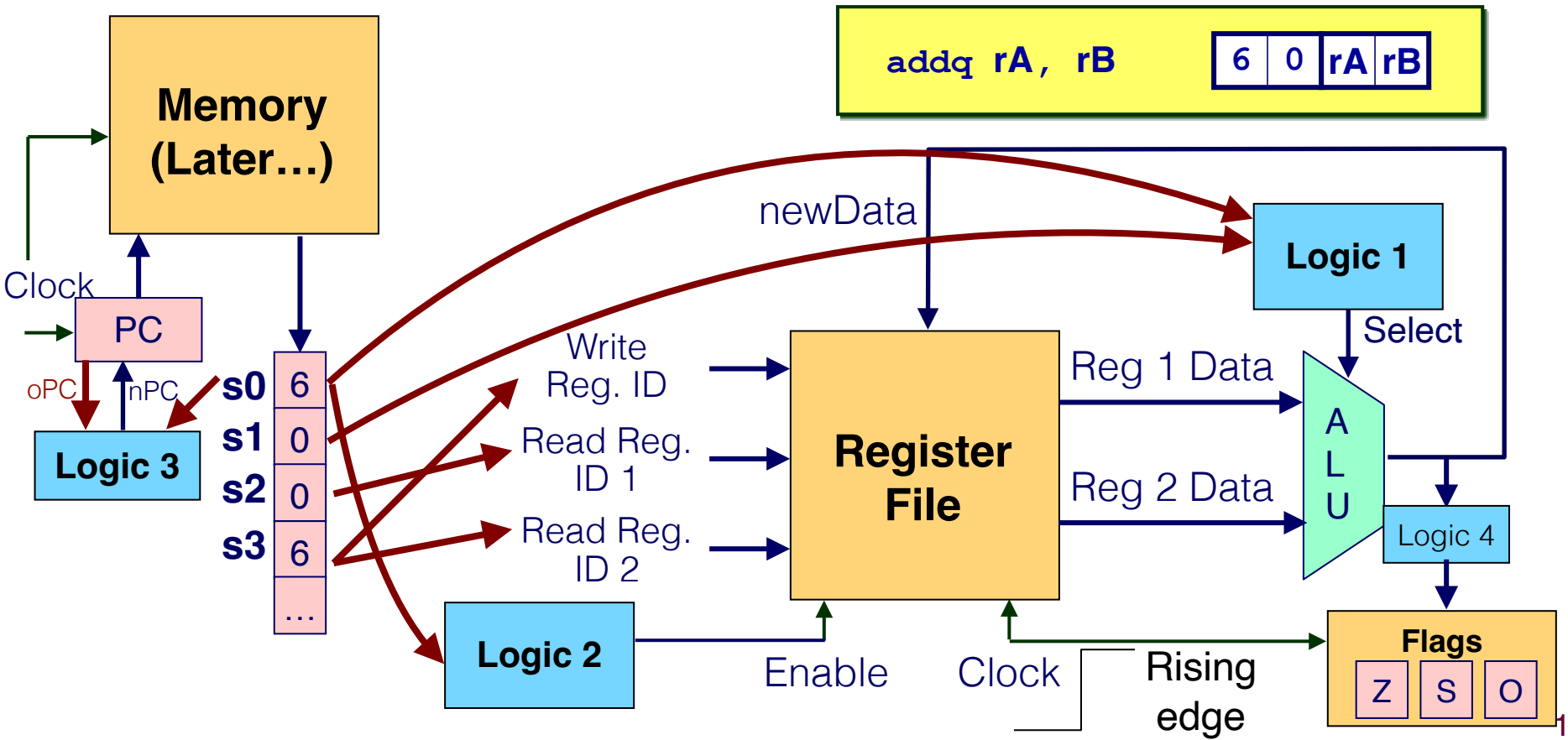
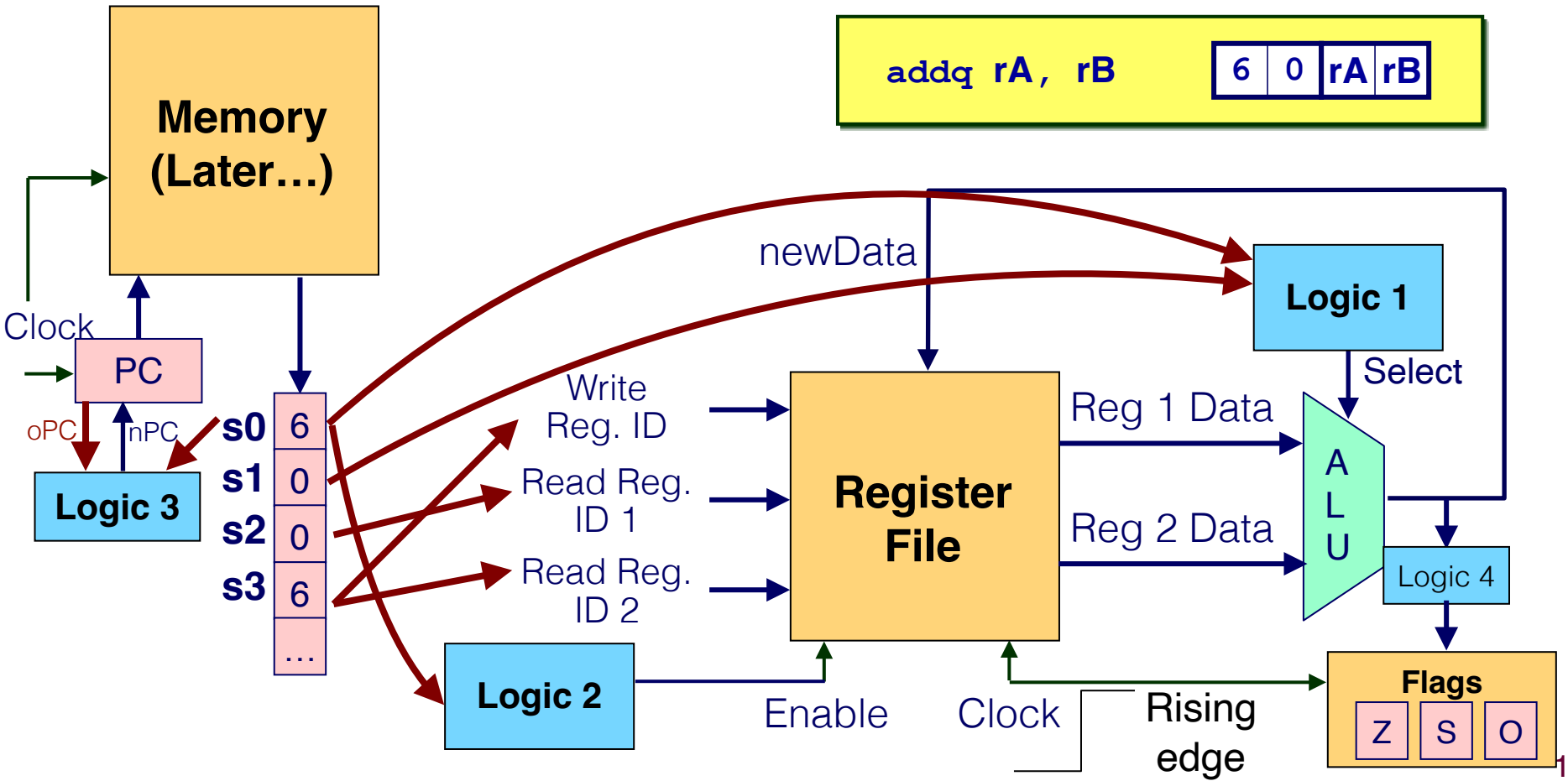
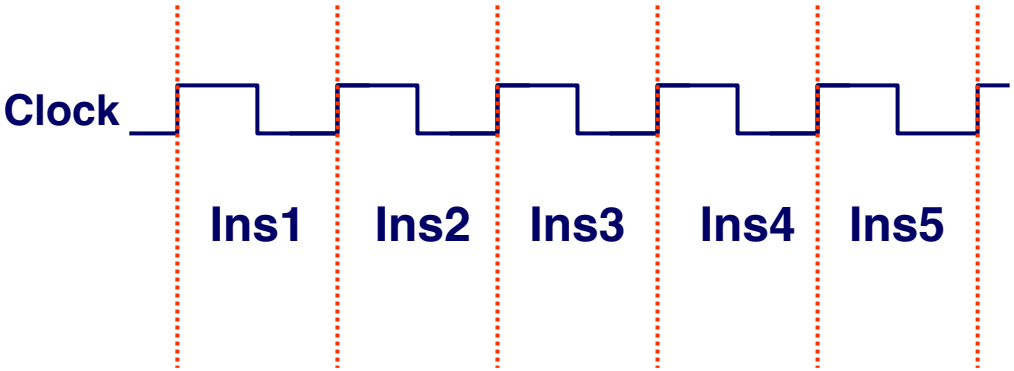


Executing an ADD instruction

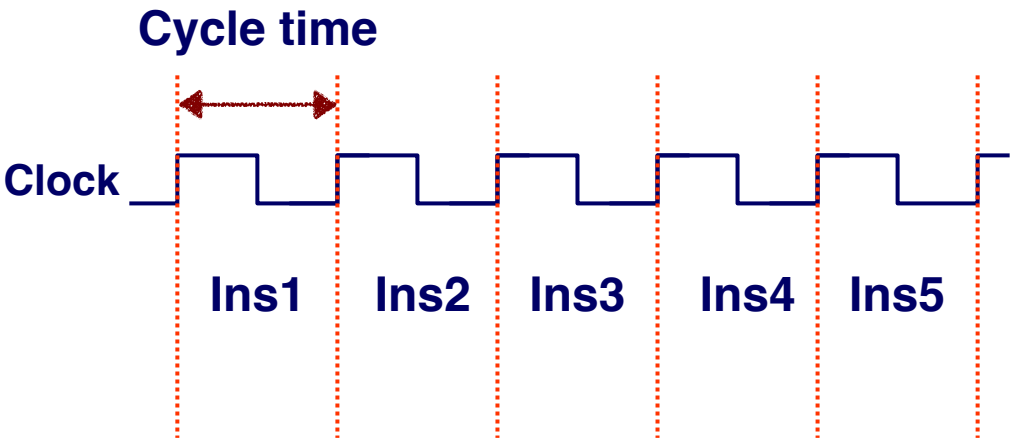
- When the rising edge of the clock arrives, the RF/PC/Flags will be written.
- So the following has to be ready: newData, nPC, which means Logic1, Logic2, Logic3, and Logic4 has to finish.



Executing many ADD instructions

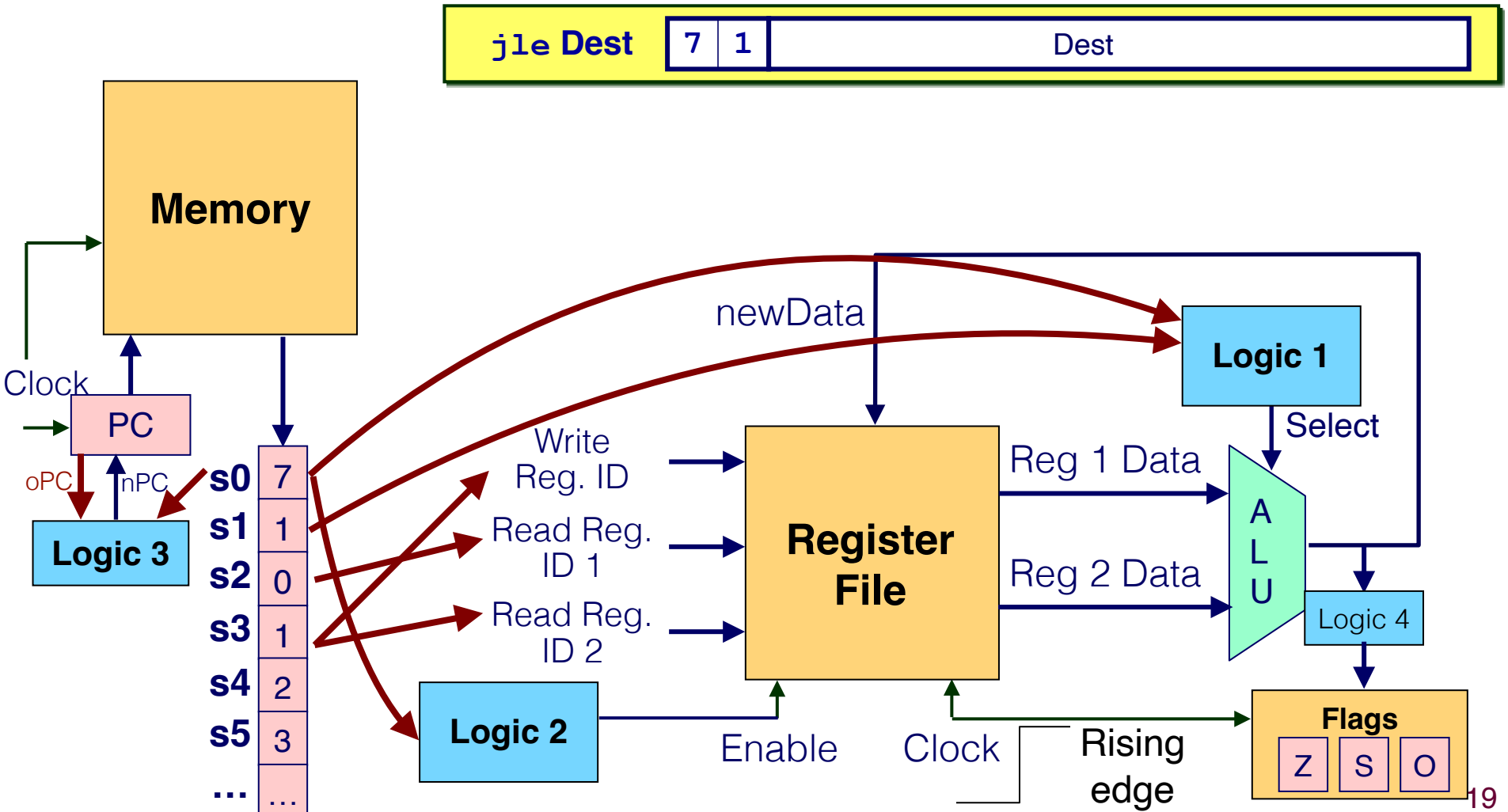


Executing many ADD instructions

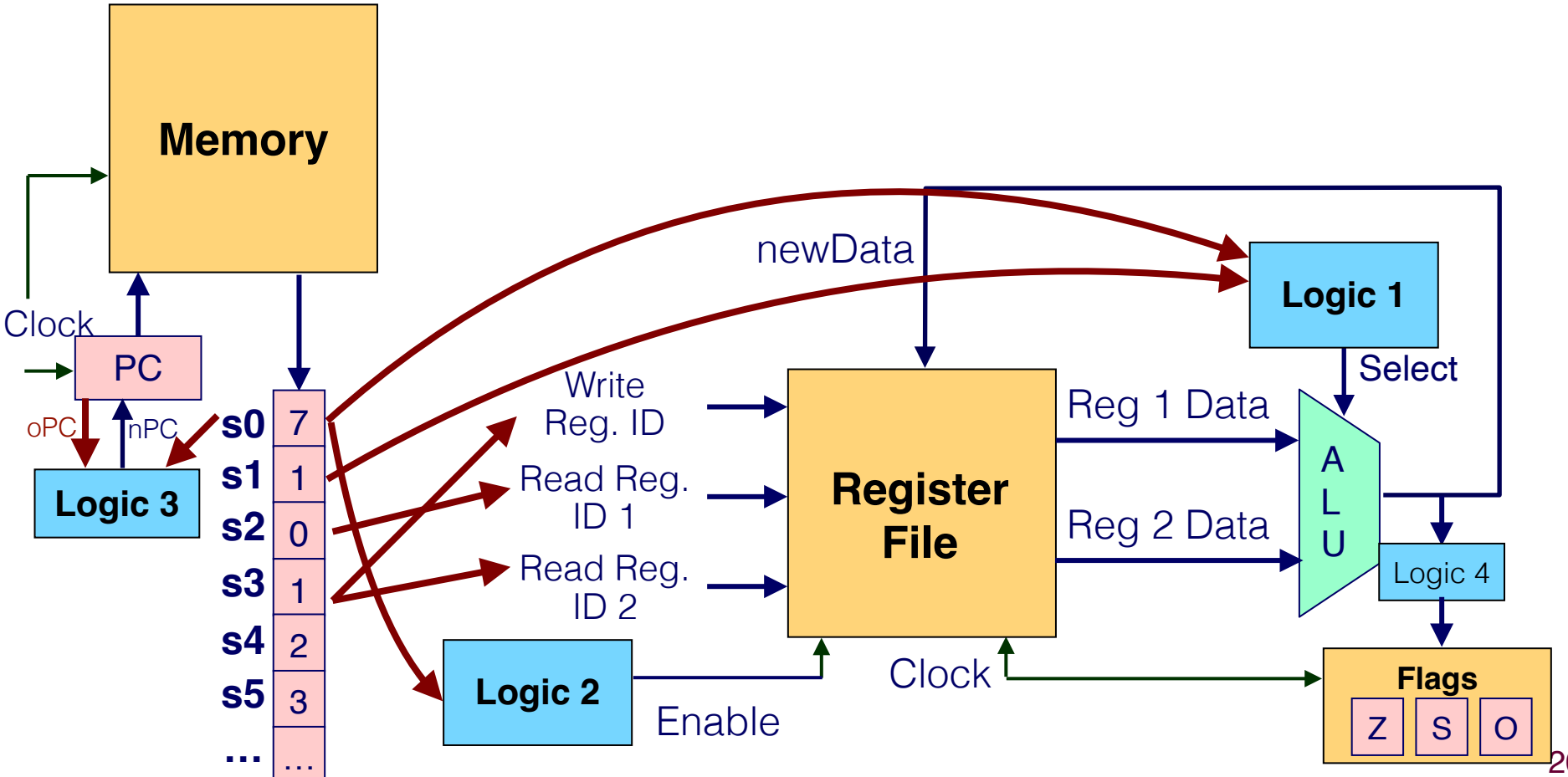


Executing a JLE instruction

- Let's say the binary encoding for `jle .L0` is `71 0123000000000000`
- What are the logics now?

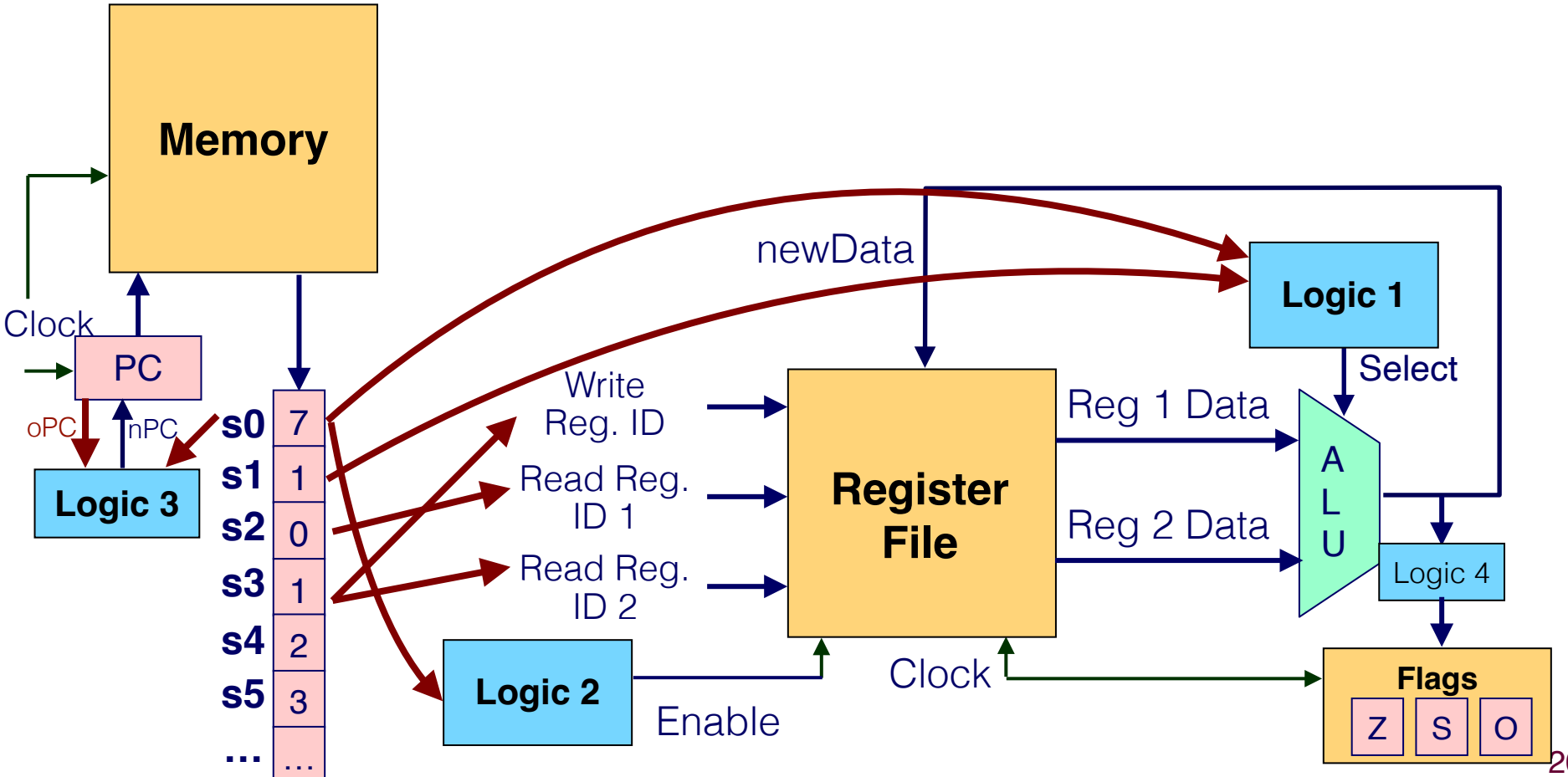


Executing a JLE instruction



Executing a JLE instruction

- Logic 1: if (s0 == 6) select = s1;



Executing a JLE instruction

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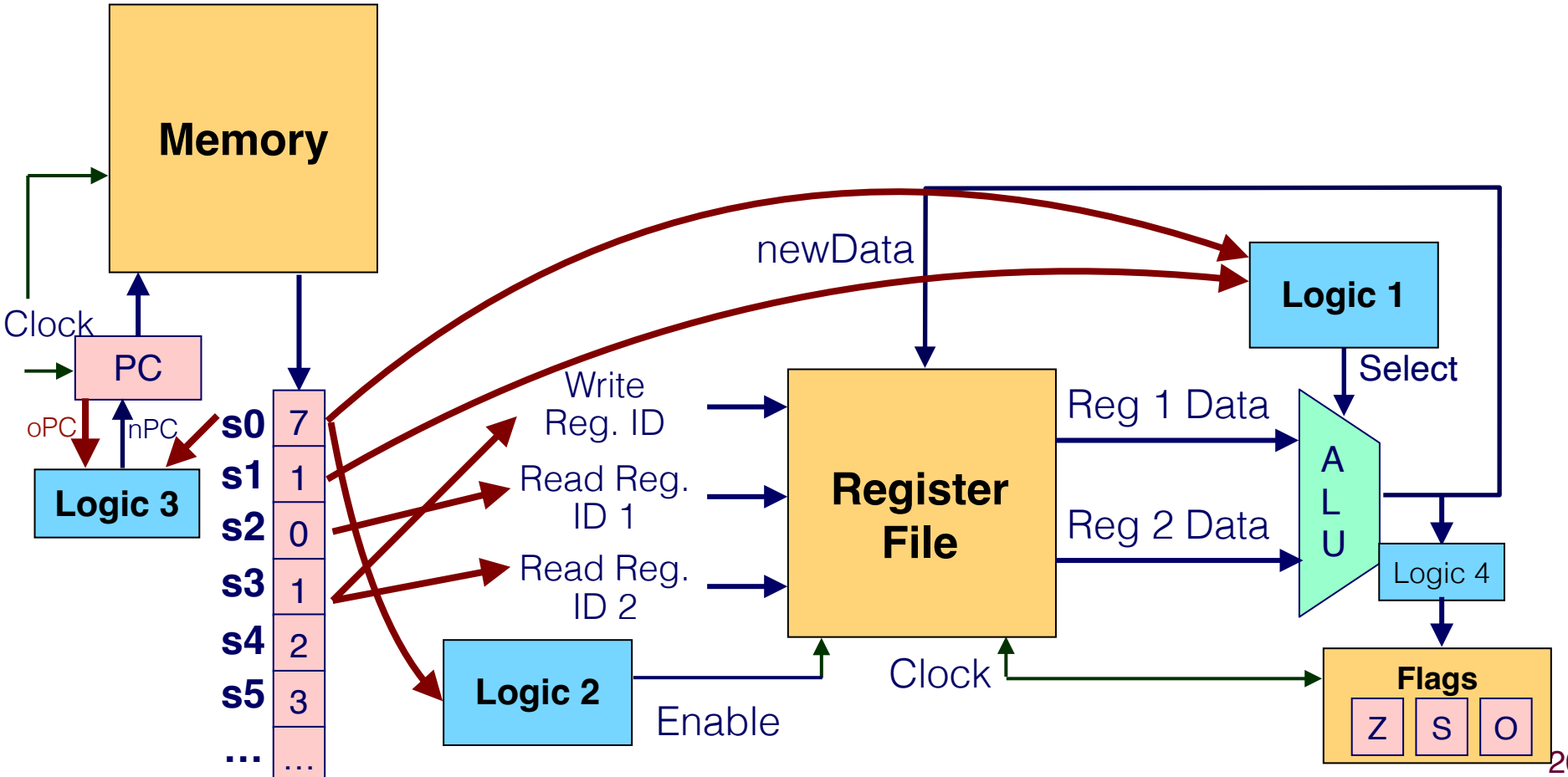
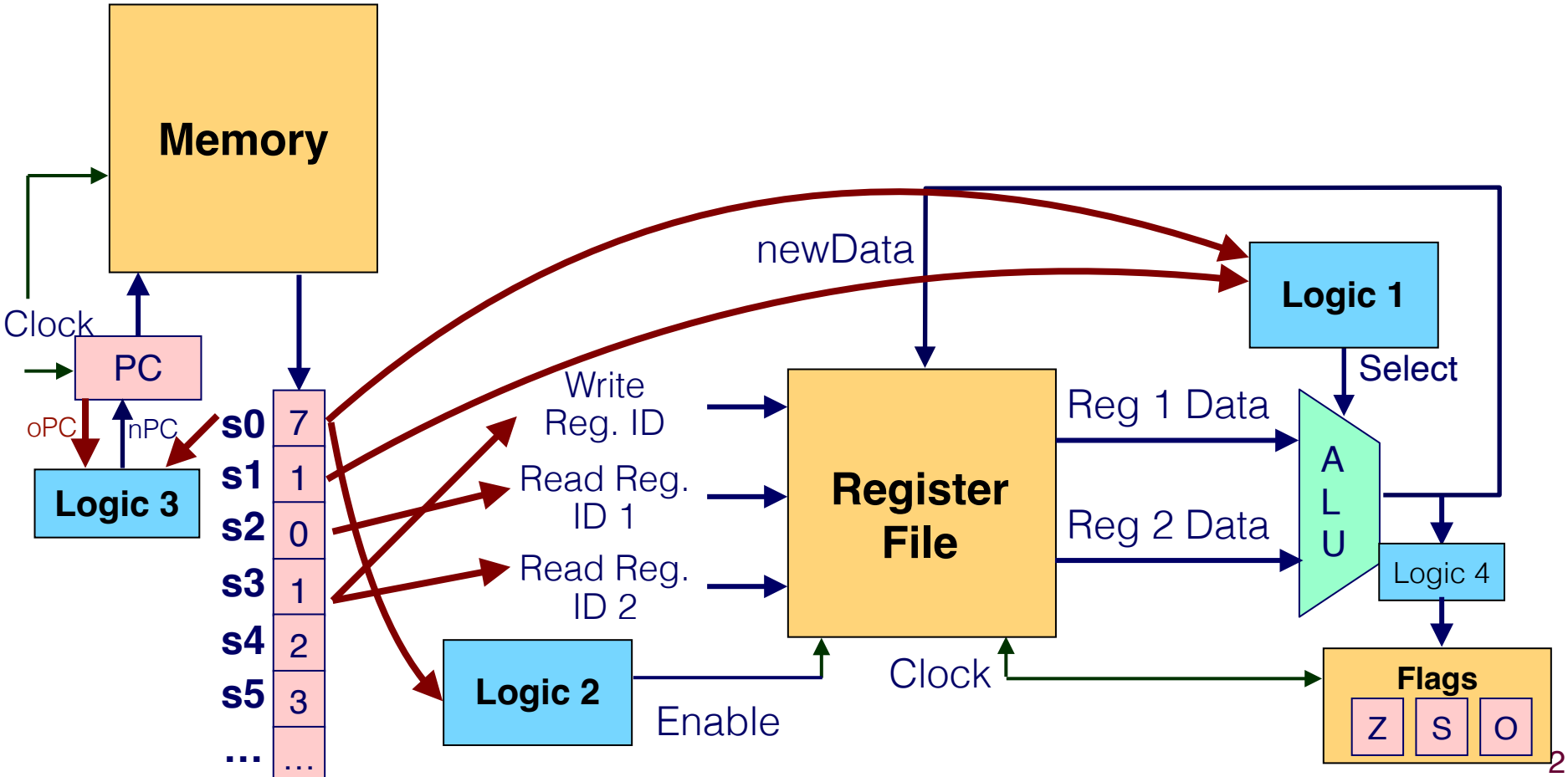
- Logic 2: if (s0 == 6) Enable = 1; else Enable = 0;



`jle` **Dest**	7	1	Dest

Executing a JLE instruction

- Logic 3??

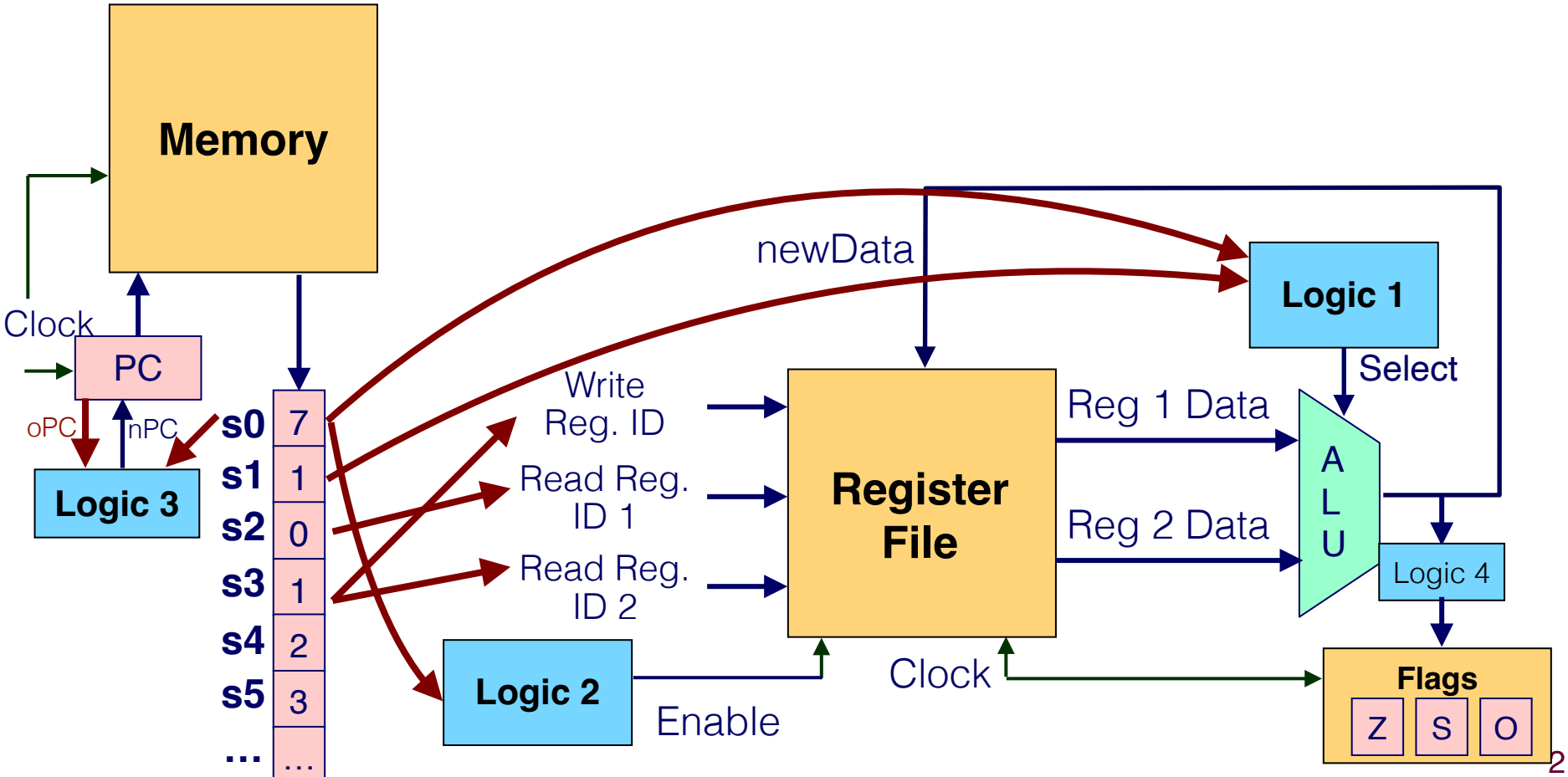


jle Dest	7	1	Dest

Executing a JLE instruction

- Logic 3??

if (s0 == 6) nPC = oPC + 2;

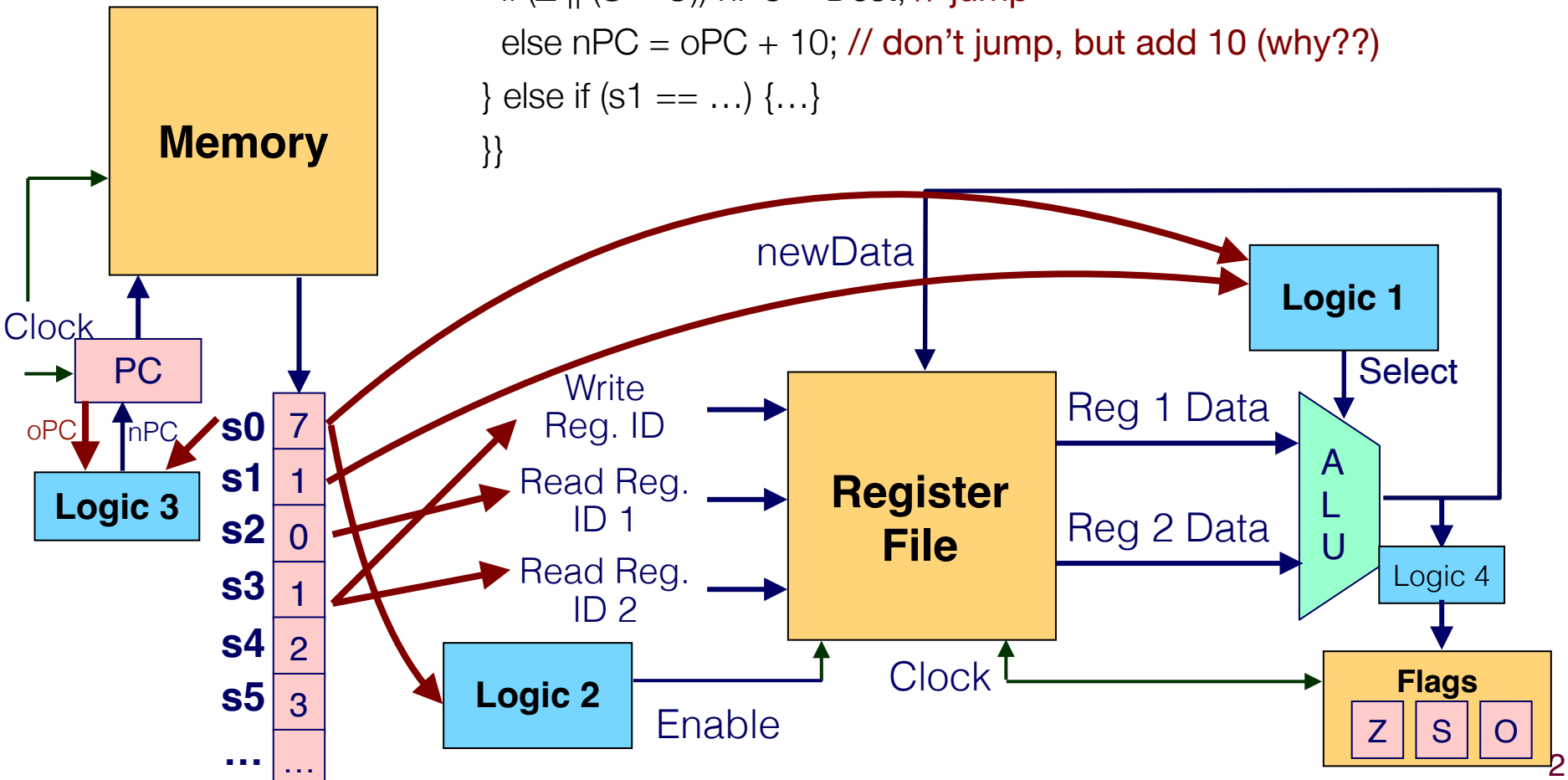


jle Dest	7	1	Dest

Executing a JLE instruction

- Logic 3??

```
if (s0 == 6) nPC = oPC + 2;
else if (s0 == 7) {
  if (s1 == 1) { // jLE
    if (Z || (S ^ O)) nPC = Dest; // jump
    else nPC = oPC + 10; // don't jump, but add 10 (why??)
  } else if (s1 == …) {…}
  }}
```



jle Dest	7	1	Dest

Executing a JLE instruction

- Logic 3??

```
if (s0 == 6) nPC = oPC + 2;
else if (s0 == 7) {
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    if (Z || (S ^ O)) nPC = Dest; // jump
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  } else if (s1 == …) {…}
 }}
```
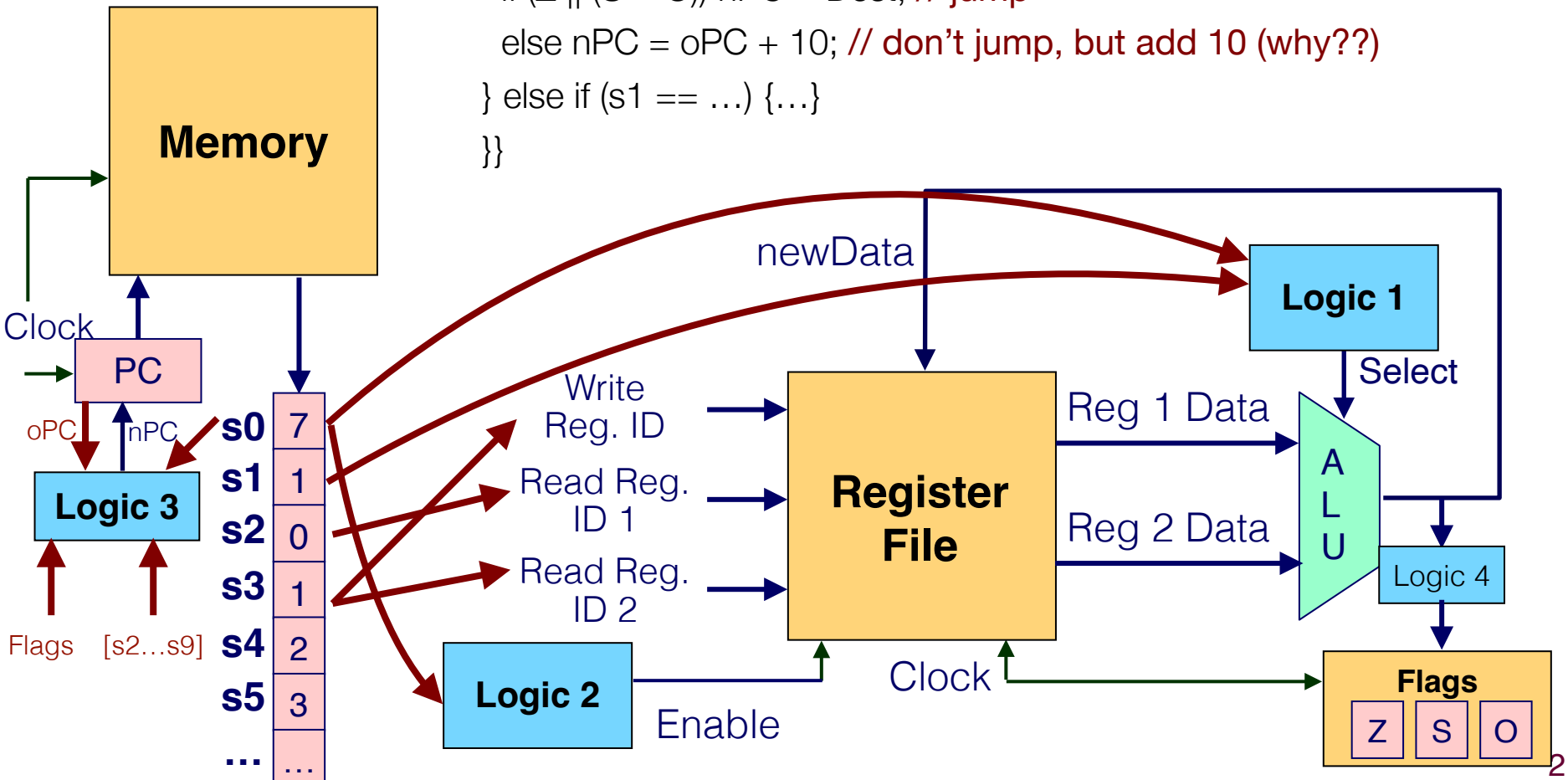
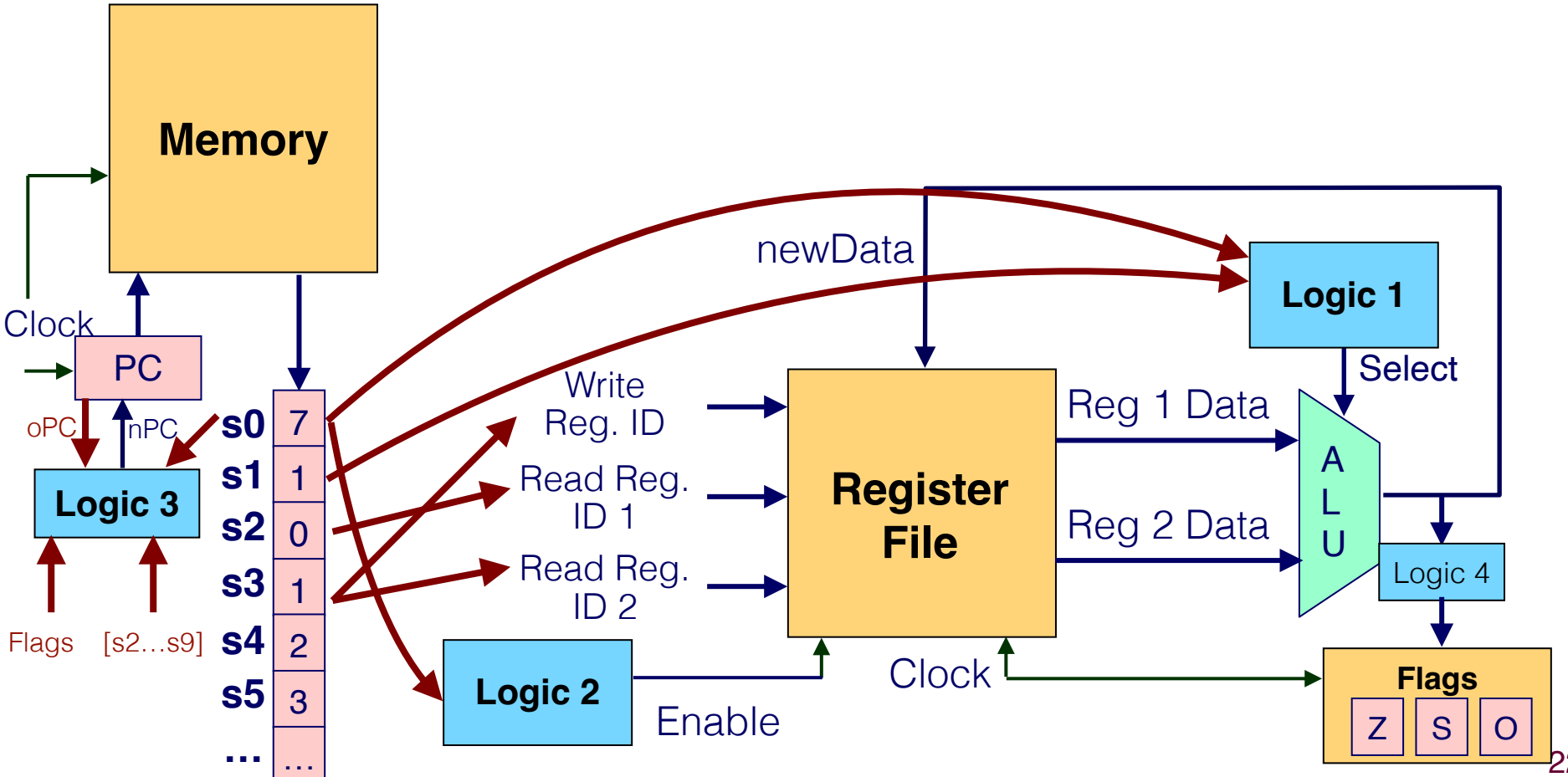



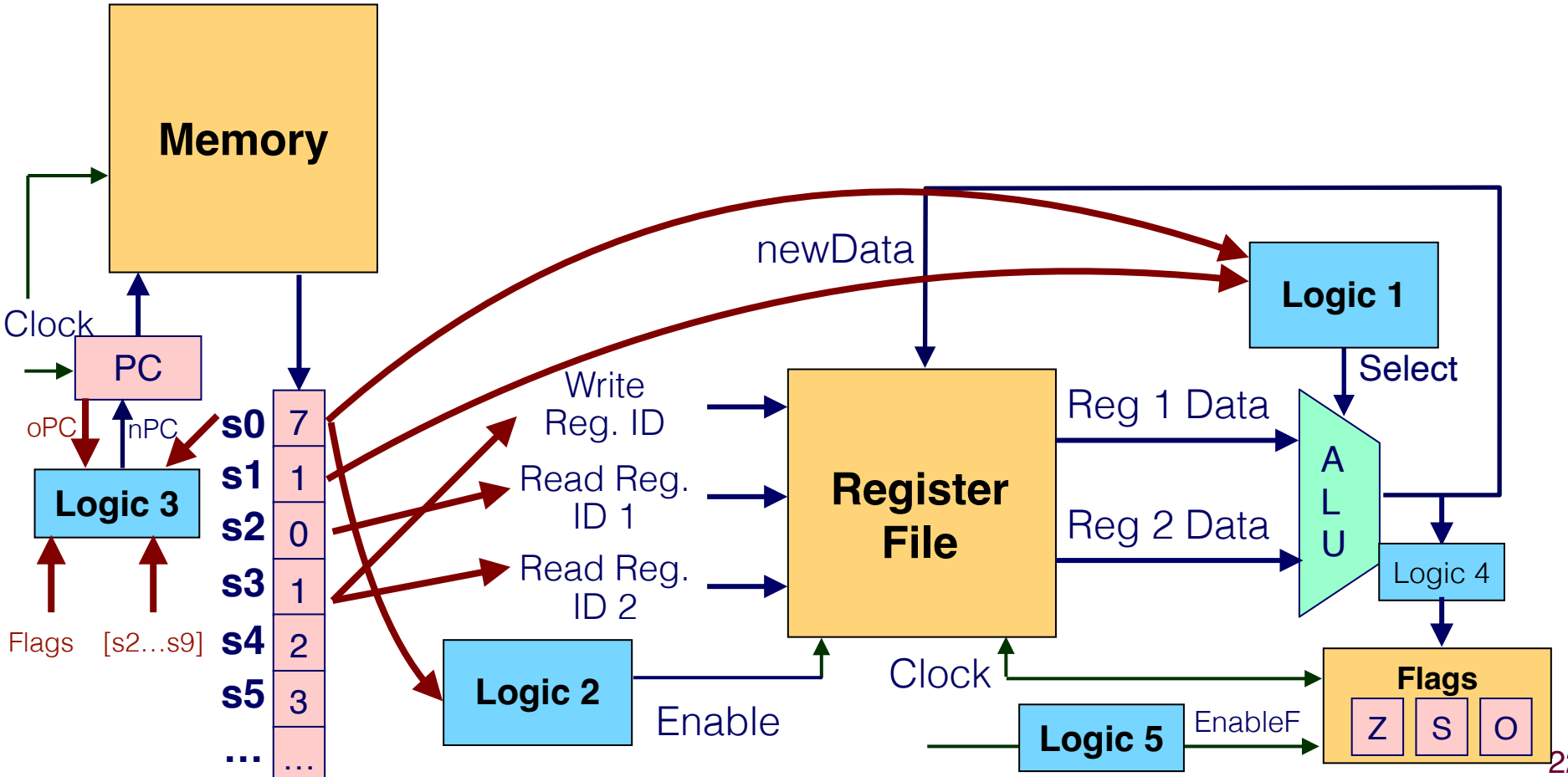
Executing a JLE instruction

- Logic 4? Does JLE write flags?



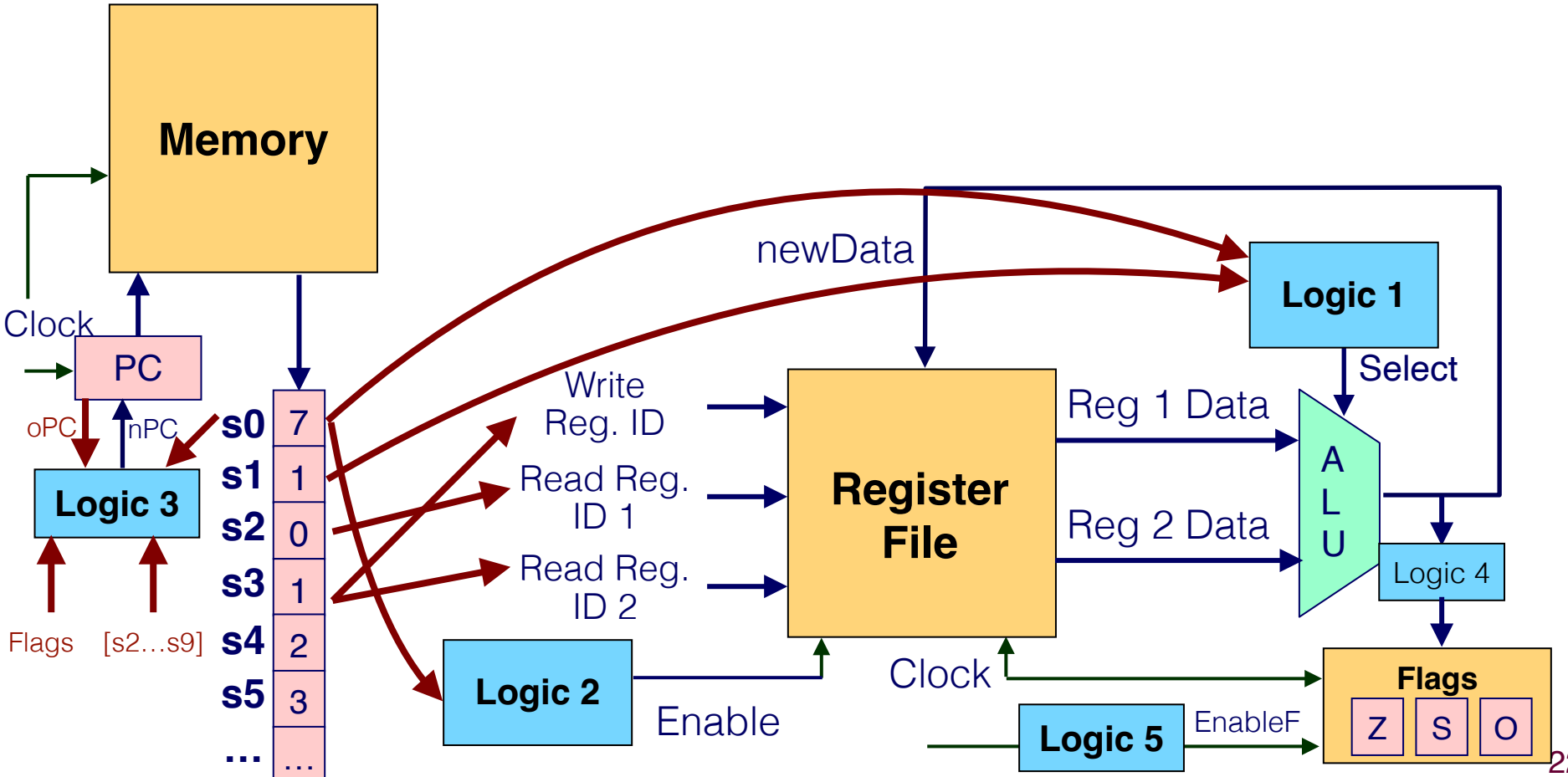
Executing a JLE instruction

- Logic 4? Does JLE write flags?
- Need another piece of logic.

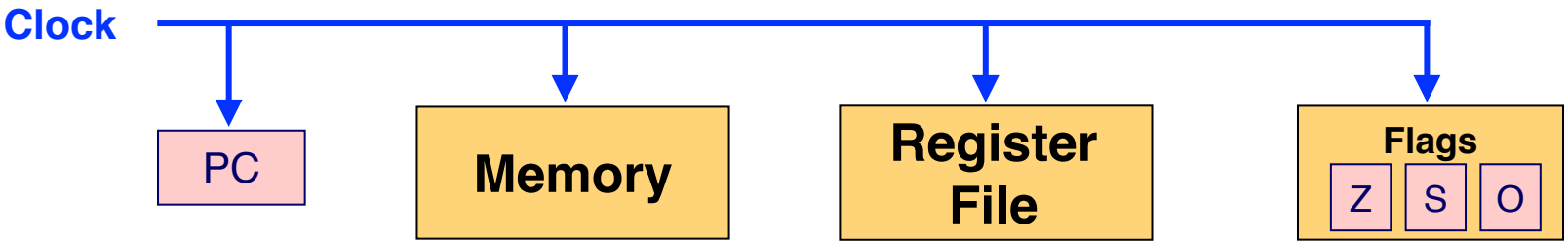


Executing a JLE instruction

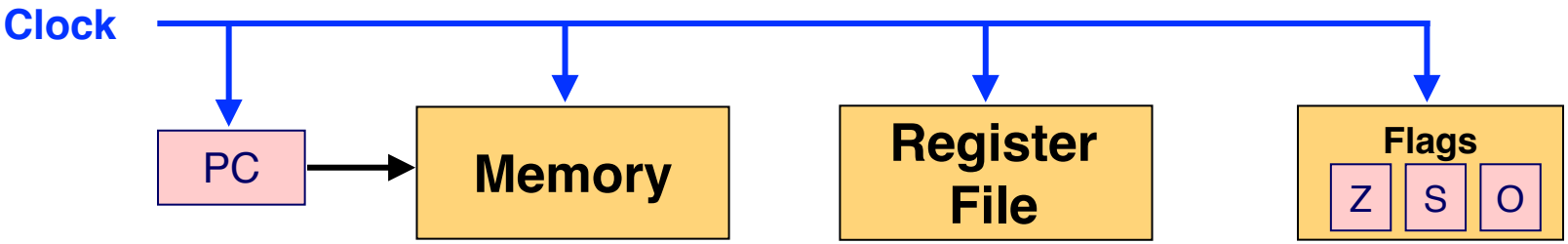
- Logic 4? Does JLE write flags?
- Need another piece of logic.
- Logic 5: if (s0 == 7) EnableF = 0; else if (s0 == 6) EnableF = 1;



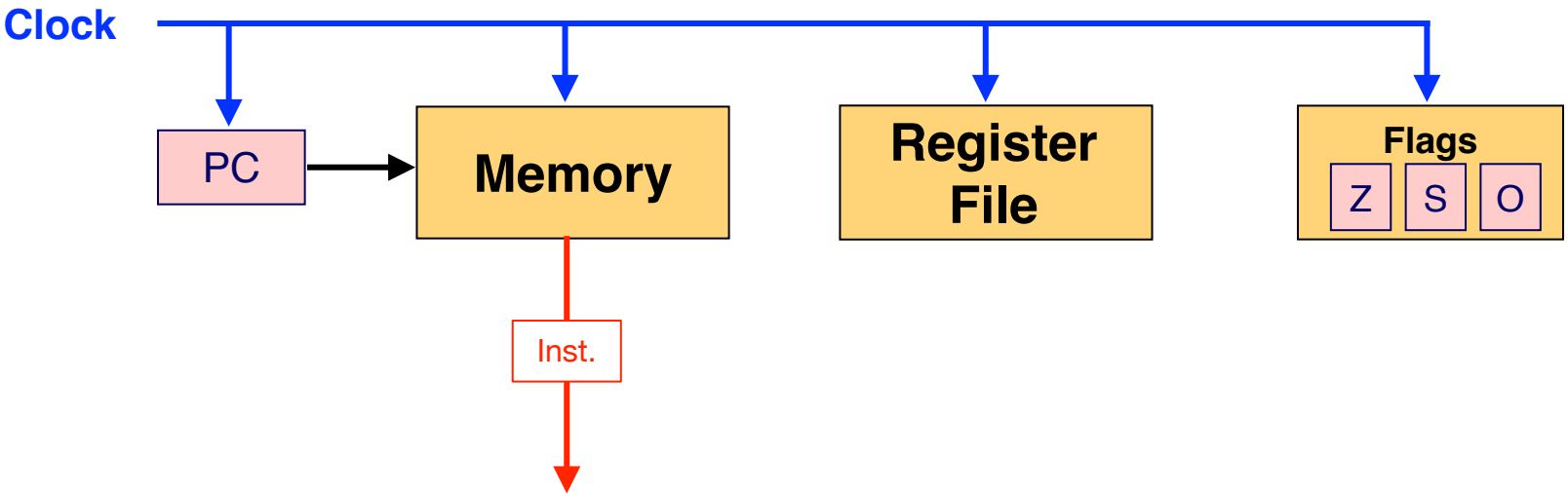
Microarchitecture (So far)



Microarchitecture (So far)



Microarchitecture (So far)



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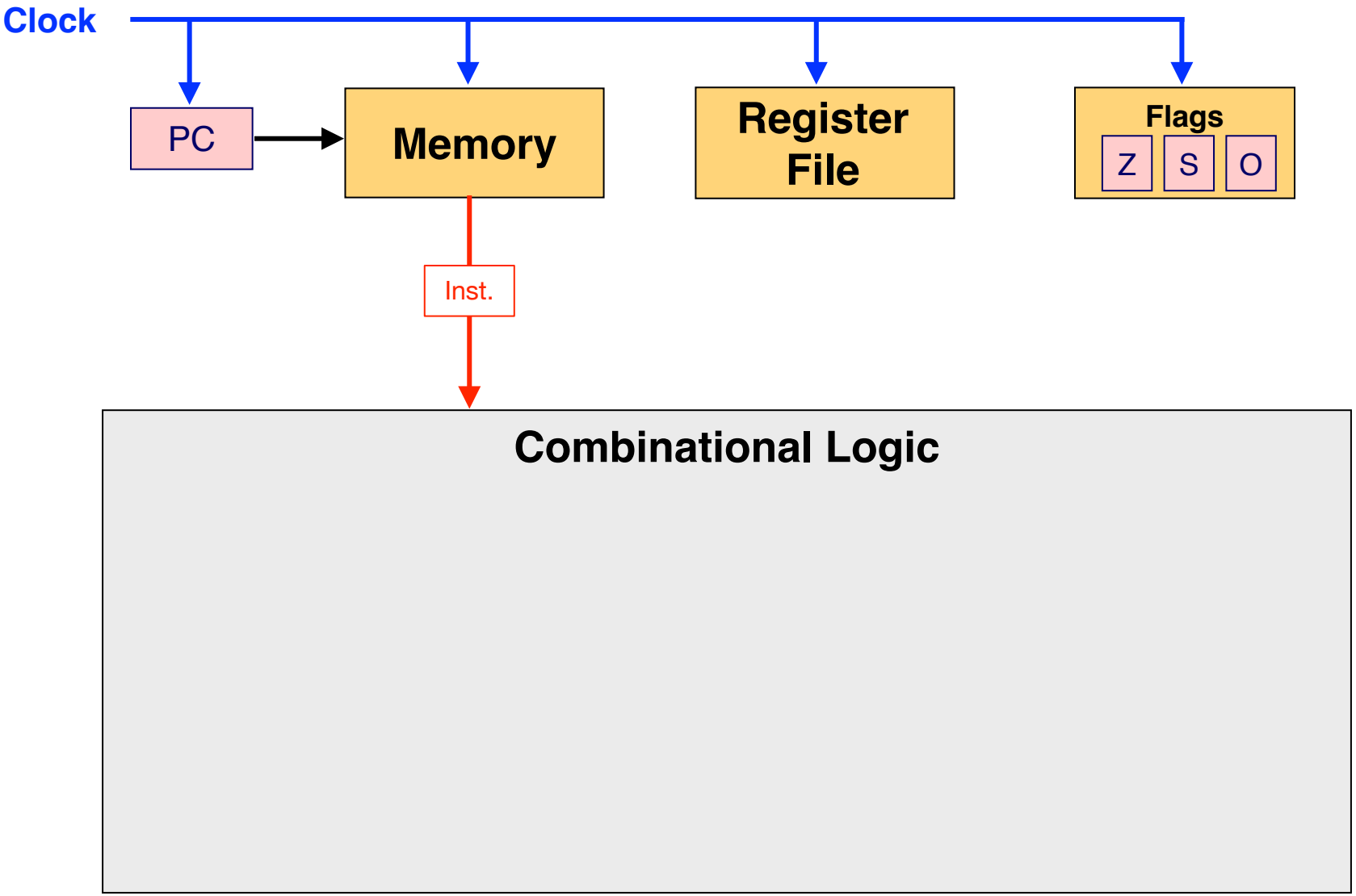

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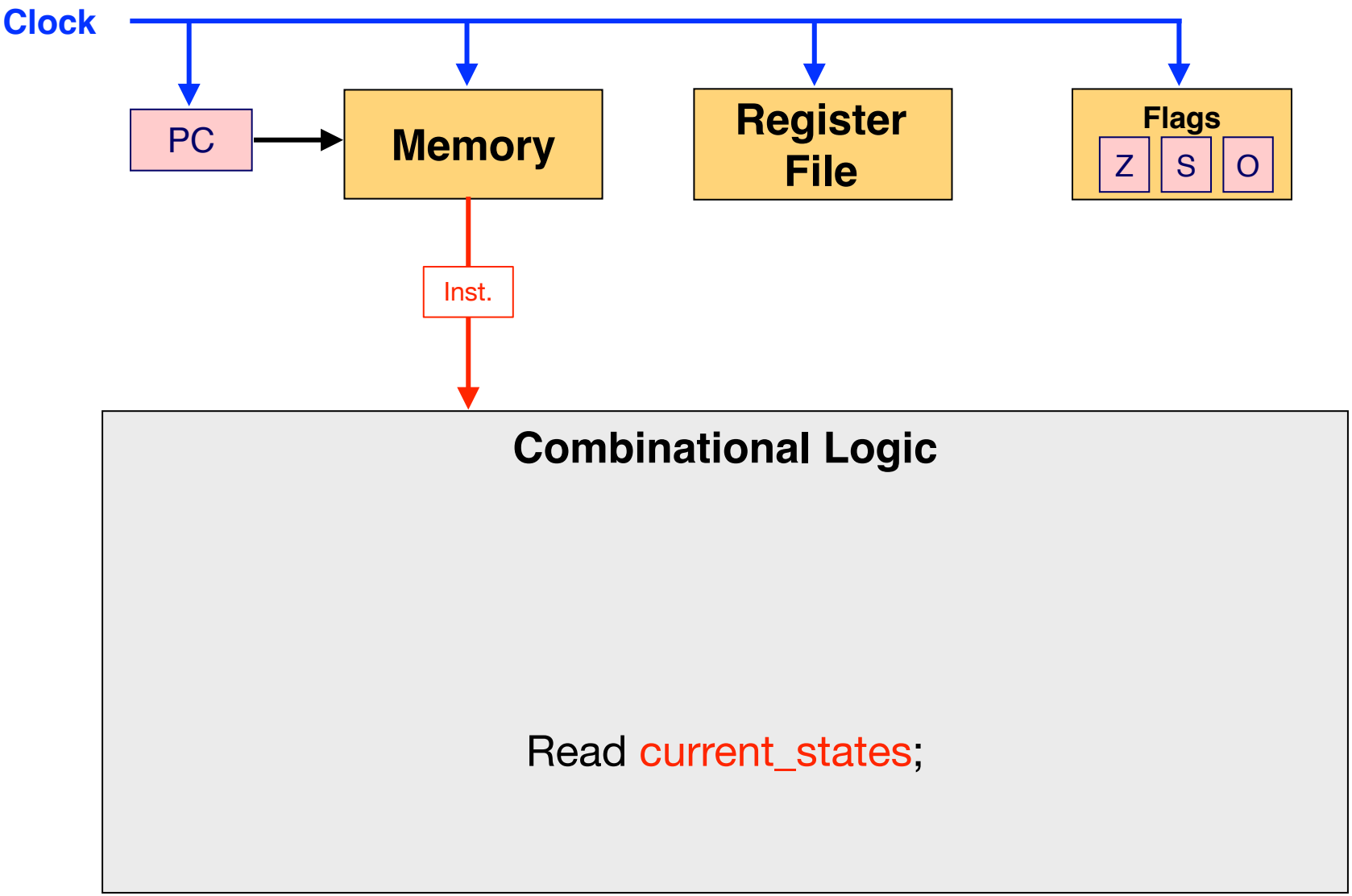

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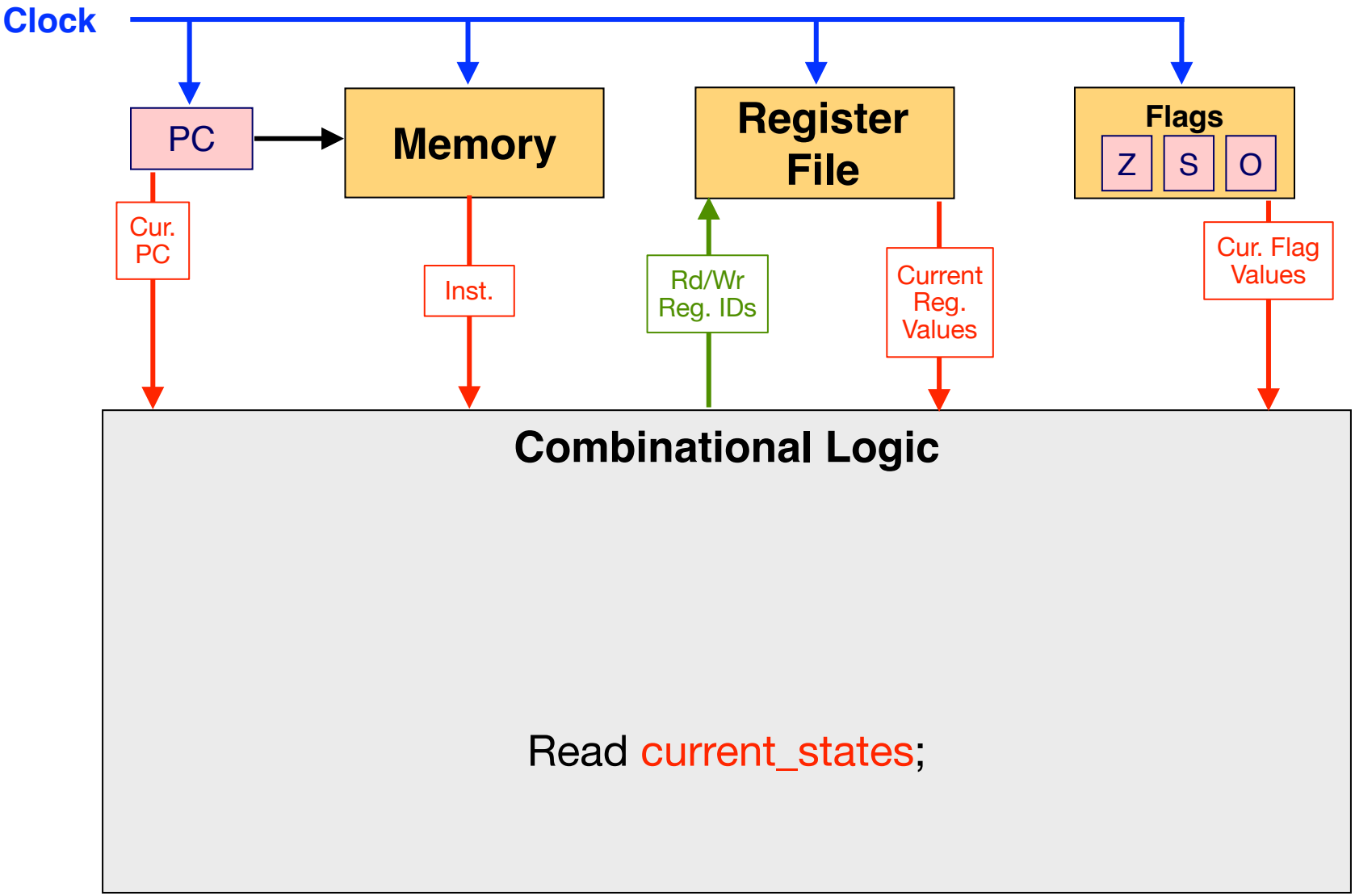
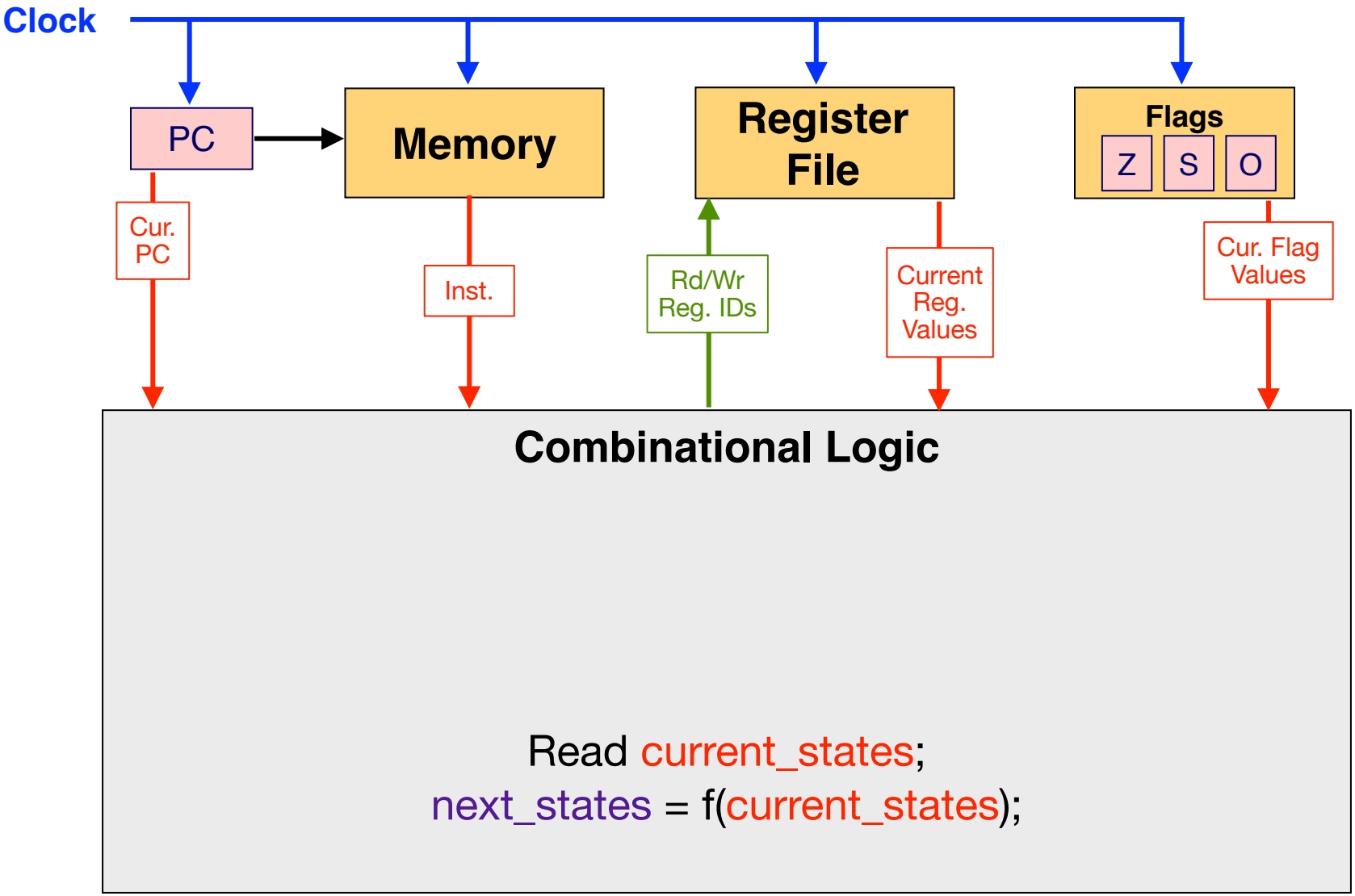
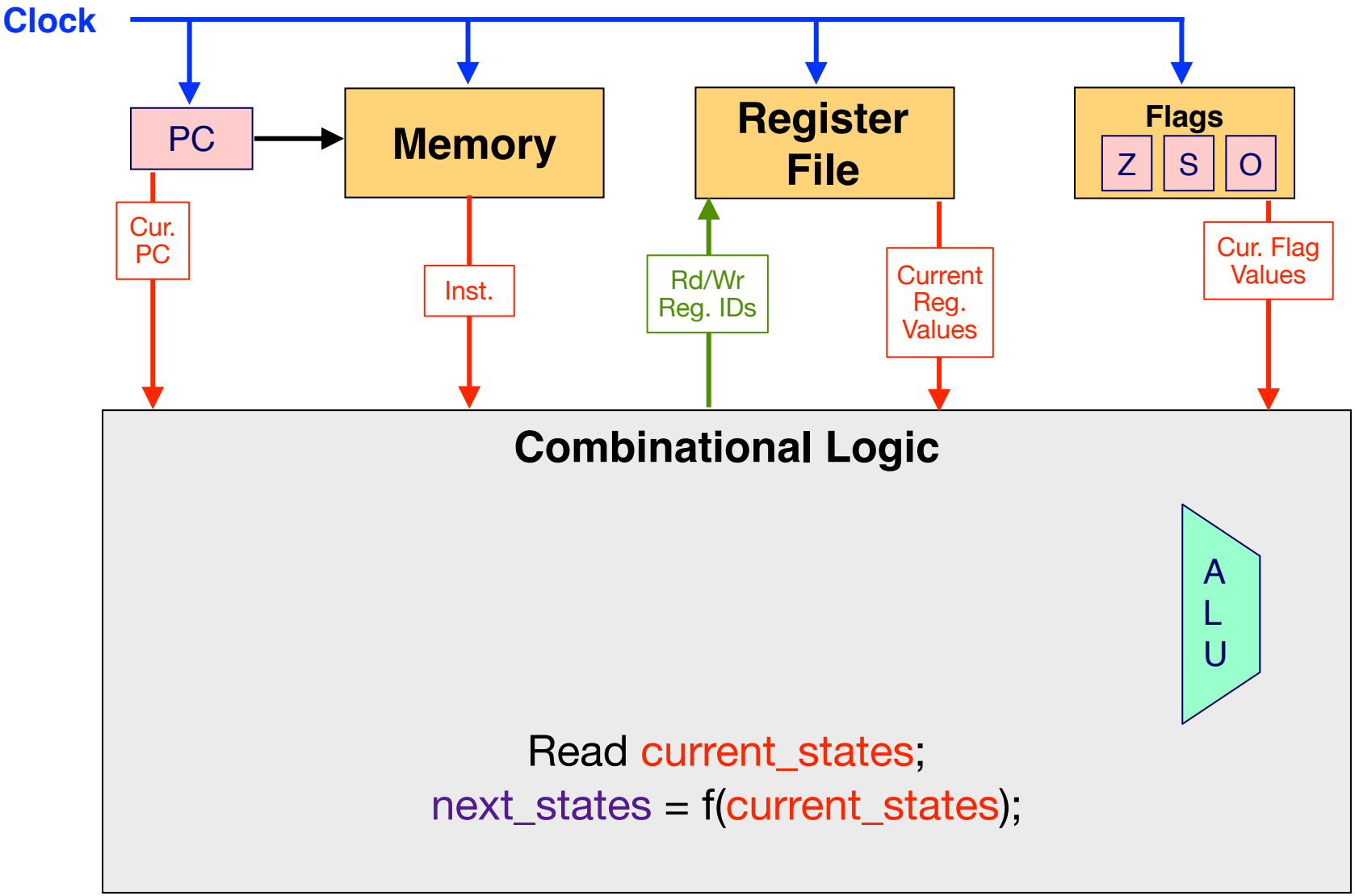


Microarchitecture (So far)



Microarchitecture (So far)



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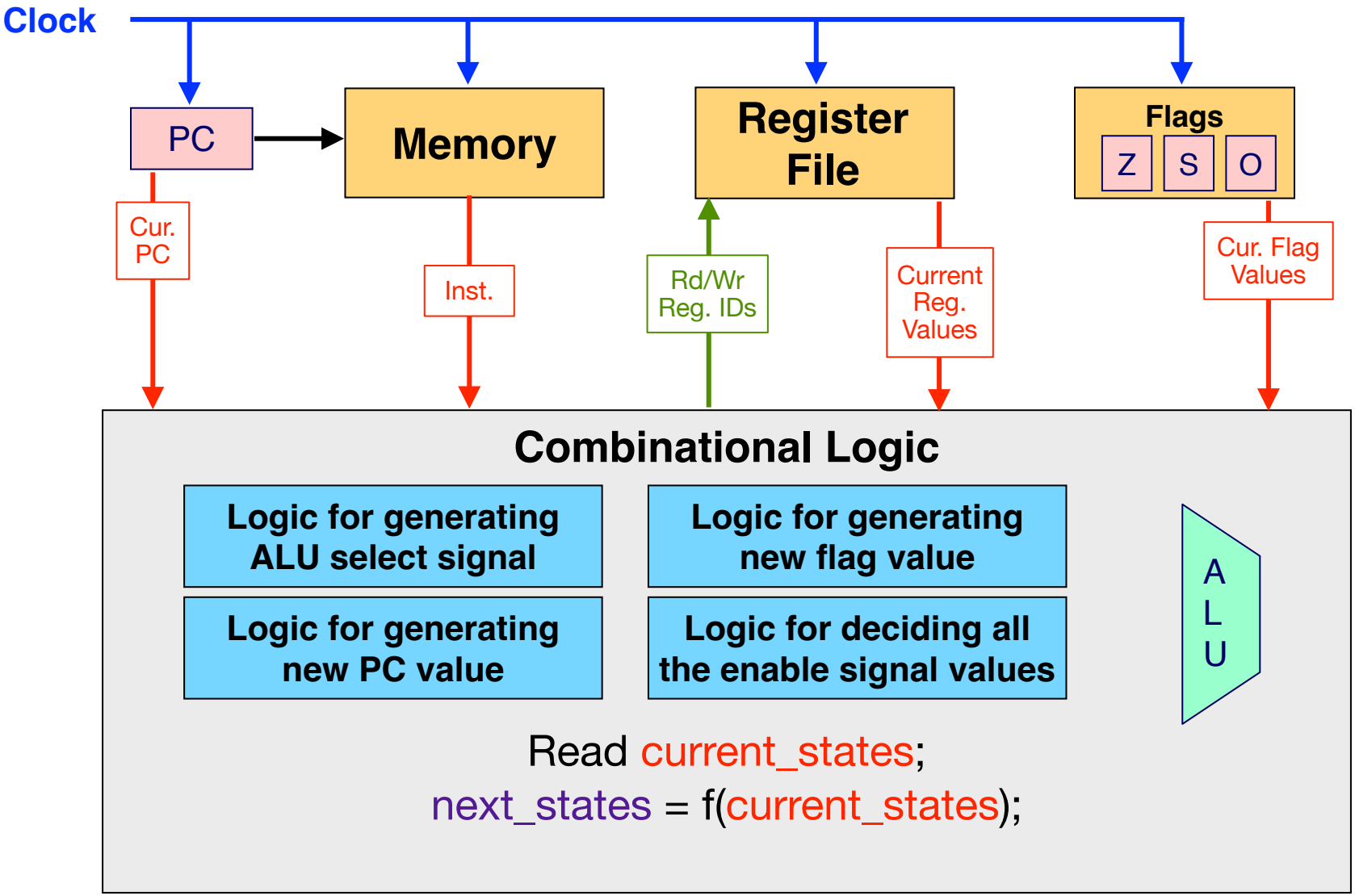

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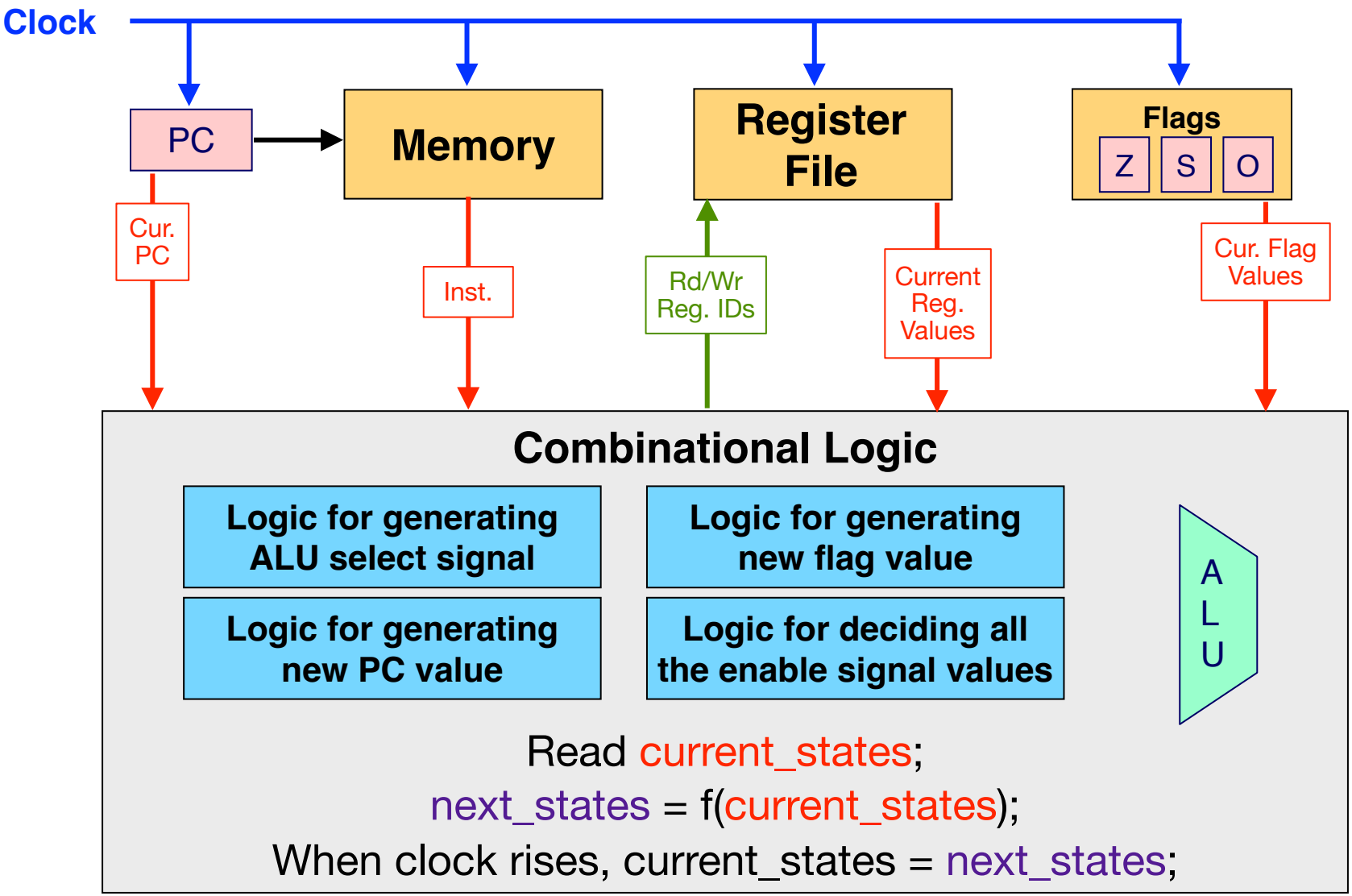

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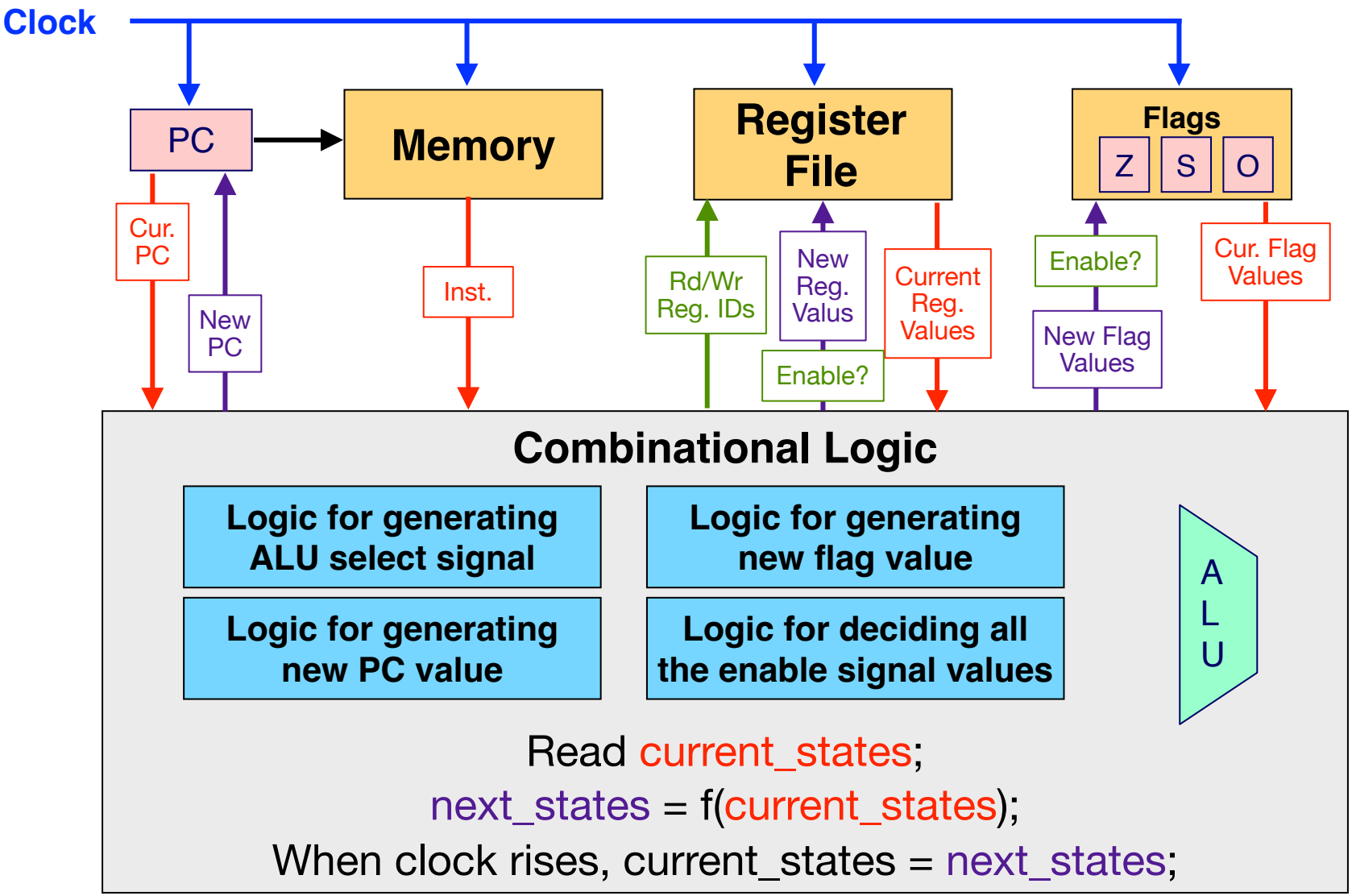
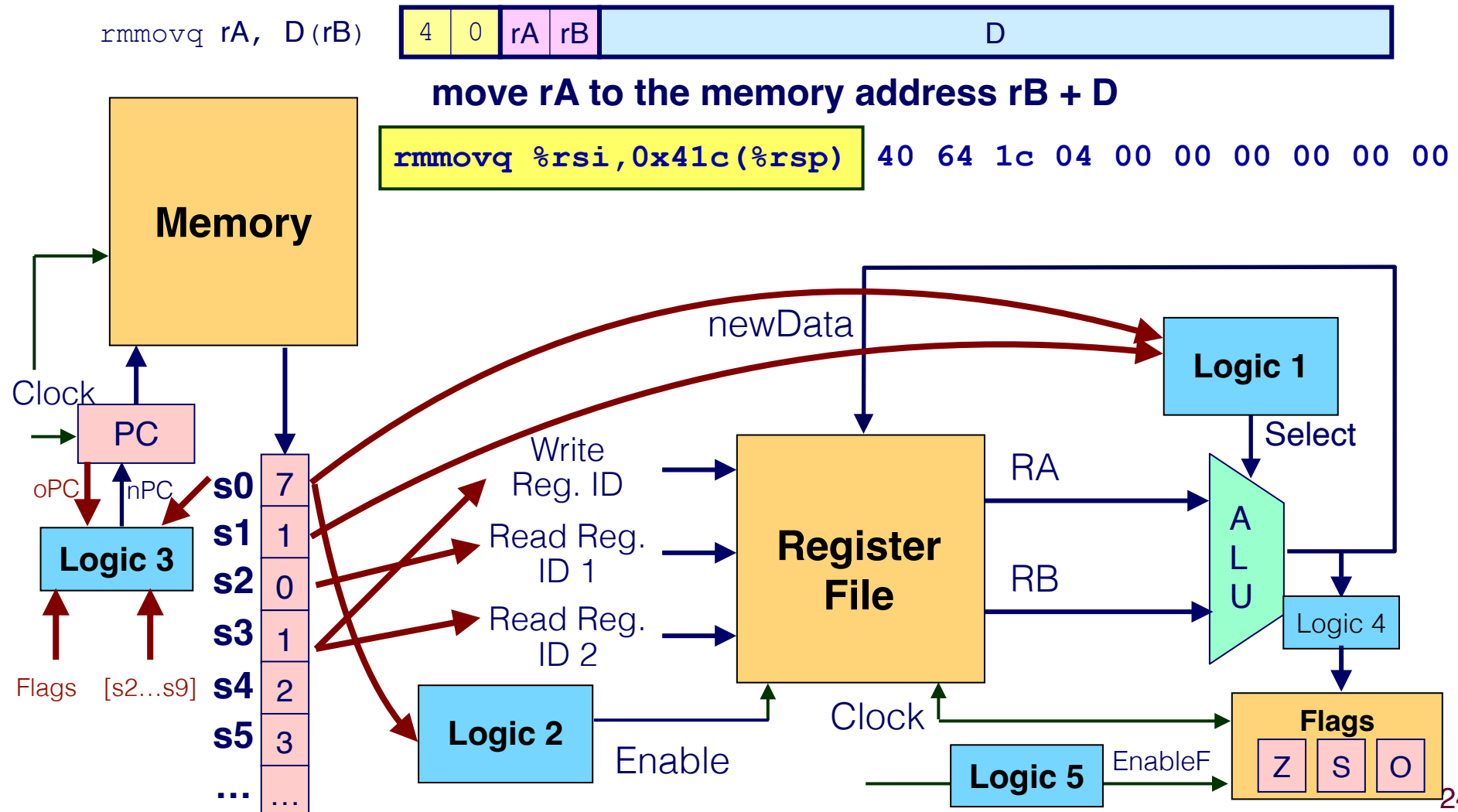


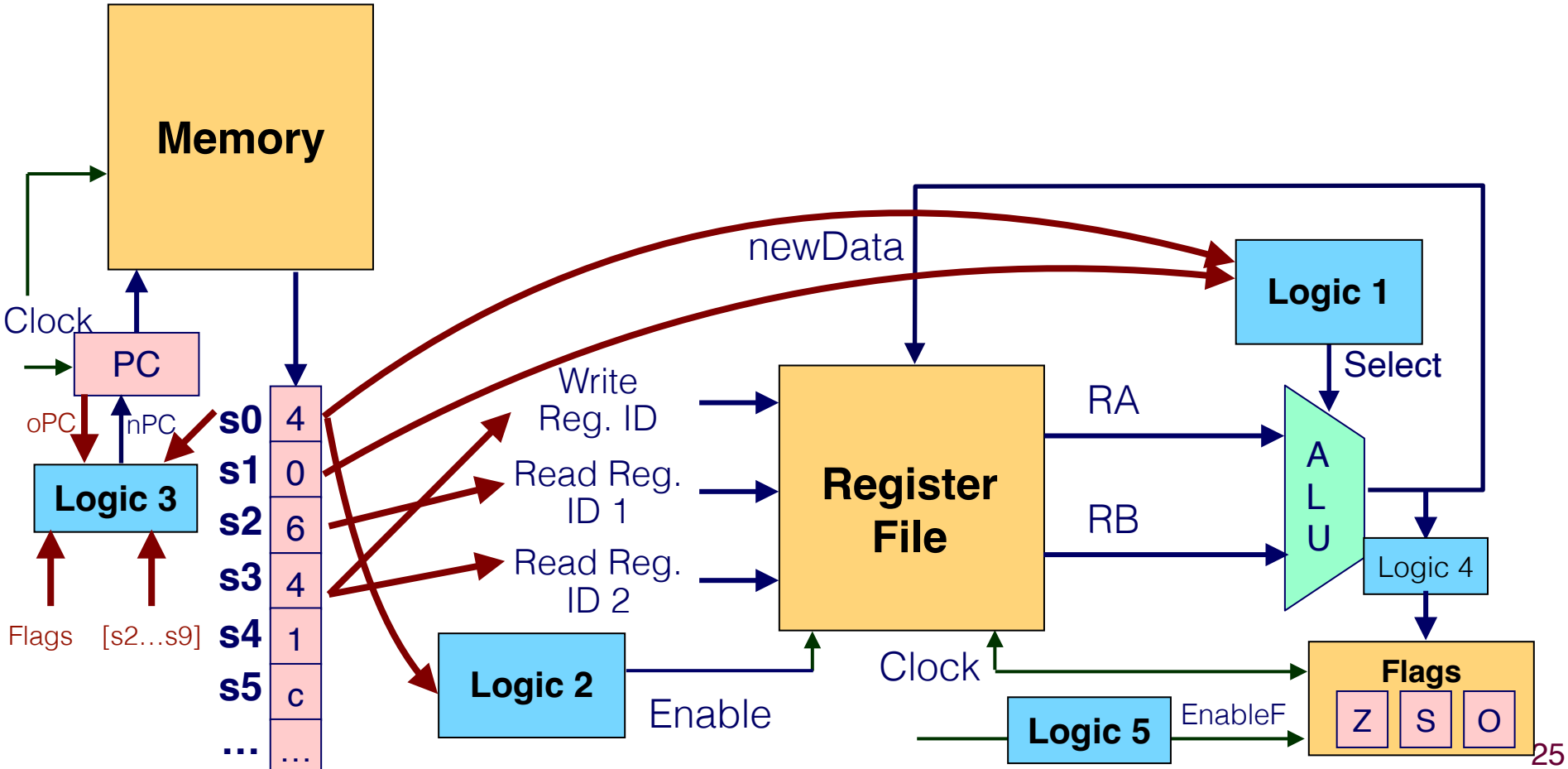
Executing a MOV instruction

- How do we modify the hardware to execute a move instruction?



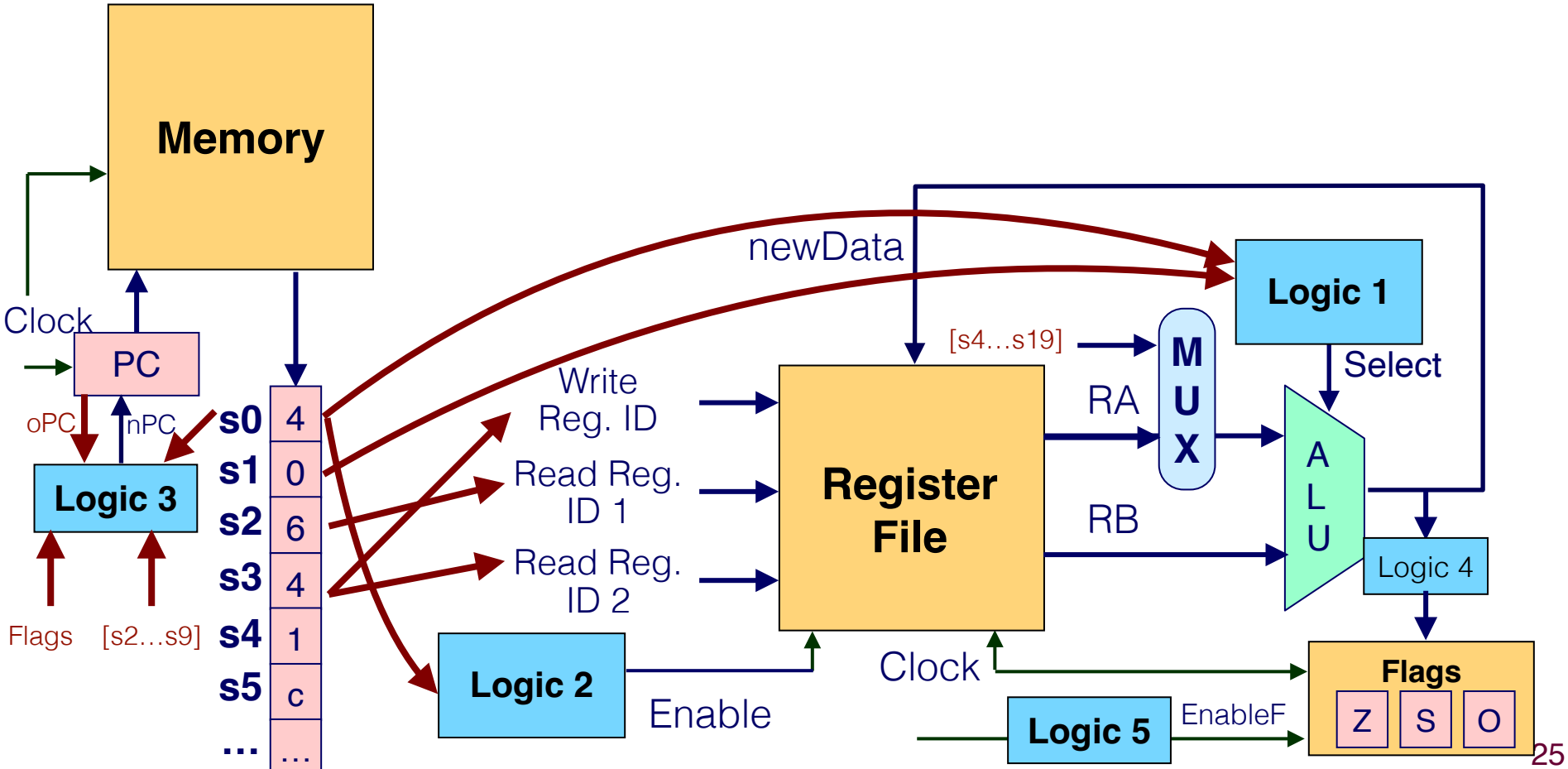
move rA to the memory address rB + D

`rmmovq rA, D(rB)`



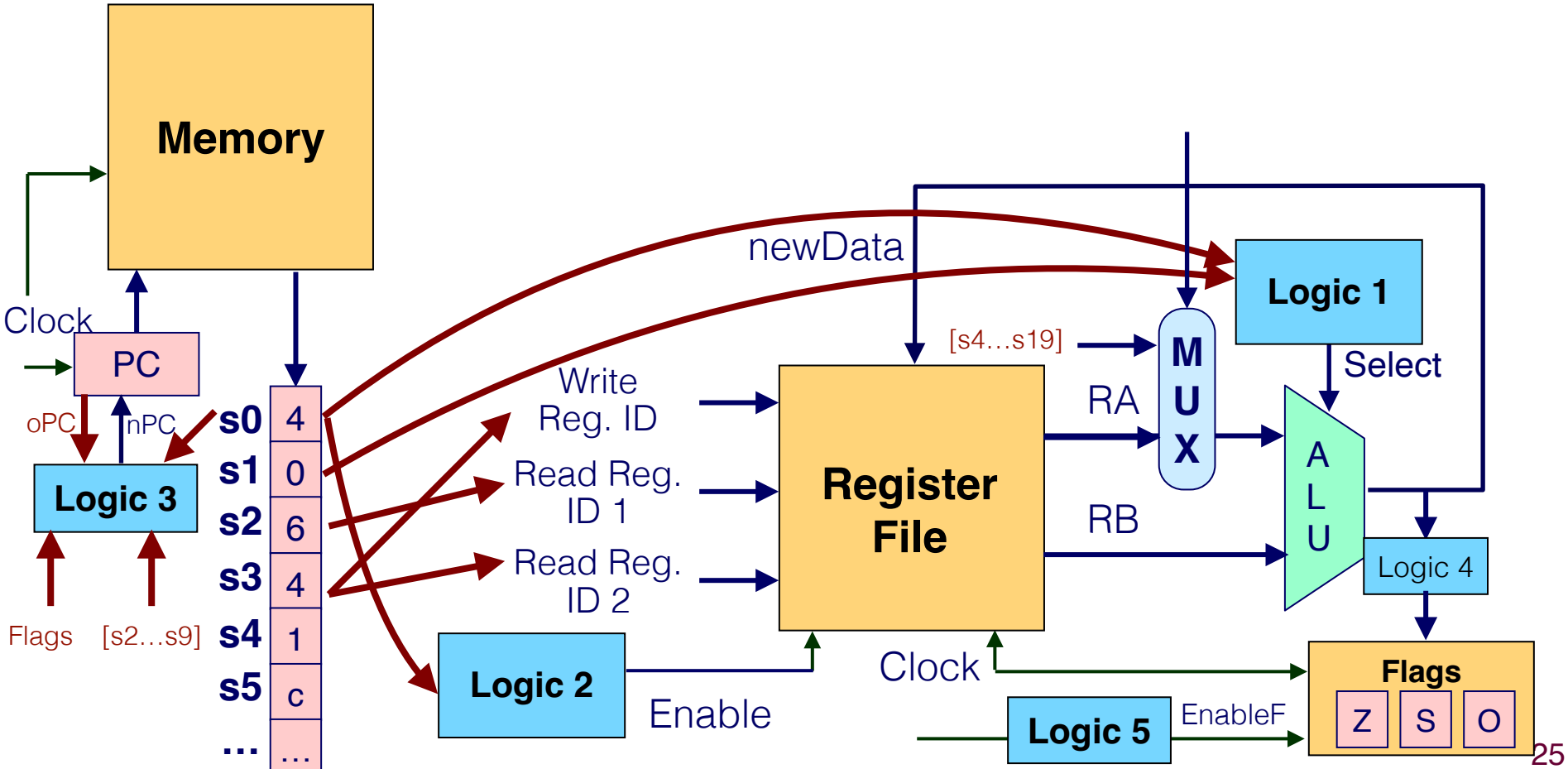
move rA to the memory address rB + D

`rmmovq rA, D(rB)`



move rA to the memory address rB + D

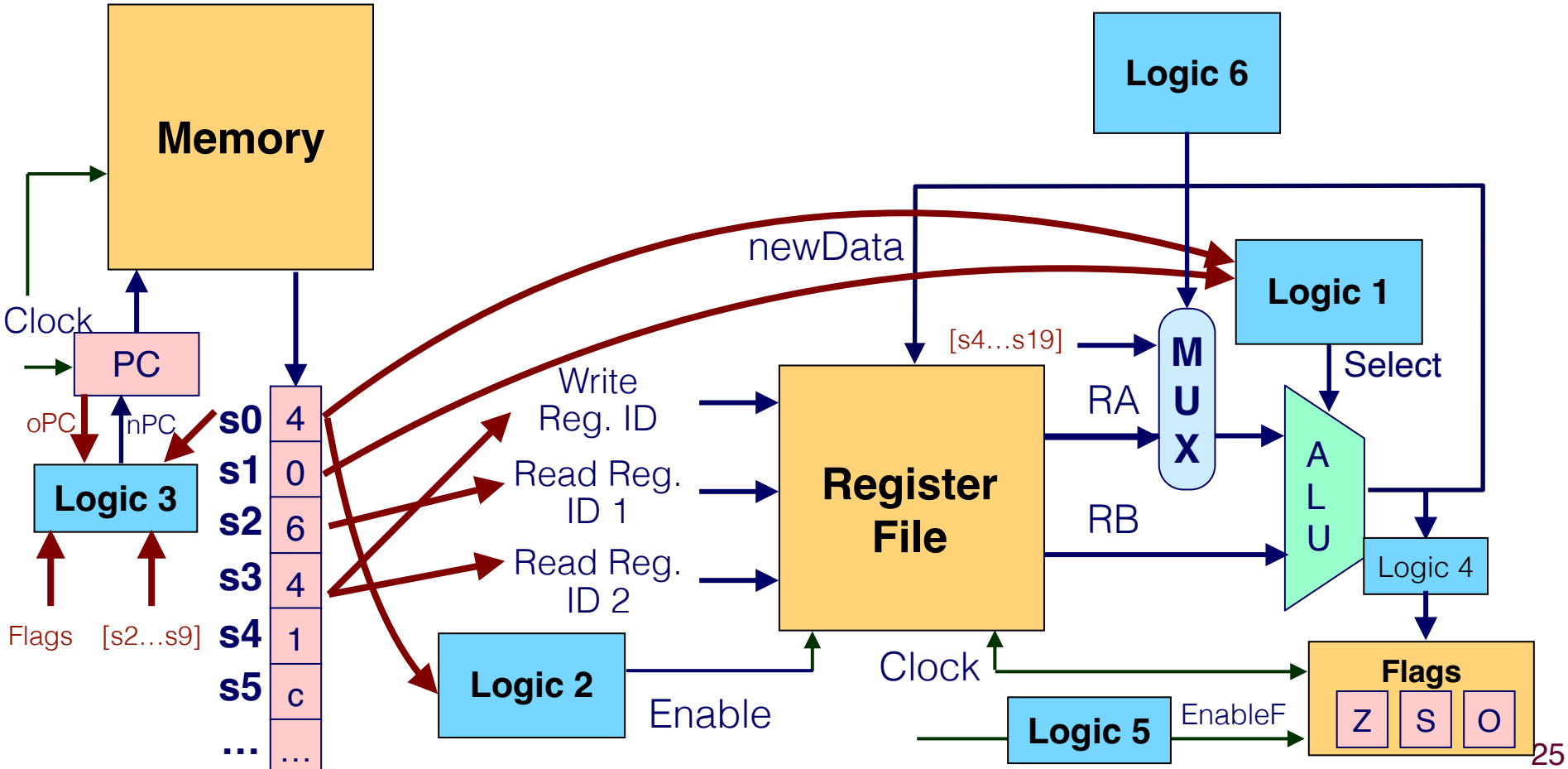
`rmmovq rA, D(rB)`



move rA to the memory address rB + D

`rmmovq rA, D(rB)`

- Need new logic (Logic 6) to select the input to the ALU for Enable.



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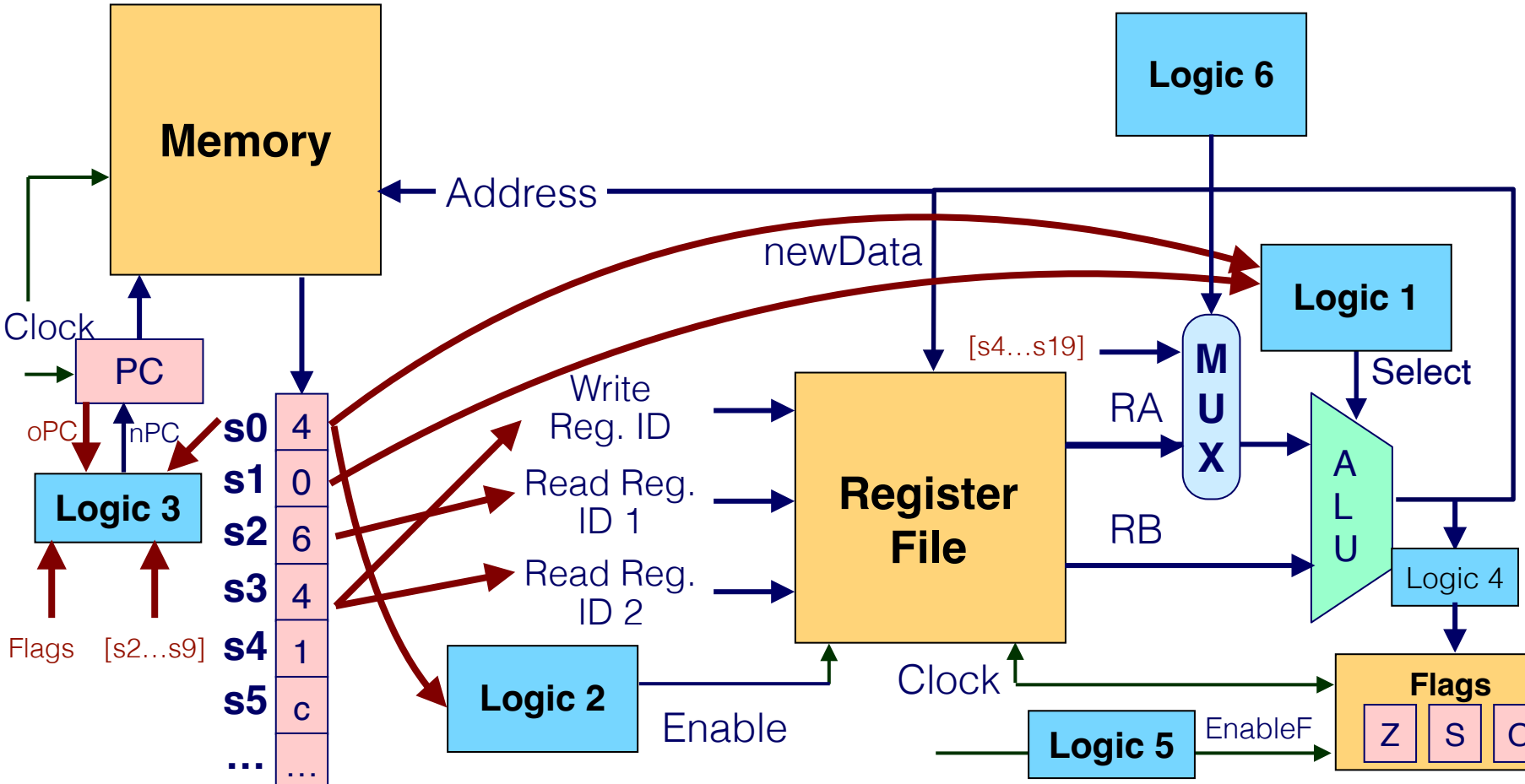

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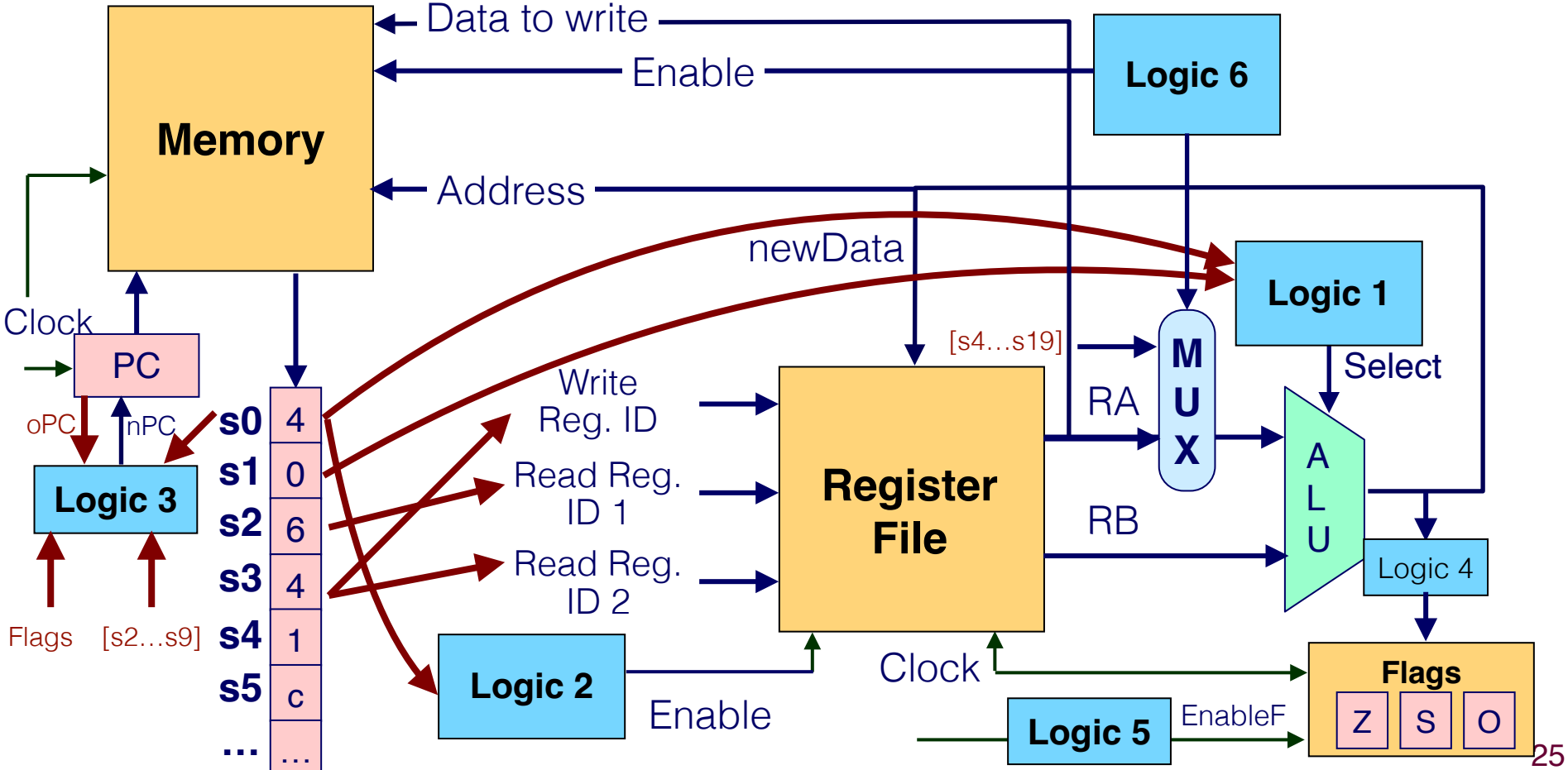

How About Memory to Register MOV?

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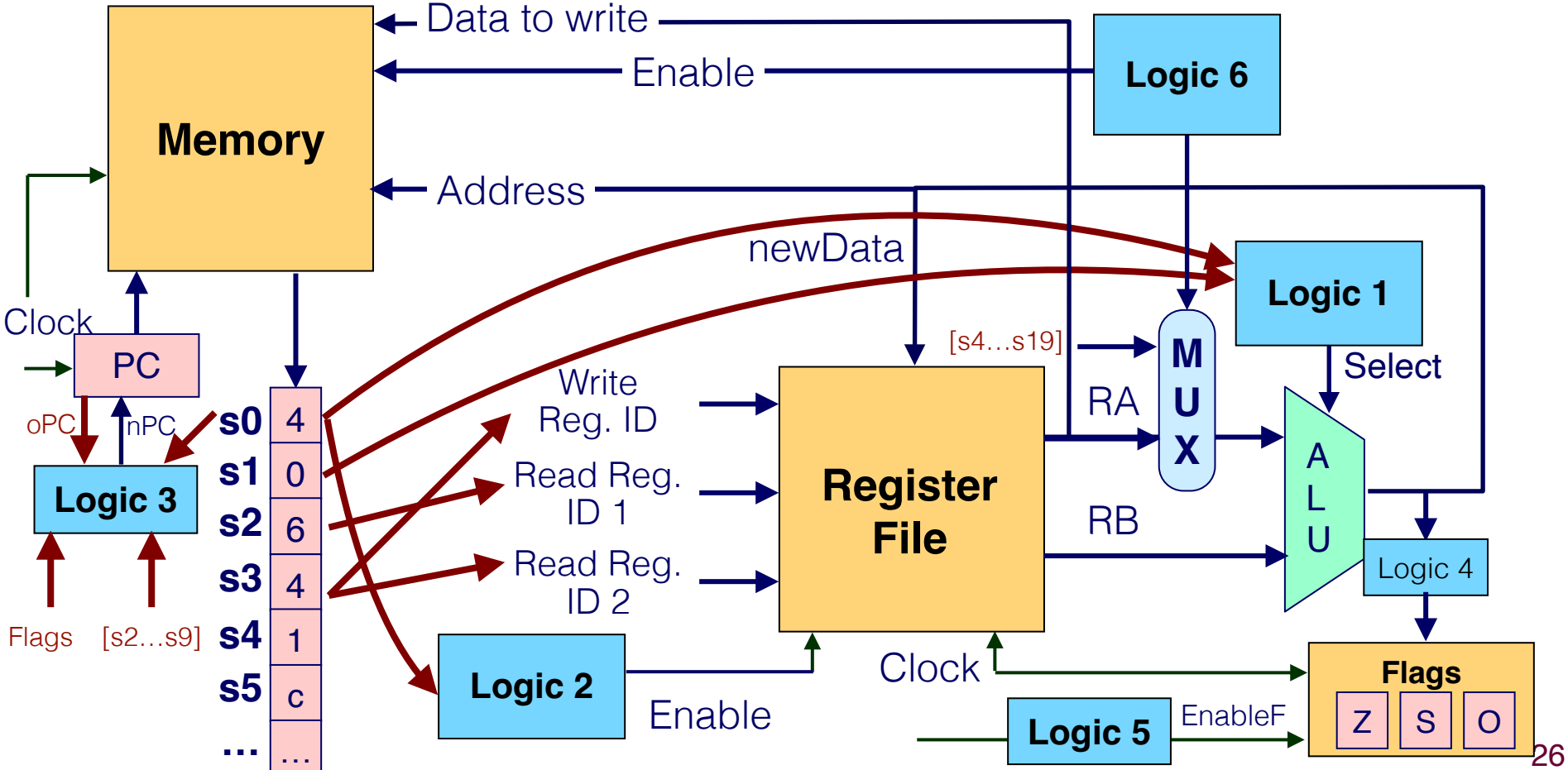

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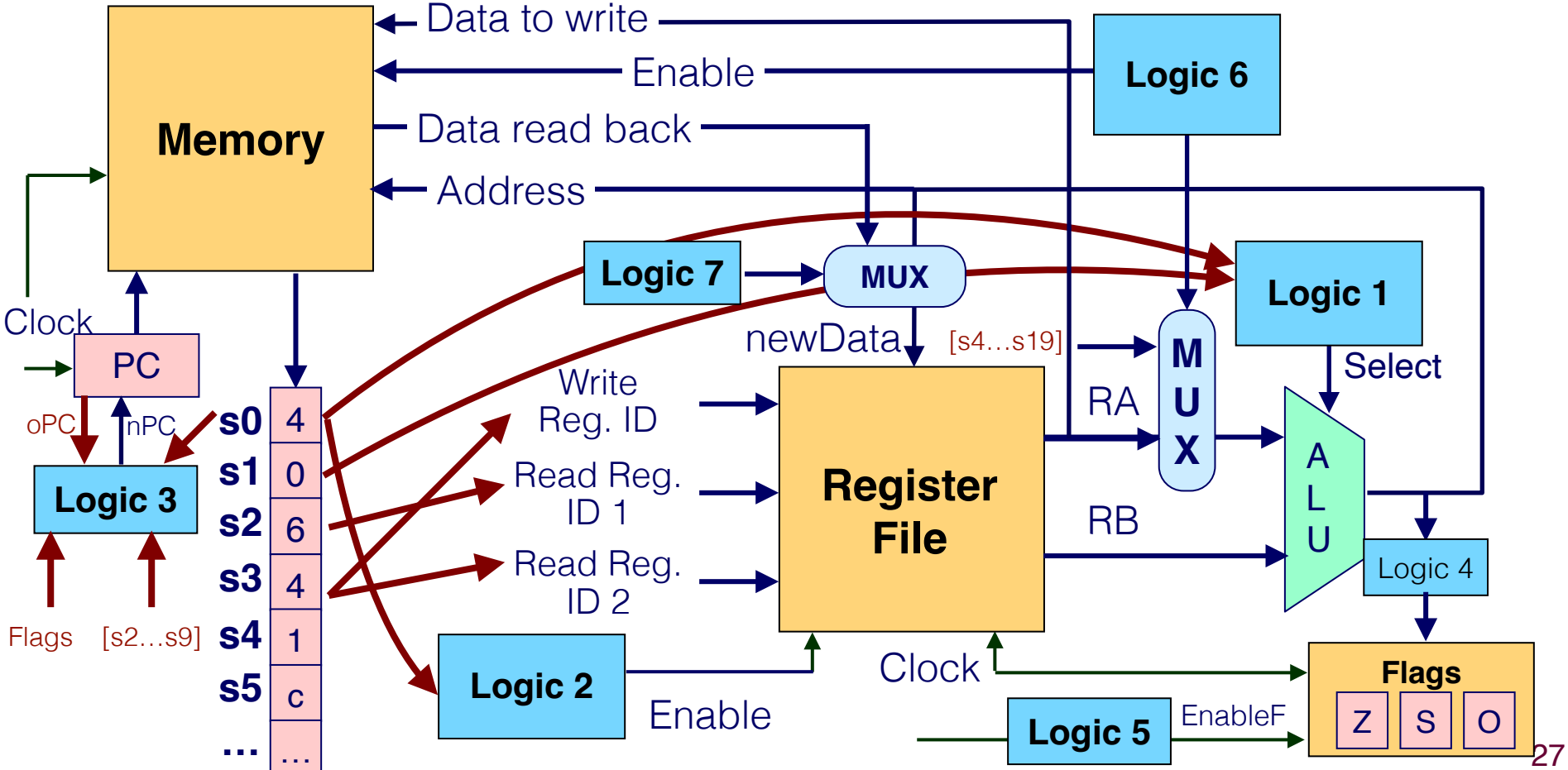
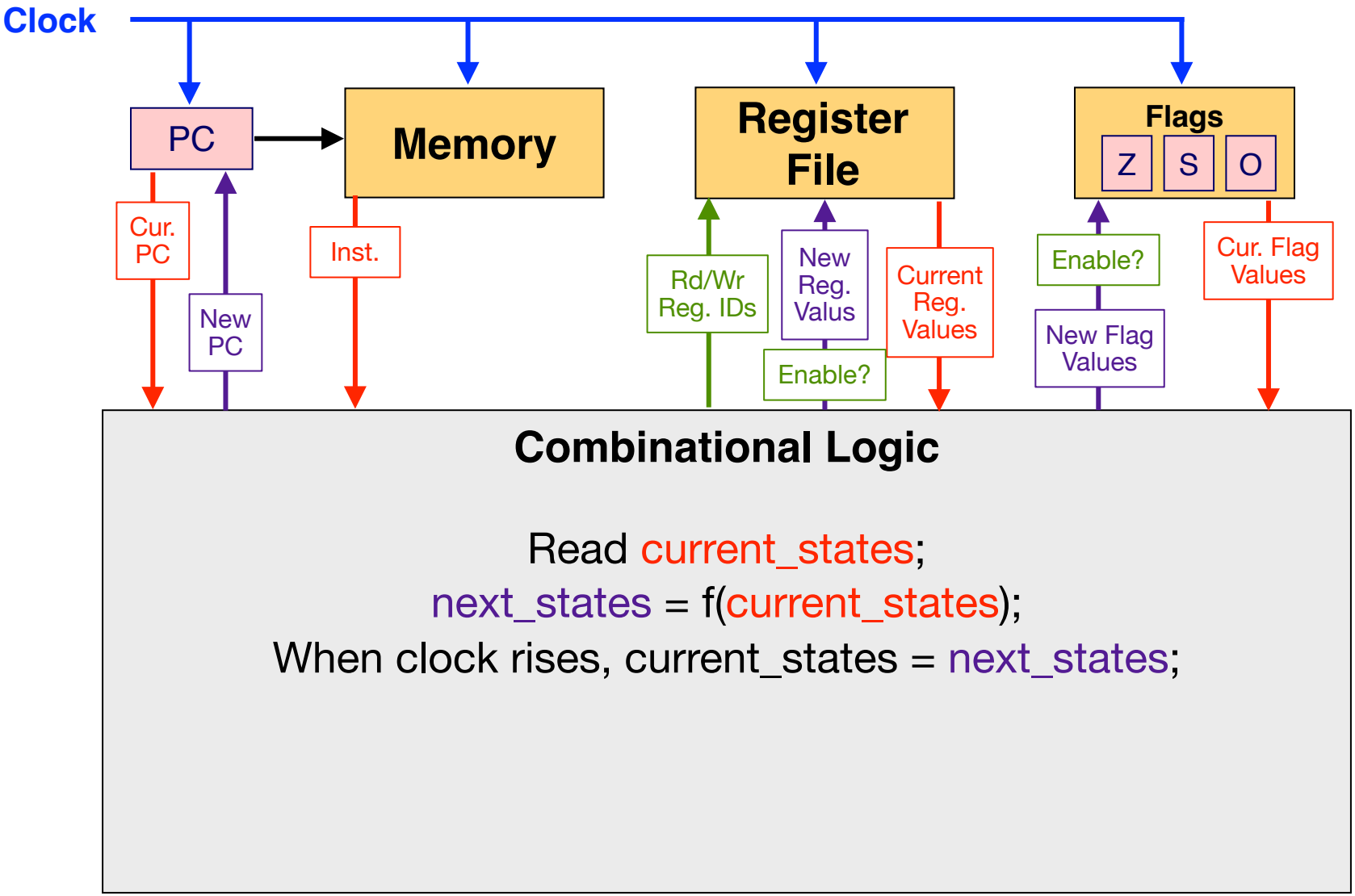


Microarchitecture (with MOV)



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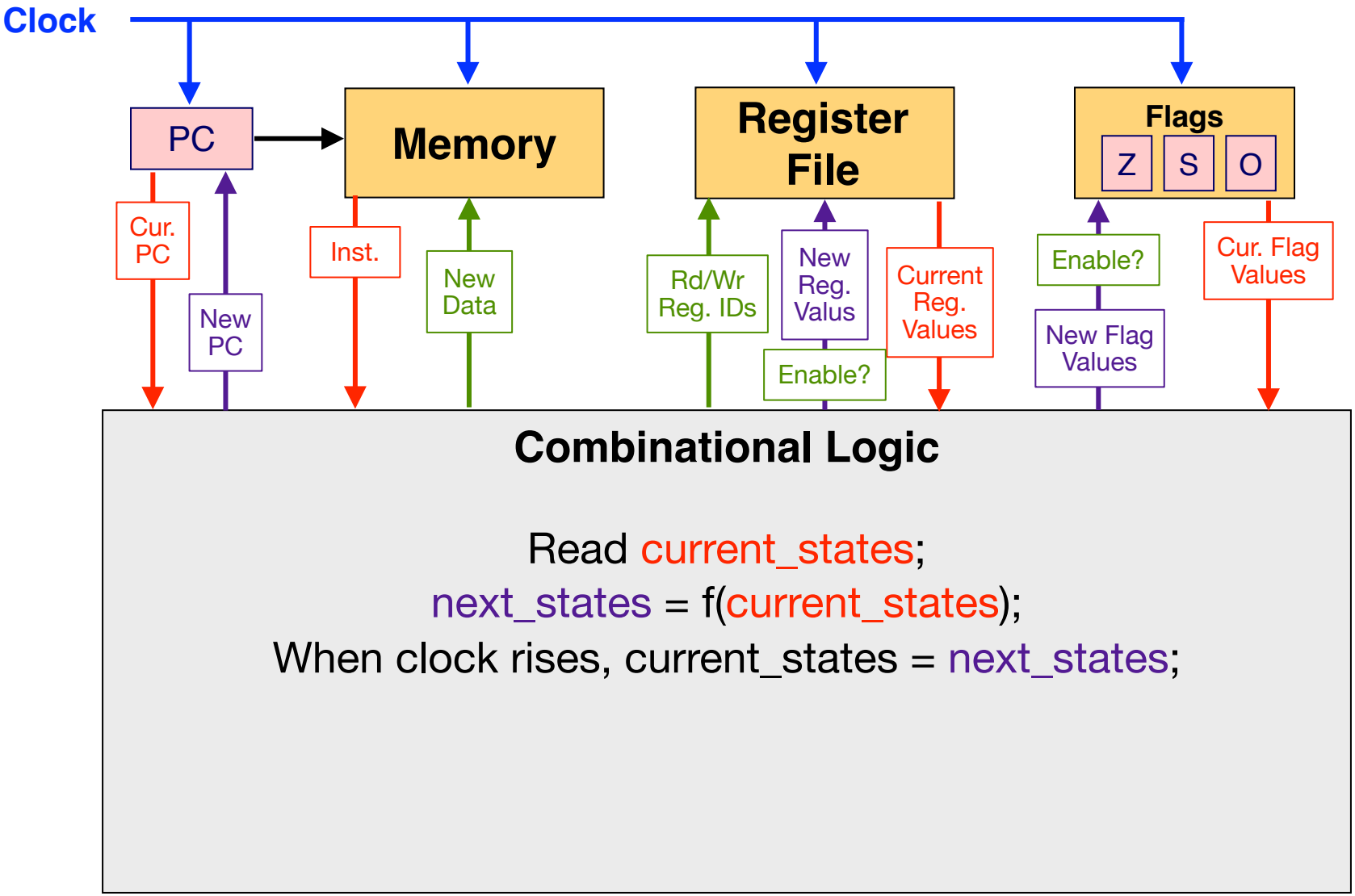

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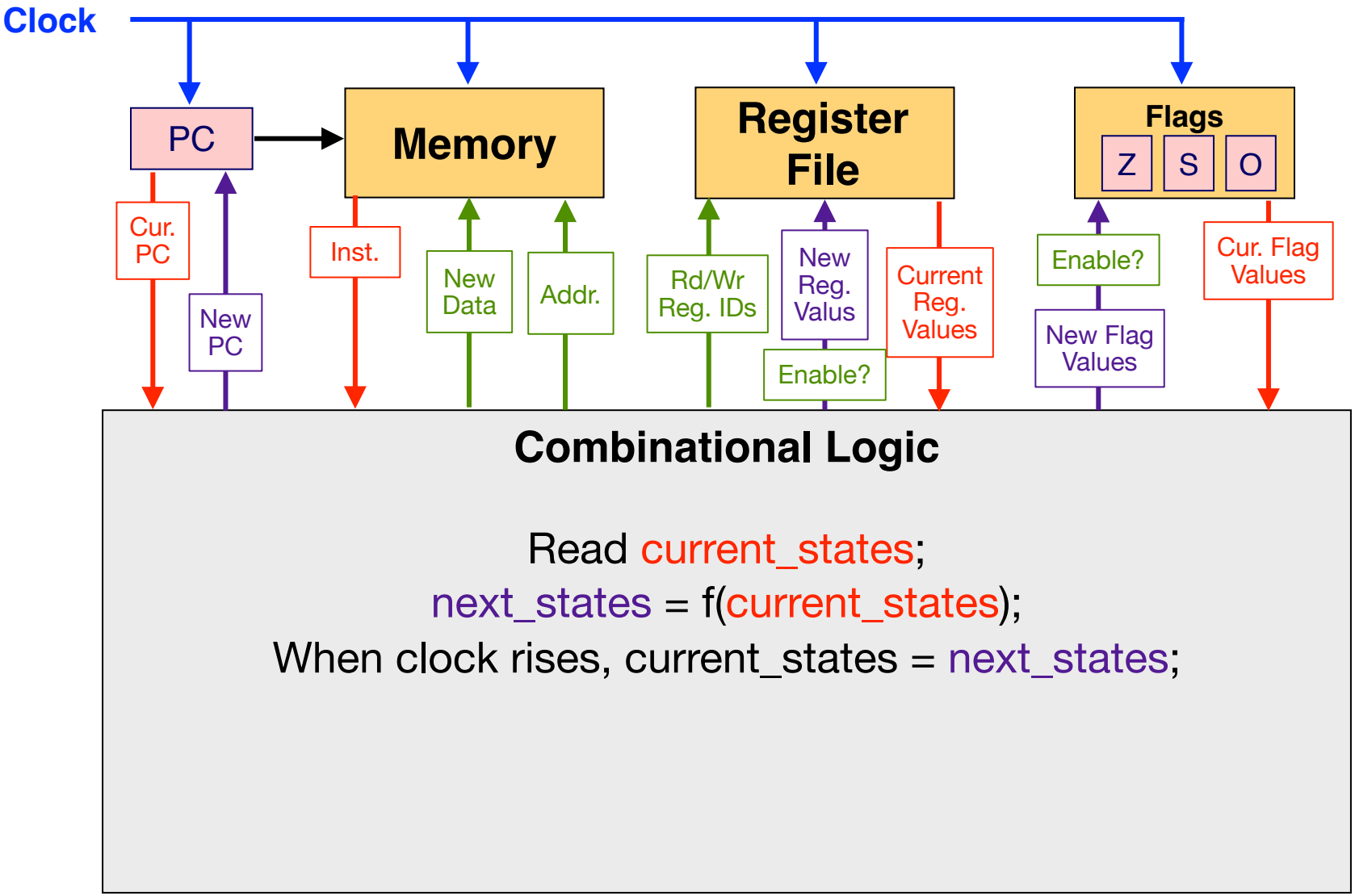

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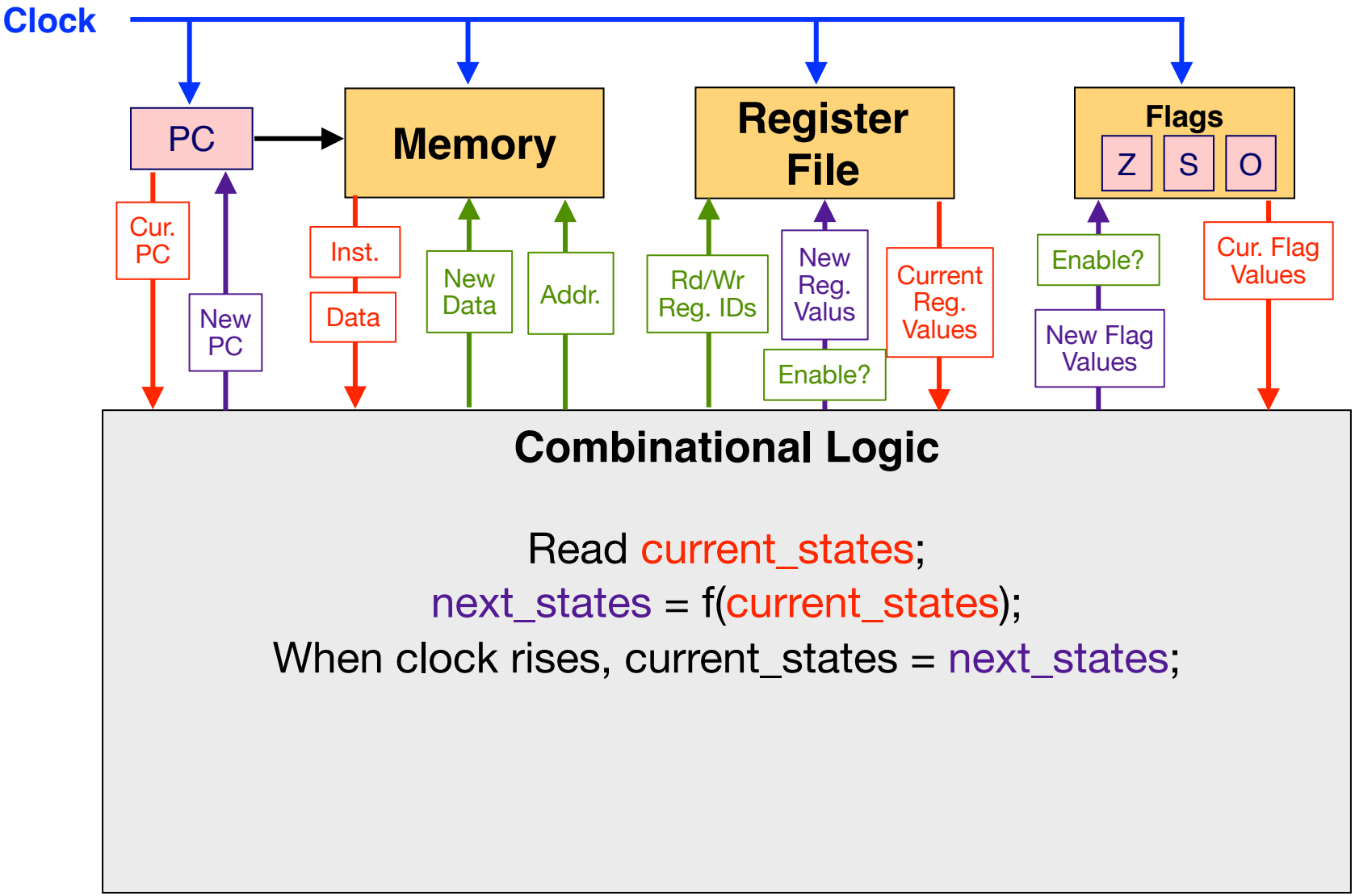

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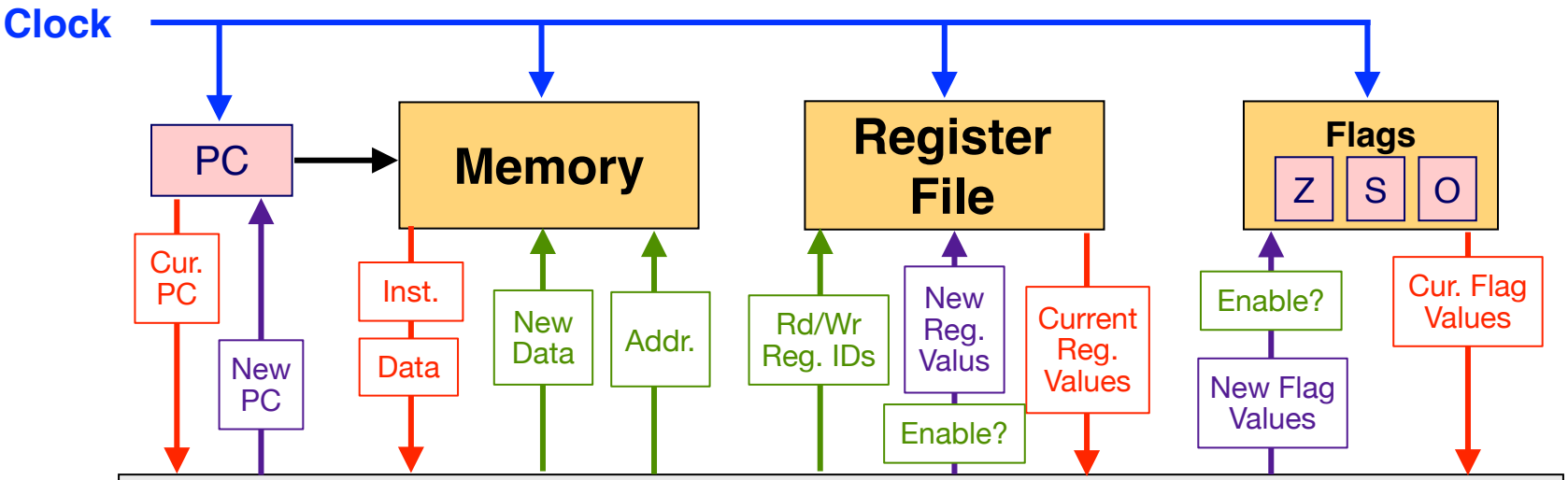


Read current_states;

next_states = f(current_states);

When clock rises, current_states = next_states;

next_states has to be ready before the close rises

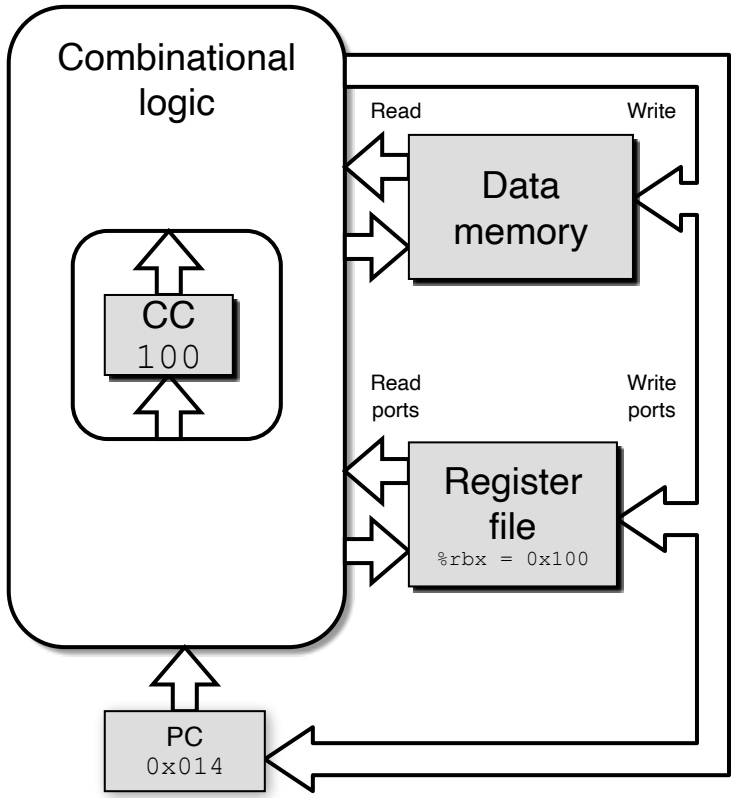
Single-Cycle Microarchitecture: Illustration

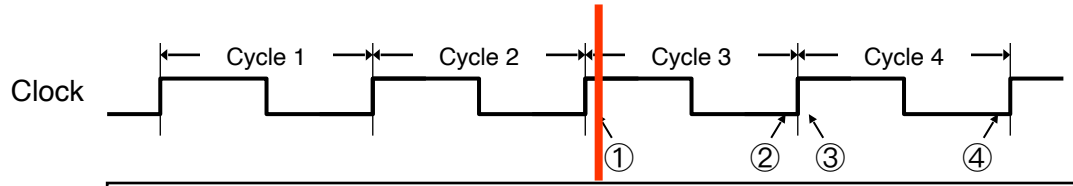
Think of it as a state machine

Every cycle, one instruction gets executed. At the end of the cycle, architecture states get modified.

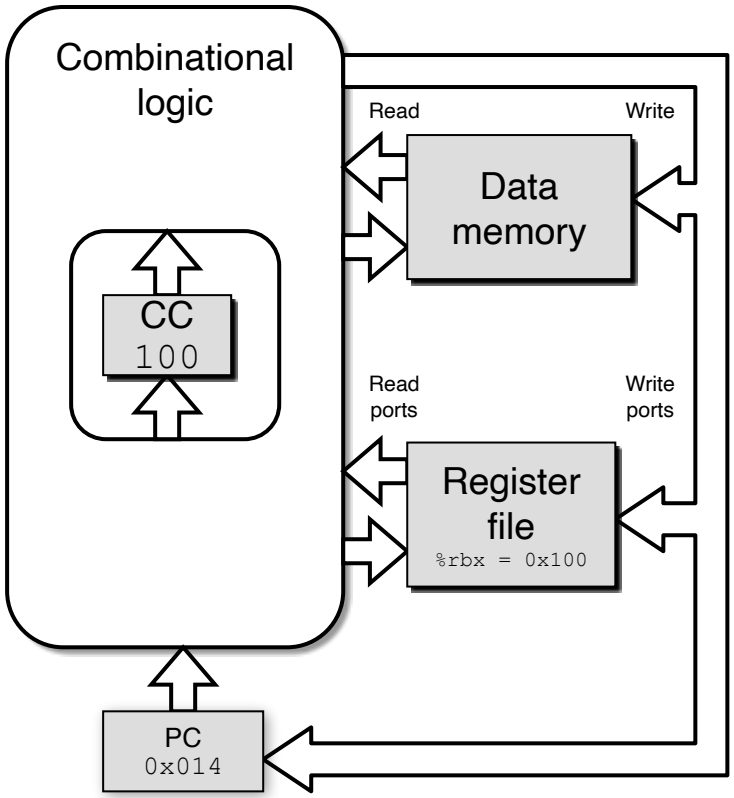
States (All updated as clock rises)

- PC register
- Cond. Code register
- Data memory
- Register file

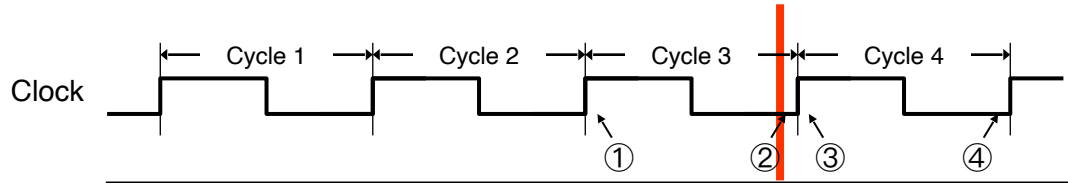




Cycle 1:	`0x000: irmovq $0x100,%rbx`	`# %rbx <-- 0x100`
Cycle 2:	`0x00a: irmovq $0x200,%rdx`	`# %rdx <-- 0x200`
Cycle 3:	`0x014: addq %rdx,%rbx`	`# %rbx <-- 0x300 CC <-- 000`
Cycle 4:	`0x016: je dest`	`# Not taken`
Cycle 5:	`0x01f: rmmovq %rbx,0(%rdx)`	`# M[0x200] <-- 0x300`



- state set according to second `irmovq` instruction
- combinational logic starting to react to state changes



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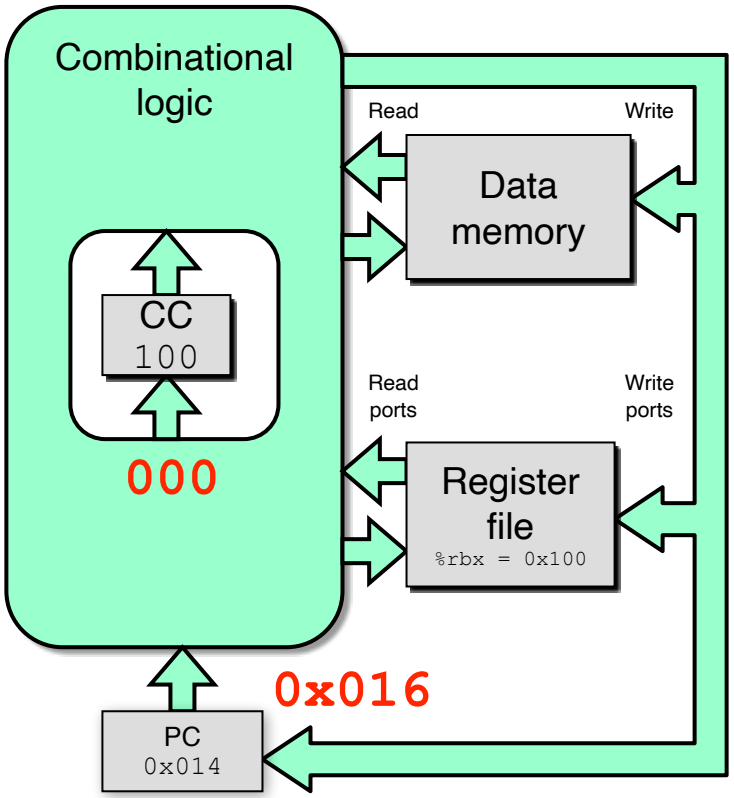
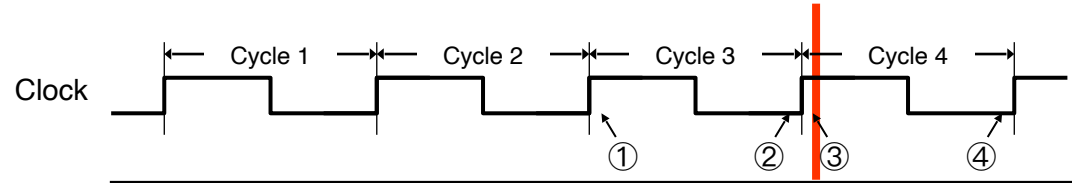


- state set according to second `irmovq` instruction
- combinational logic generates results for addq instruction



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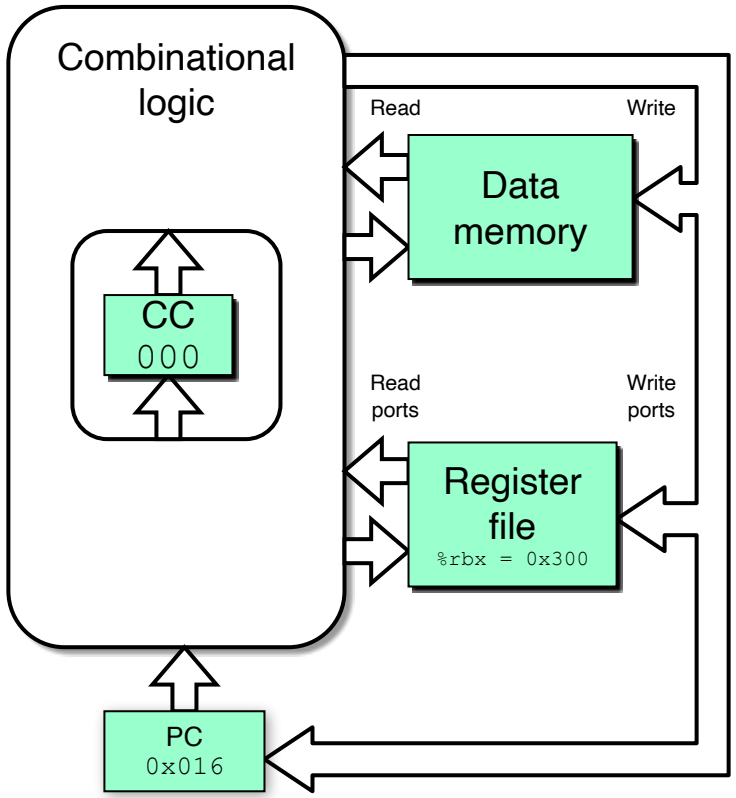

- state set according to `addq` instruction
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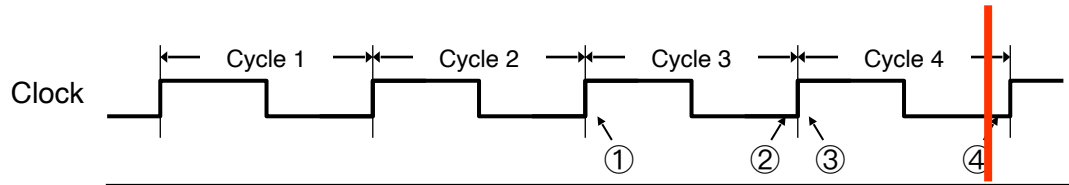

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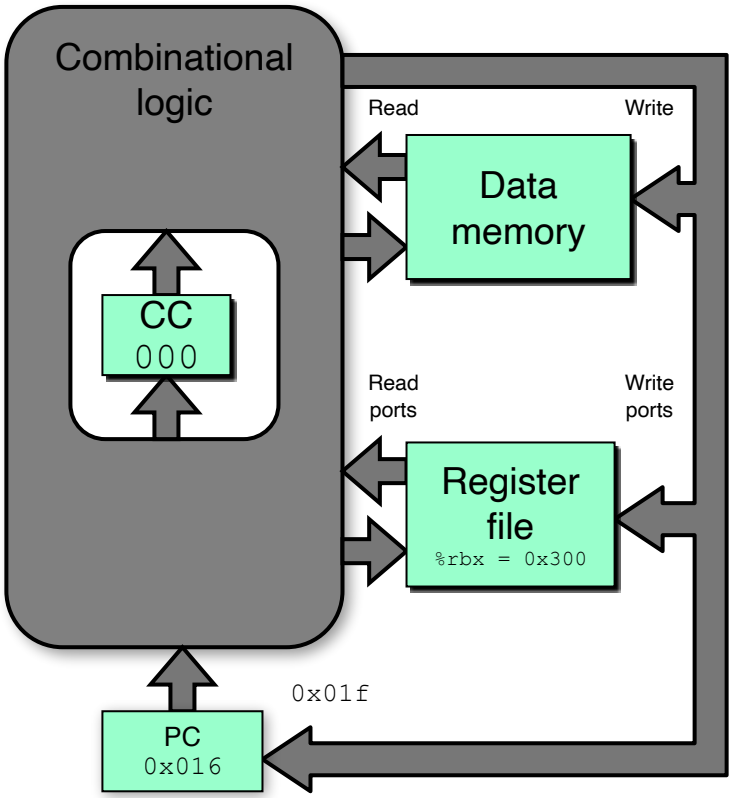

- state set according to `addq` instruction
- combinational logic generates results for `je` instruction

Processor Microarchitecture

- Sequential, single-cycle microarchitecture implementation
  - Basic idea
  - Hardware implementation
- Pipelined microarchitecture implementation
  - Basic Principles
  - Difficulties: Control Dependency
  - Difficulties: Data Dependency

Performance Model

Execution time of a program (in seconds) **= # of Dynamic Instructions**

X # of cycles taken to execute an instruction (on average)

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Improving Performance

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- We will talk about one technique that simultaneously achieves 2 & 3.

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  - The entire hardware is occupied to execute one instruction at a time. Can’t execute multiple instructions at the same time.
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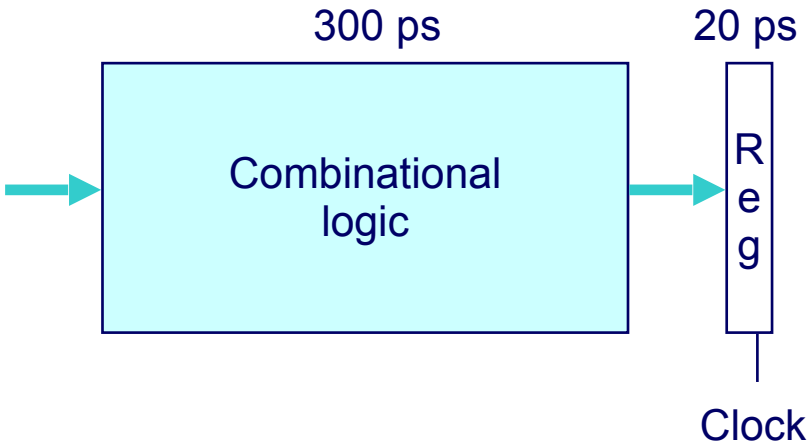
A Motivating Example



- Computation requires total of 300 picoseconds
- Additional 20 picoseconds to save result in register
- Must have clock cycle time of at least 320 ps