CSC 252/452: Computer Organization
Fall 2025: Lecture 6

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Department of Computer Science
University of Rochester

Announcement

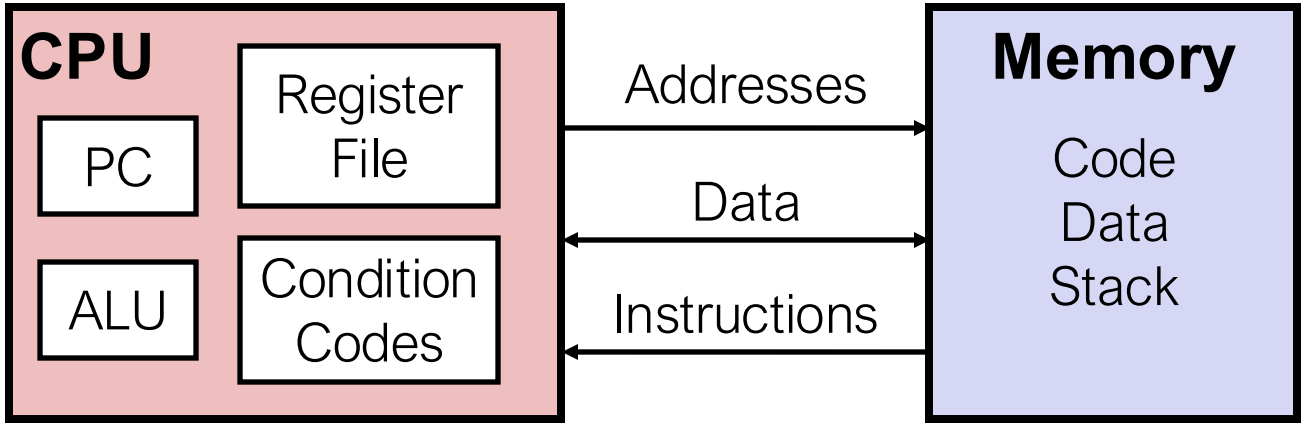
- Programming Assignment 1 is due today
  - NetID is not your 8-digit URID
  - For using slip days, email the two TAs listed in the assignment description
- Programming Assignment 2 is out today
  - Details: https://www.cs.rochester.edu/courses/252/fall2025/labs/assignment2.html
  - Due on **Oct 1st**, 11:59 PM
  - You (may still) have 3 slip days

Announcement

- Programming assignment 2 is in x86 assembly language.
- Read the instructions before getting started!!!
  - You get 1/4 point off for every wrong answer
  - Maxed out at 10
- TAs are best positioned to answer your questions about programming assignments!!!
- Programming assignments do NOT repeat the lecture materials. They ask you to synthesize what you have learned from the lectures and work out something new.

Instruction Processing Sequence

Assembly Programmer's Perspective of a Computer



Fetch Instruction (According to PC)

Instruction Processing Sequence

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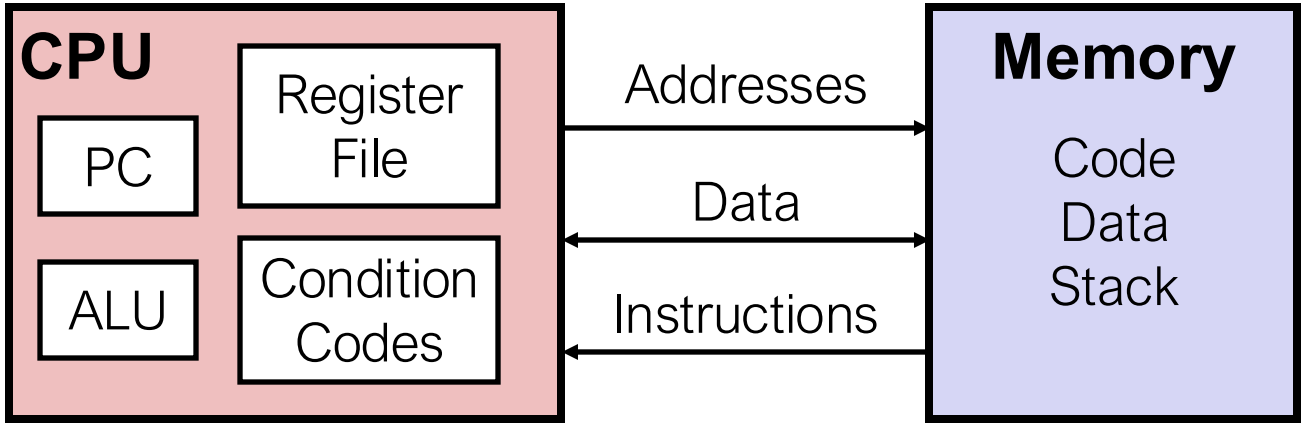

Fetch Instruction (According to PC)

`0x4801d8`

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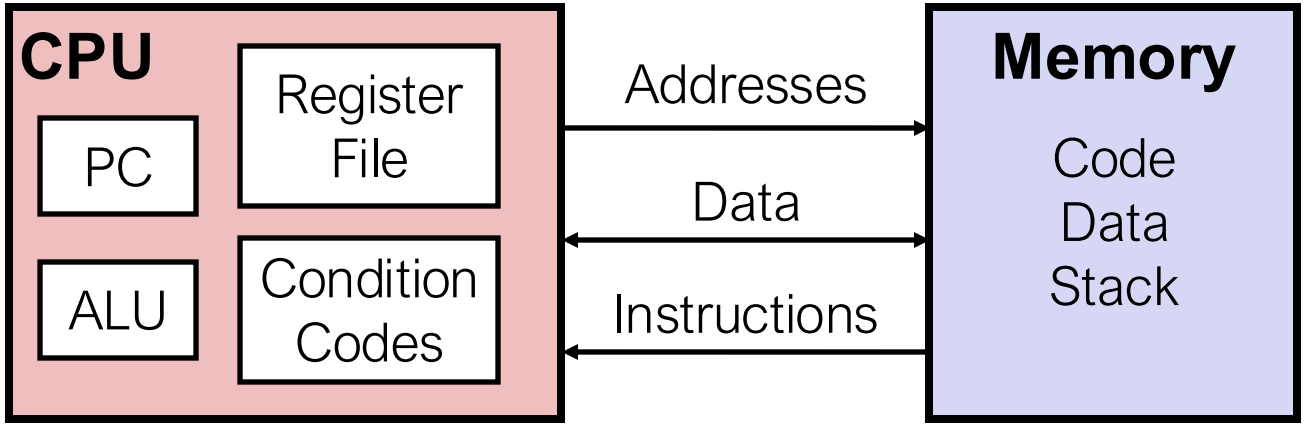

Fetch Instruction (According to PC) → Decode Instruction

```
addq %rax,(%rbx)
```

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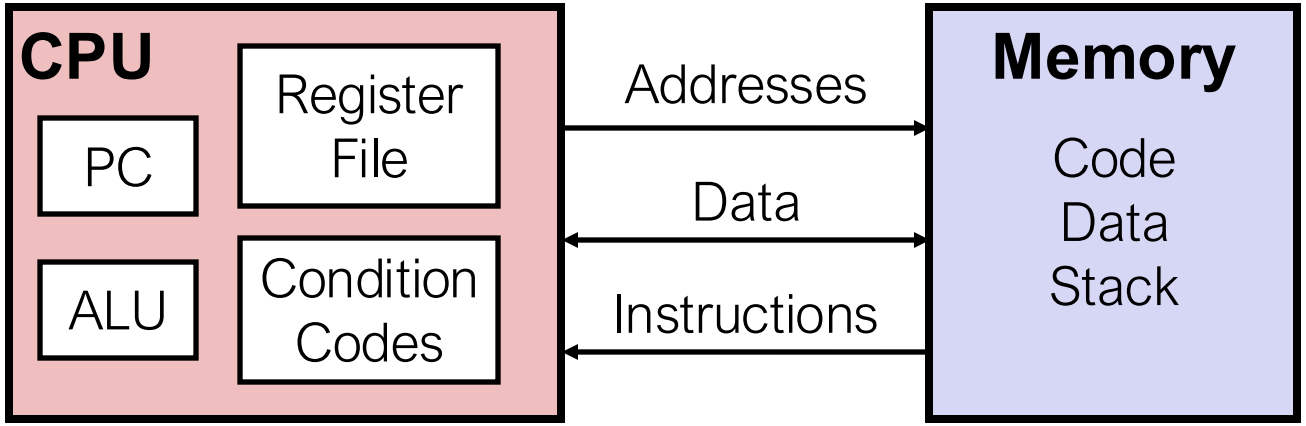

Fetch Instruction (According to PC) → Decode Instruction → Fetch Operands

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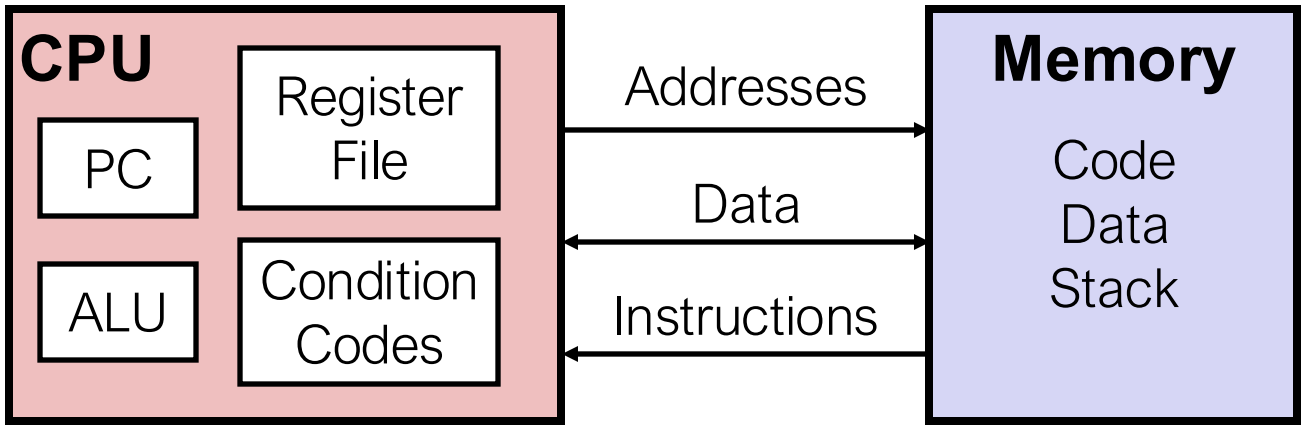

Fetch Instruction (According to PC) → Decode Instruction → Fetch Operands → Execute Instruction

Instruction Processing Sequence

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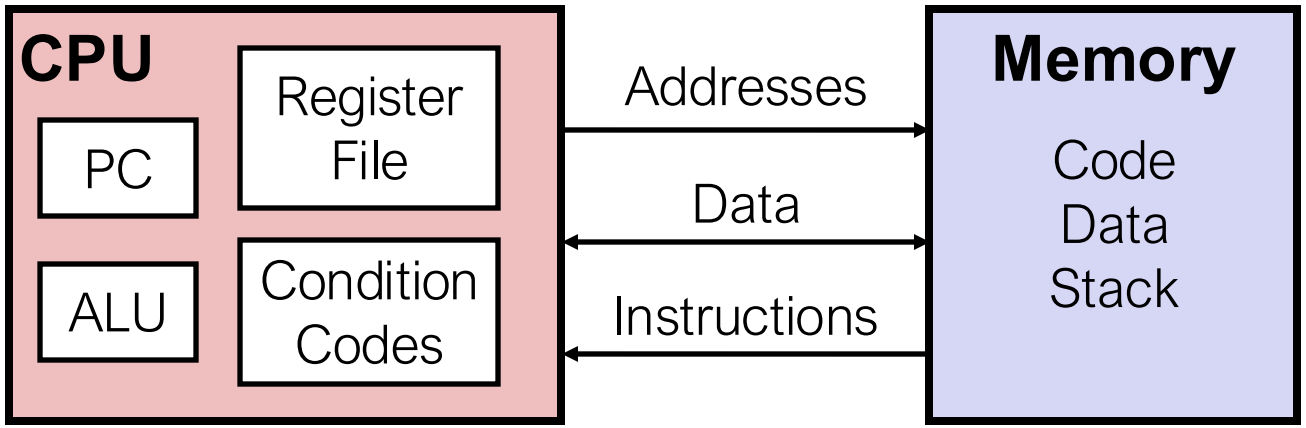

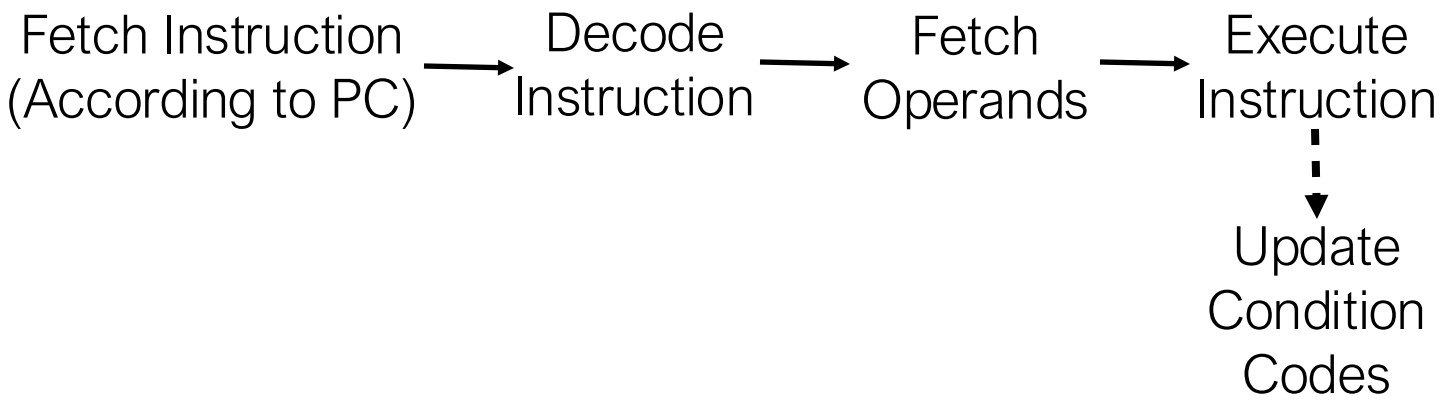

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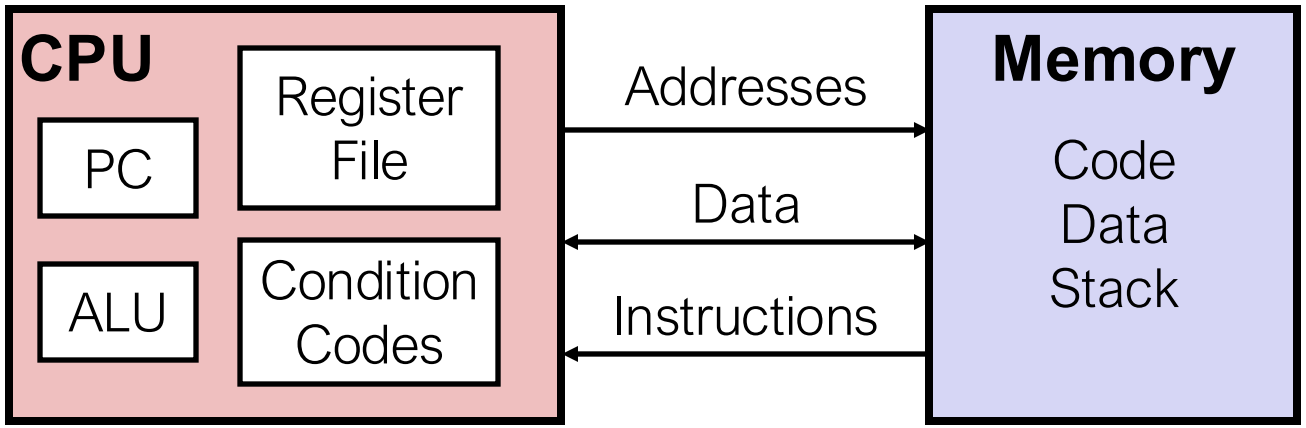

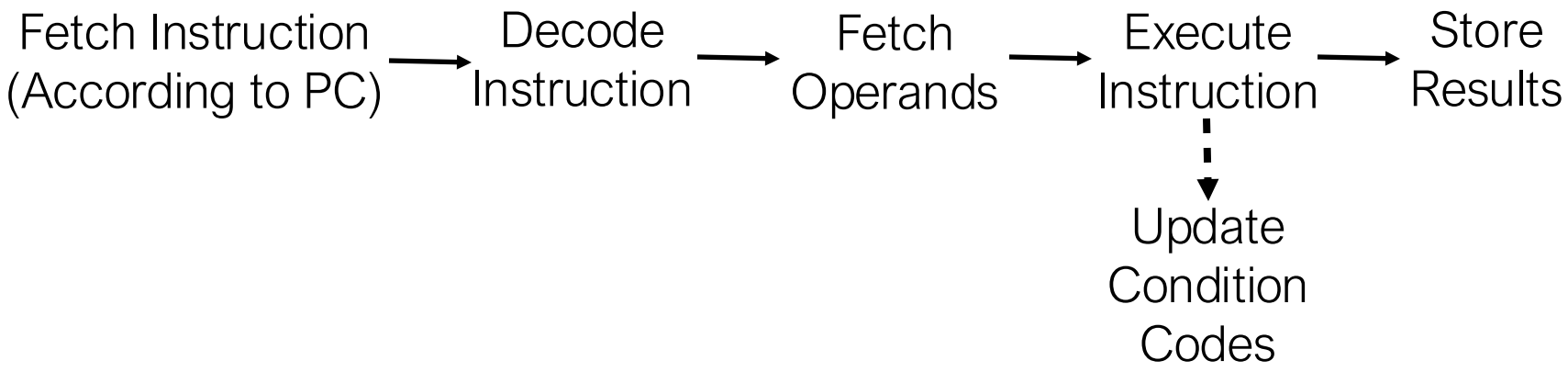

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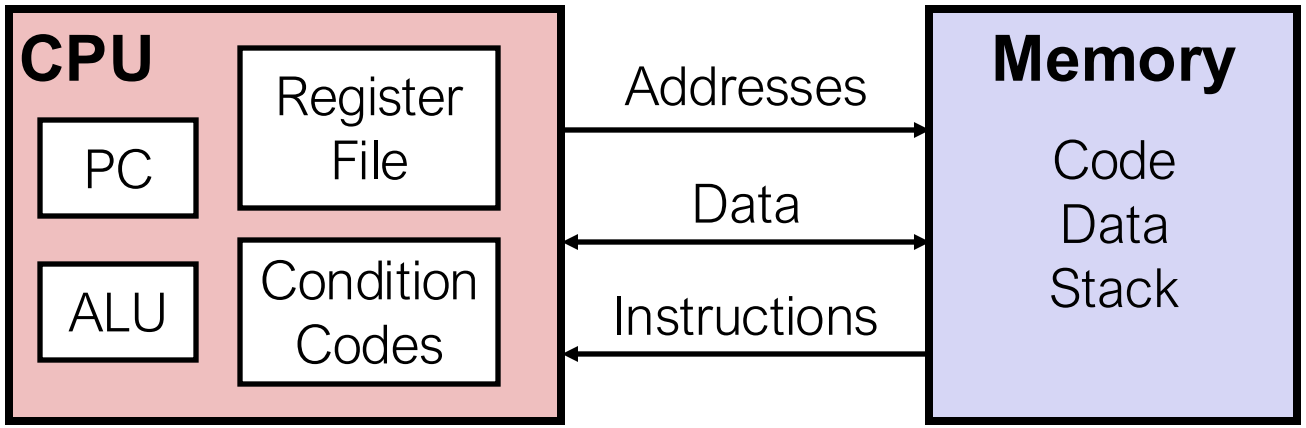

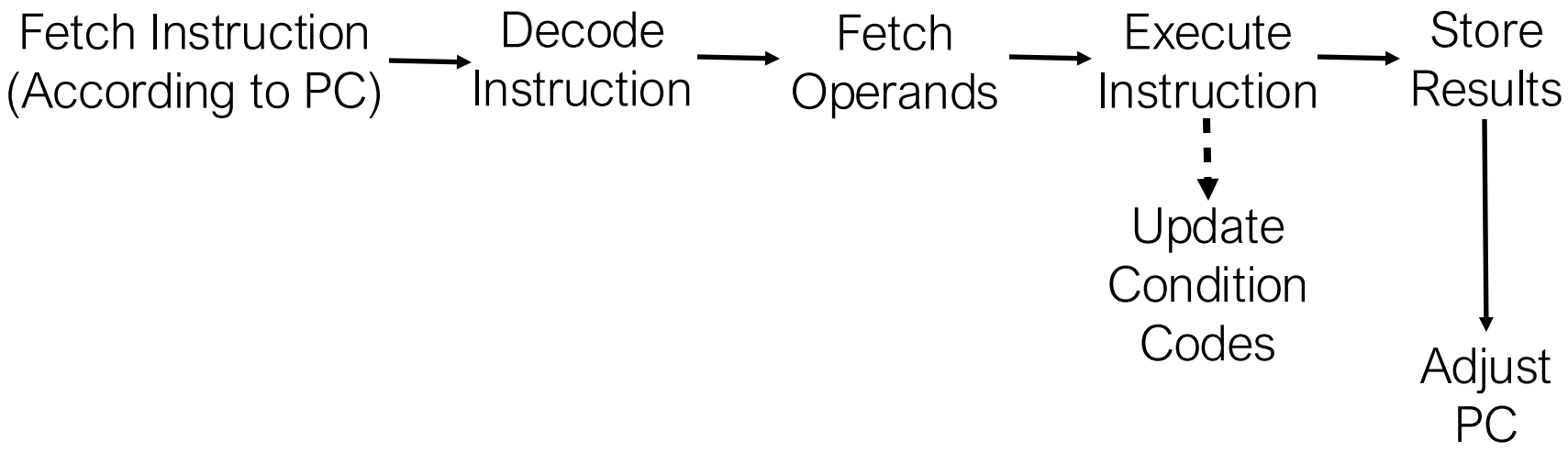

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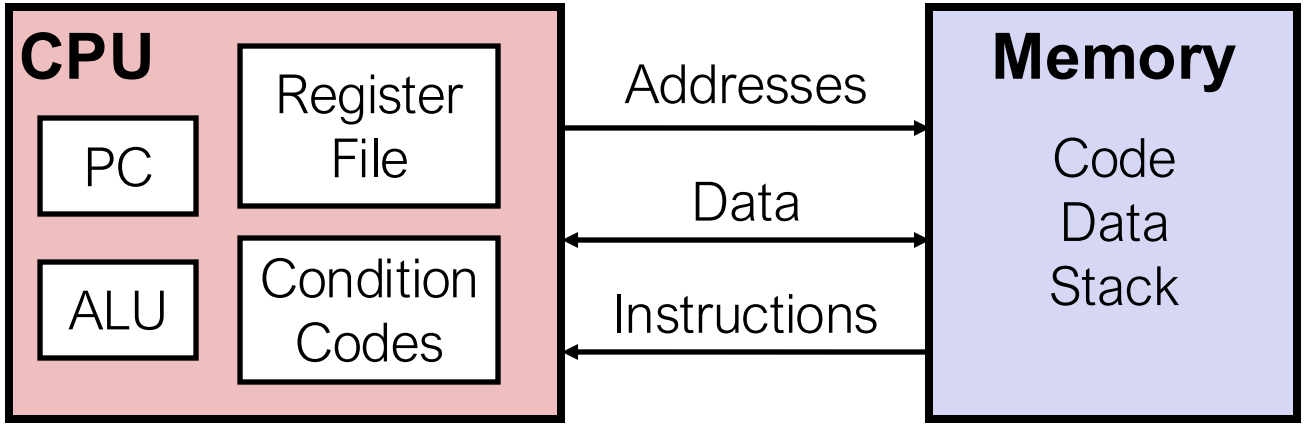

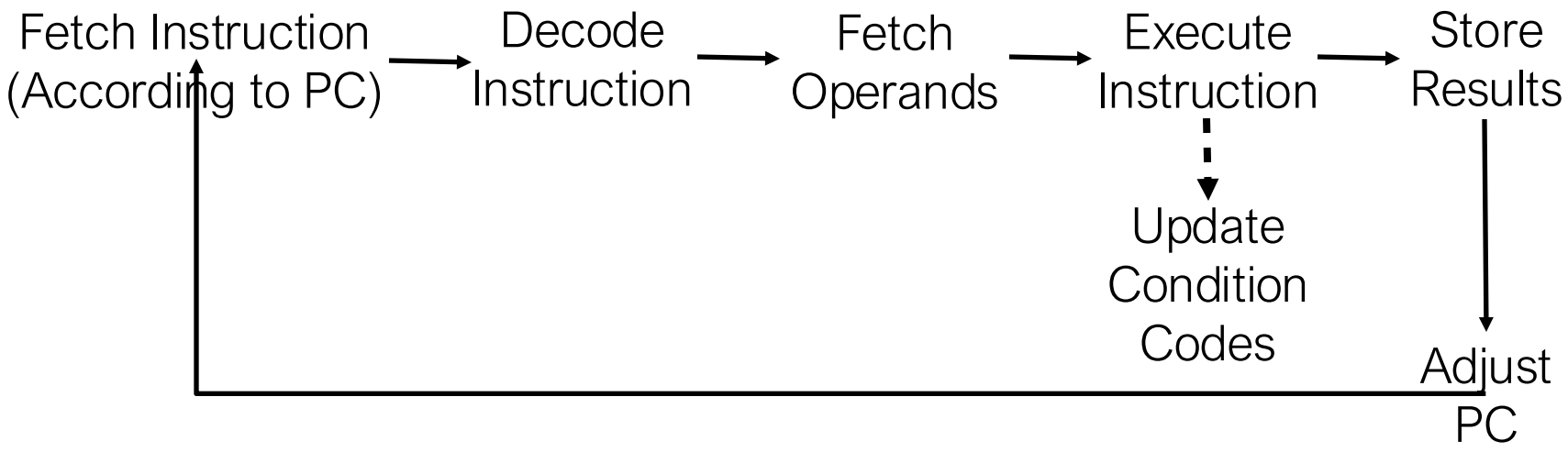

Assembly Program Instructions

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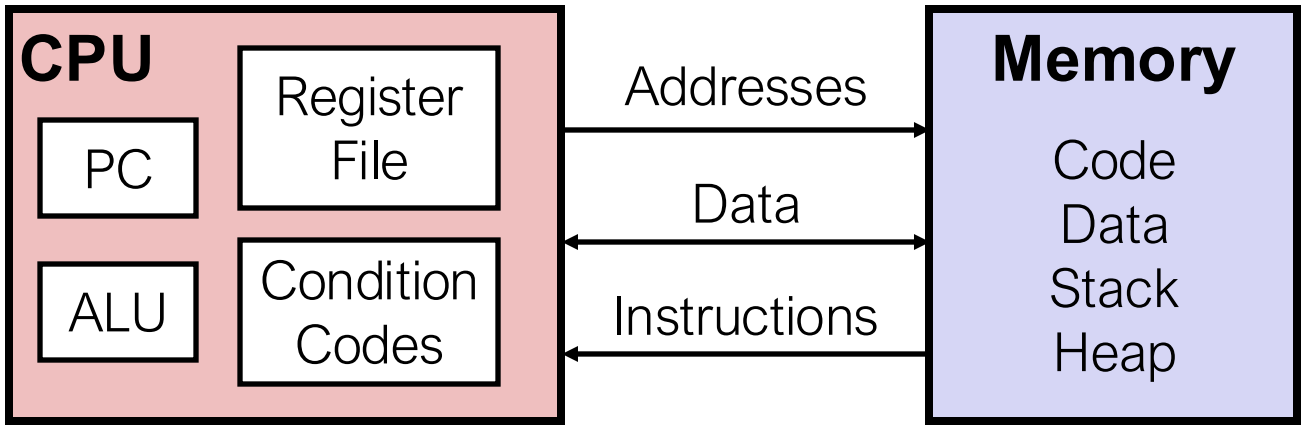

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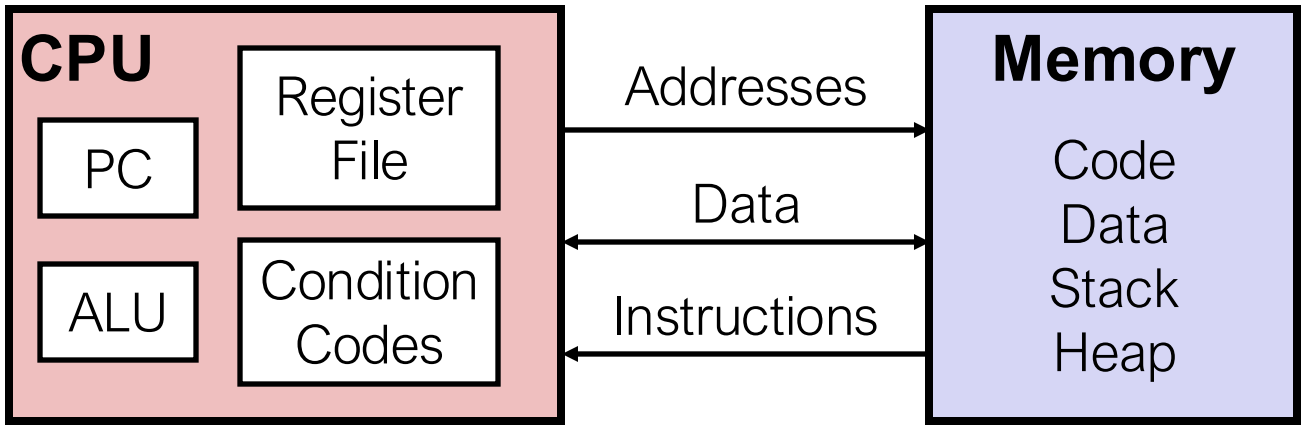

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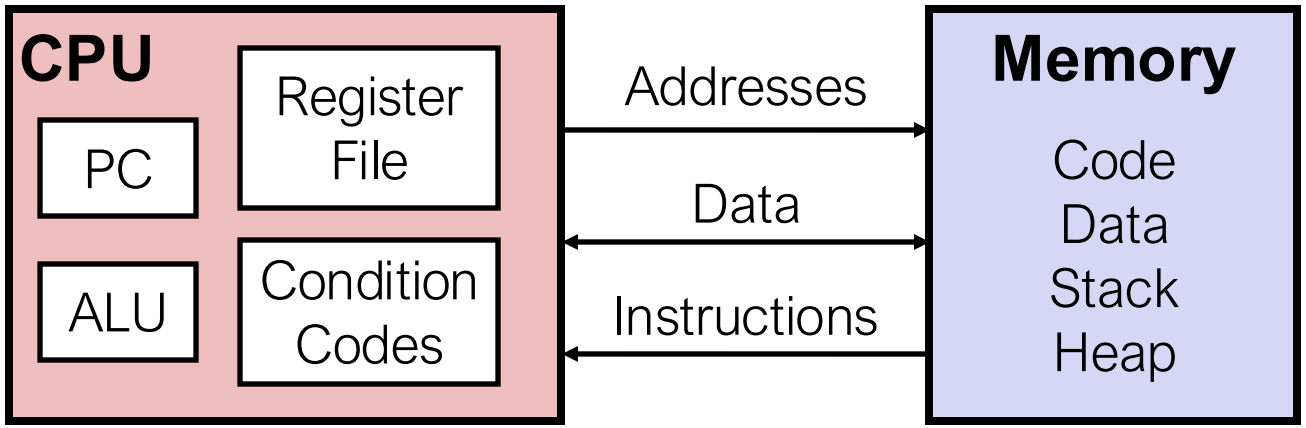

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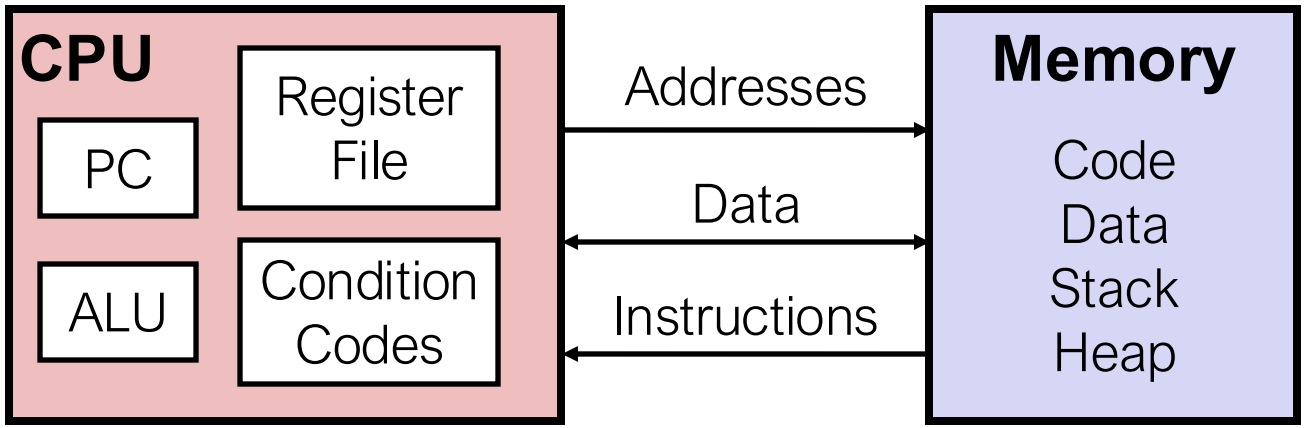

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  - **`addq %eax, %ebx`**
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- *Data Movement Instruction*: Transfer data between memory and register
  - **`movq %eax, (%ebx)`**
- *Control Instruction*: Alter the sequence of instructions (by changing PC)
  - **`jmp`**, **`call`**
  - C constructs: **`if-else`**, **`do-while`**, function call, etc.

Today: Compute and Control Instructions

- Move operations (and addressing modes)
- Arithmetic & logical operations
- Condition Codes
- Control: Conditional branches (`if`… `else`…)
- Control: Loops (`for`, `while`)
- Control: Switch Statements (`case`… `switch`…)

Data Movement Instruction Example

```
movq    %rdx, (%rdi)
```

- Semantics:
  - Move (really, **copy**) data in register **`%rdx`** to memory location whose address is the value stored in **`%rdi`**
  - Pointer dereferencing

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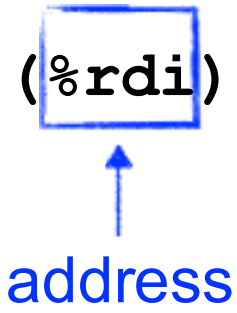

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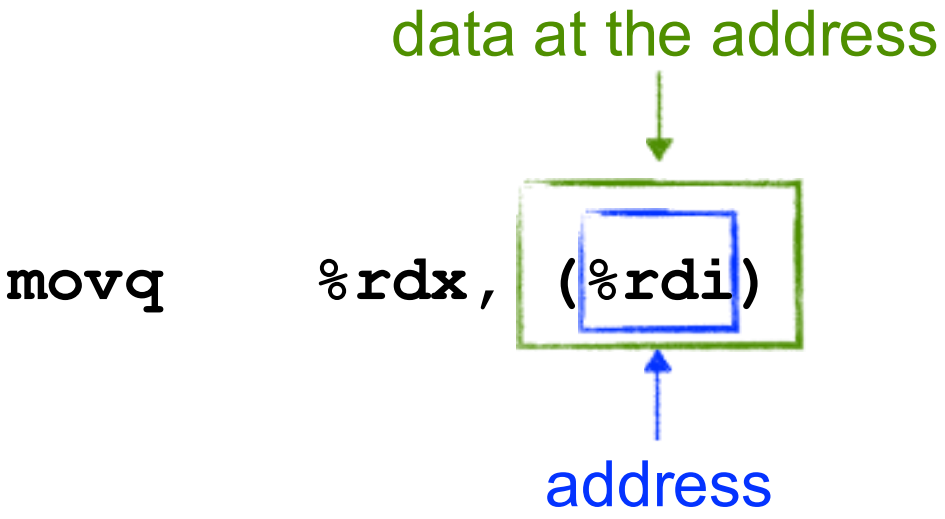

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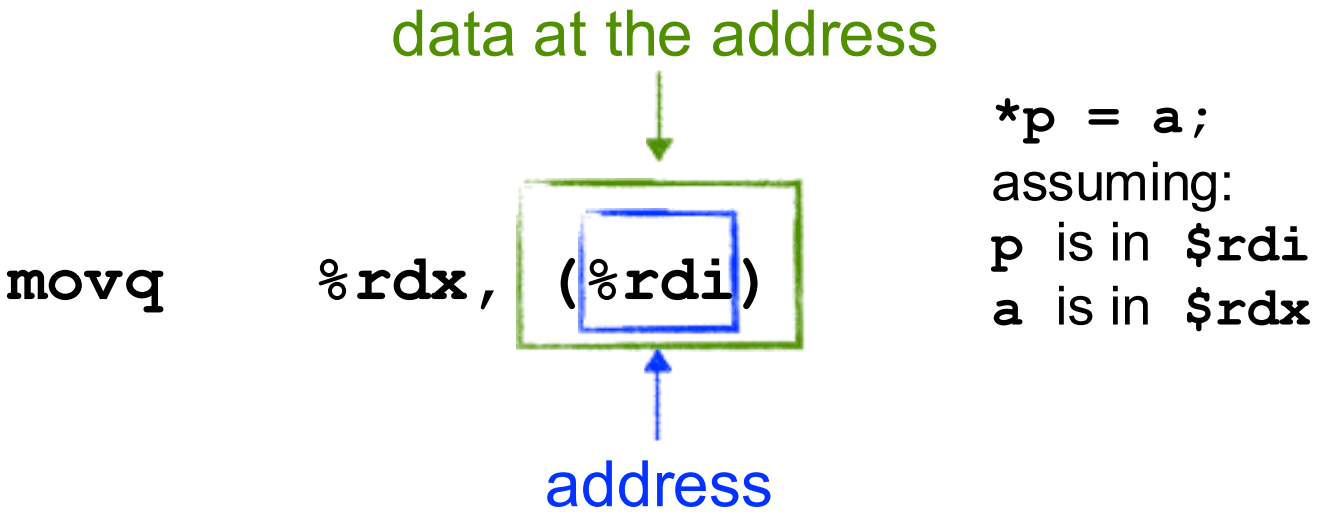

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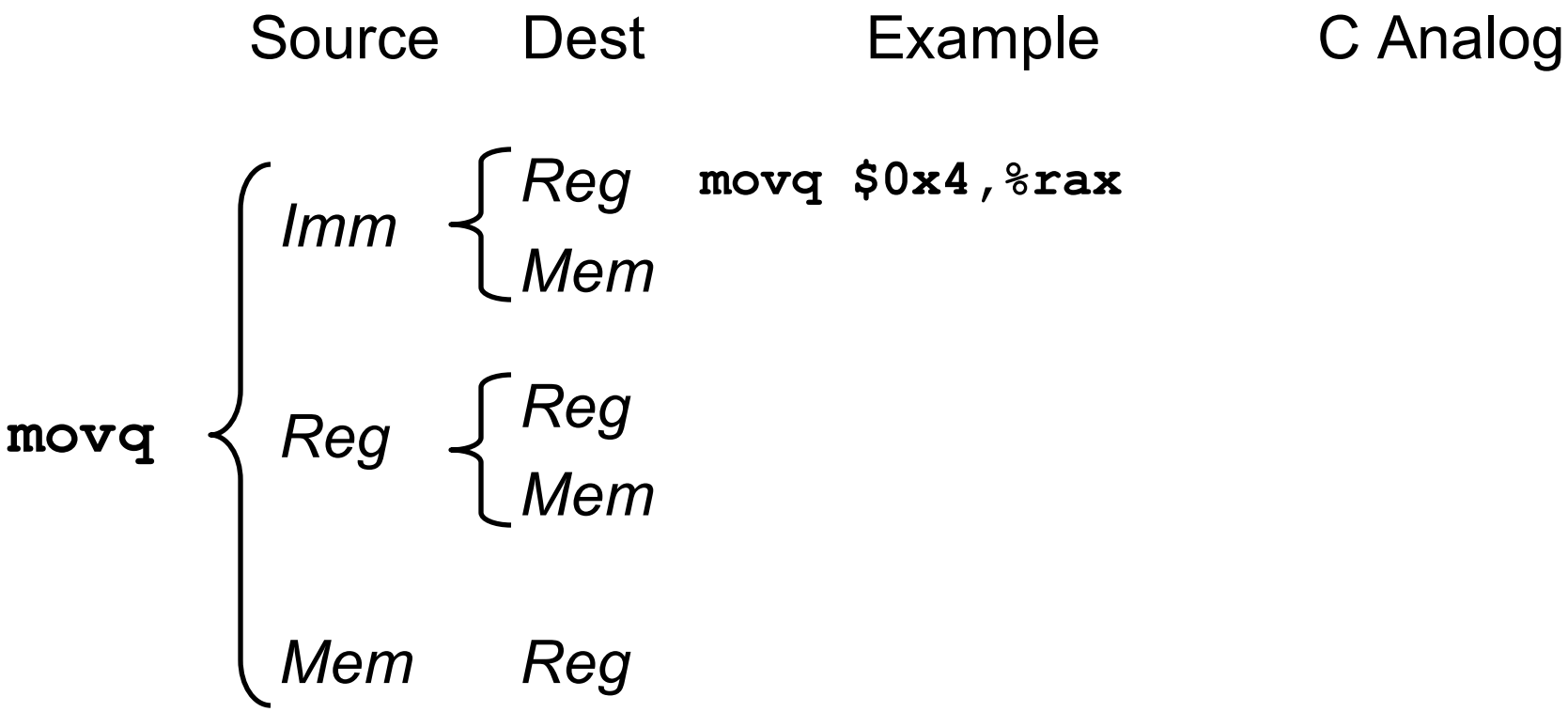
  - How to obtain the address is called "addressing mode"
- Register:
  - Example: **`%rax, %r13`**
  - But **`%rsp`** reserved for special use
- Immediate: Constant integer data
  - Example: **`$0x400`**, **`$-533;`** like C constant, but prefixed with '**`$`**'
  - Encoded with 1, 2, or 4 bytes; can only be source

`movq` Operand Combinations

	Source	Dest	Example	C Analog
movq	*Imm*	*Reg*		
		Mem		
	Reg	*Reg*		
		Mem		
	Mem	*Reg*		

Cannot do memory-memory transfer with a single instruction in x86.

`movq` Operand Combinations



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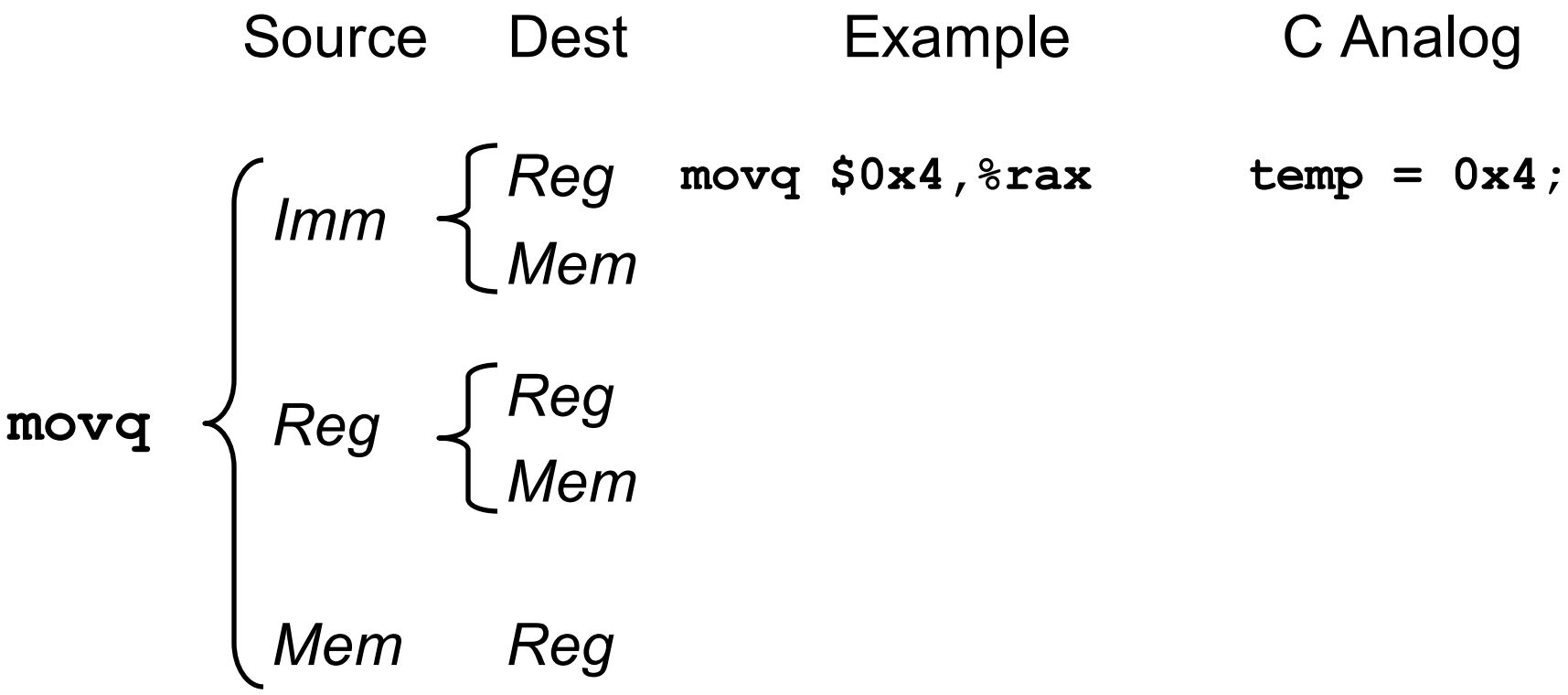

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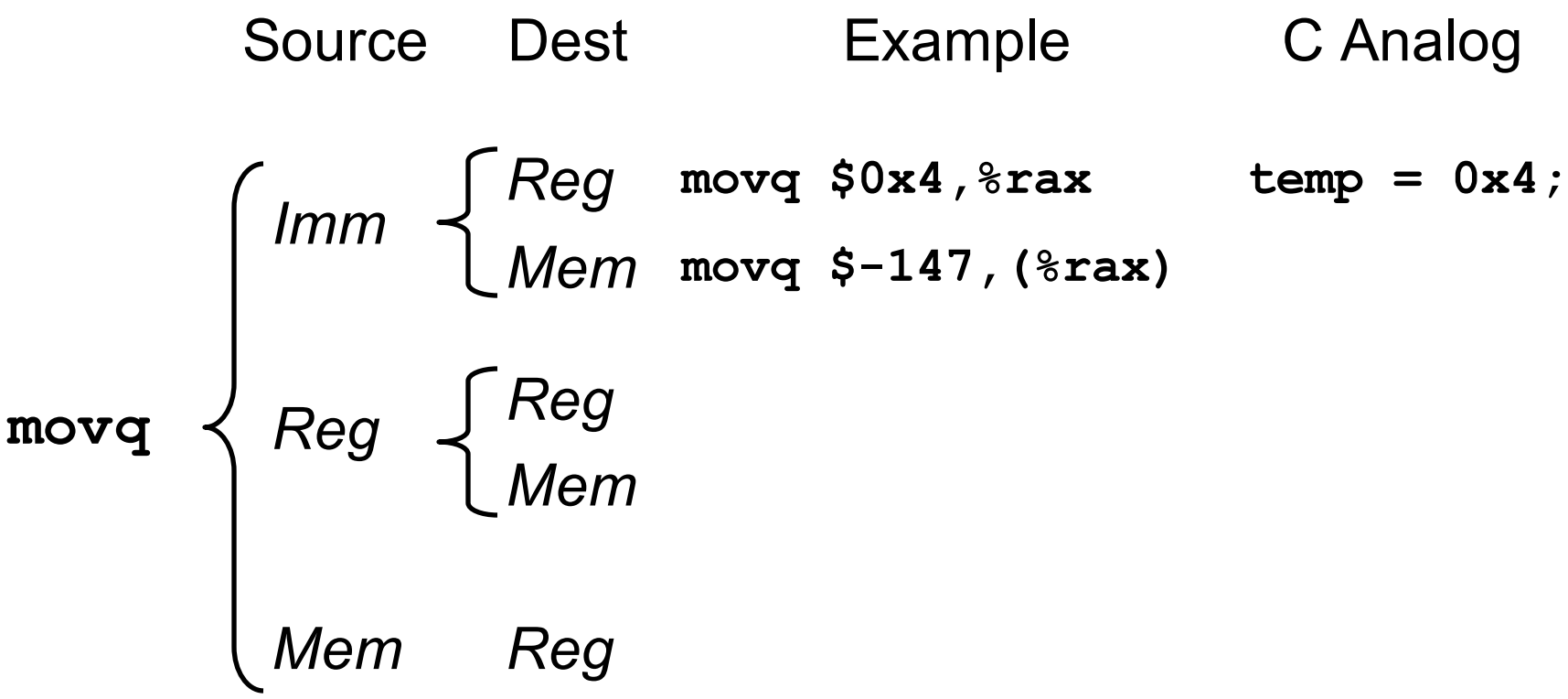

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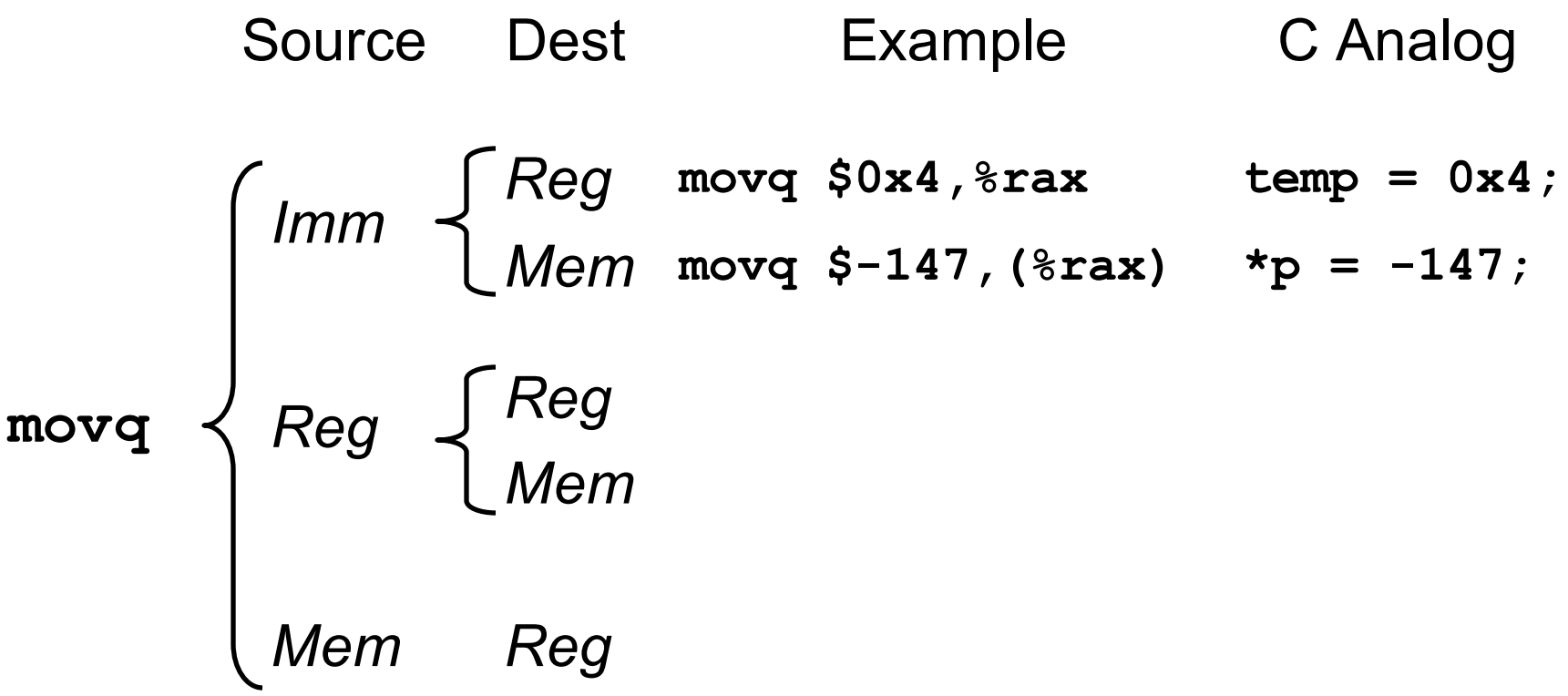

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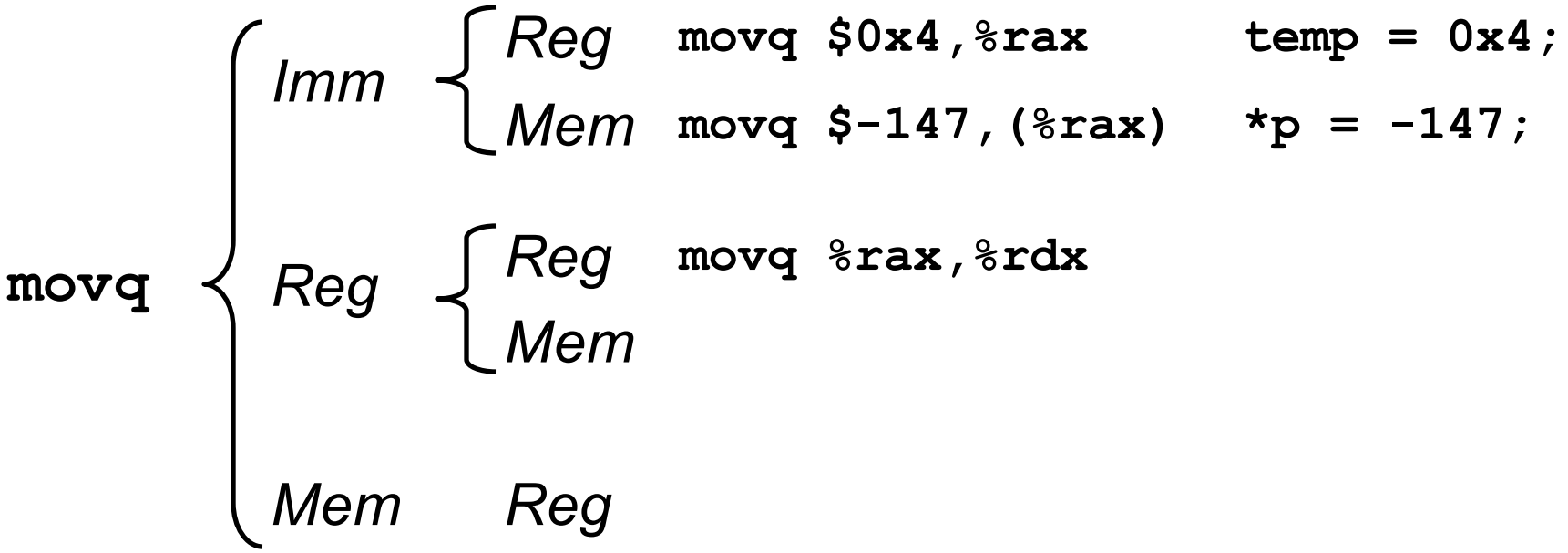

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	Reg	*Reg*	`movq %rax,%rdx`	`temp2 = temp1;`
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Example of Simple Addressing Modes

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void swap
    (long *xp, long *yp)
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  long t0 = *xp;
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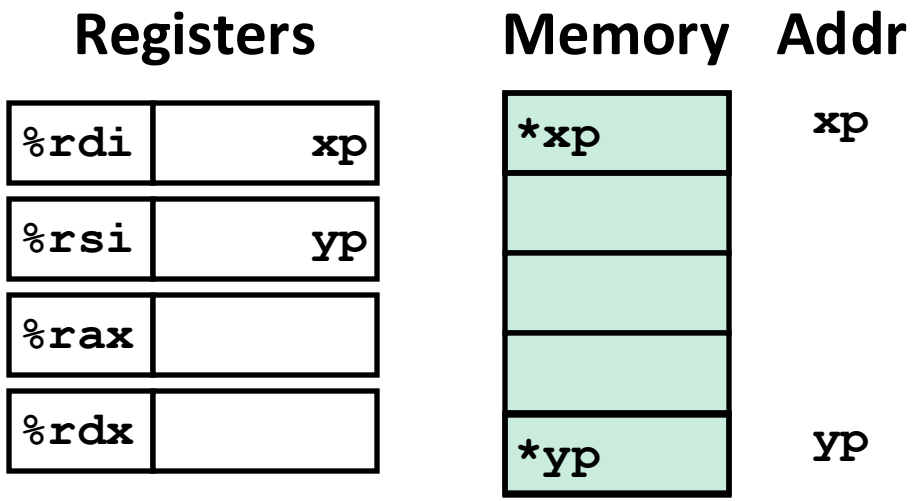

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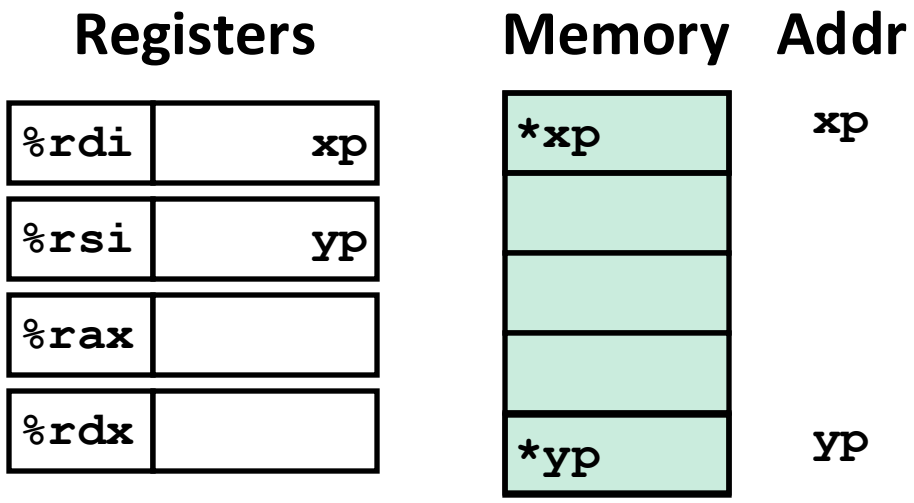


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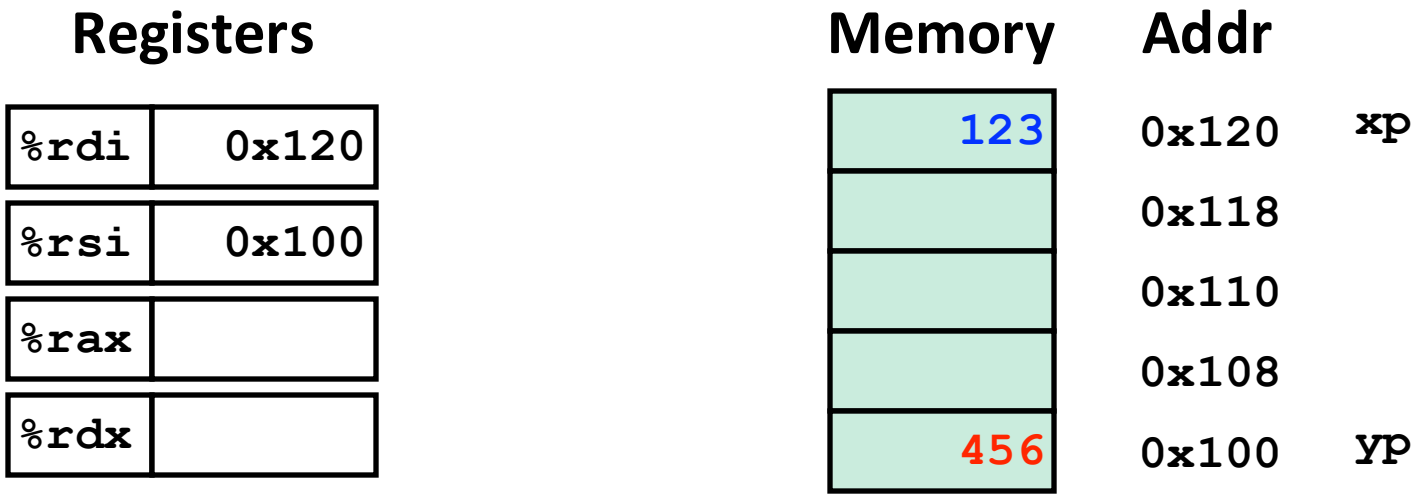
Understanding `Swap()`

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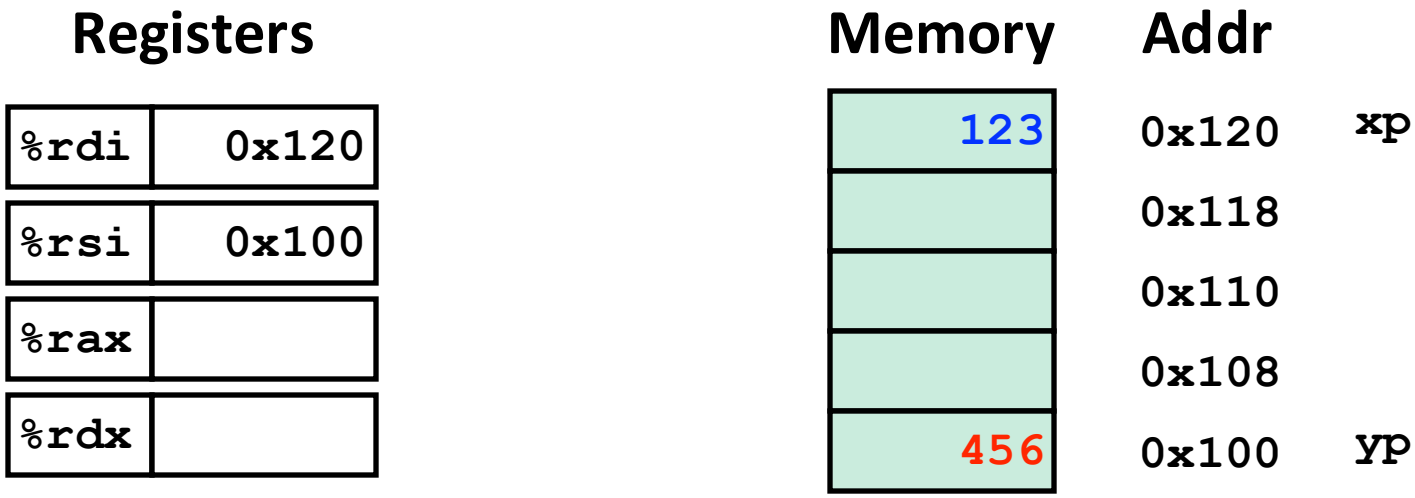


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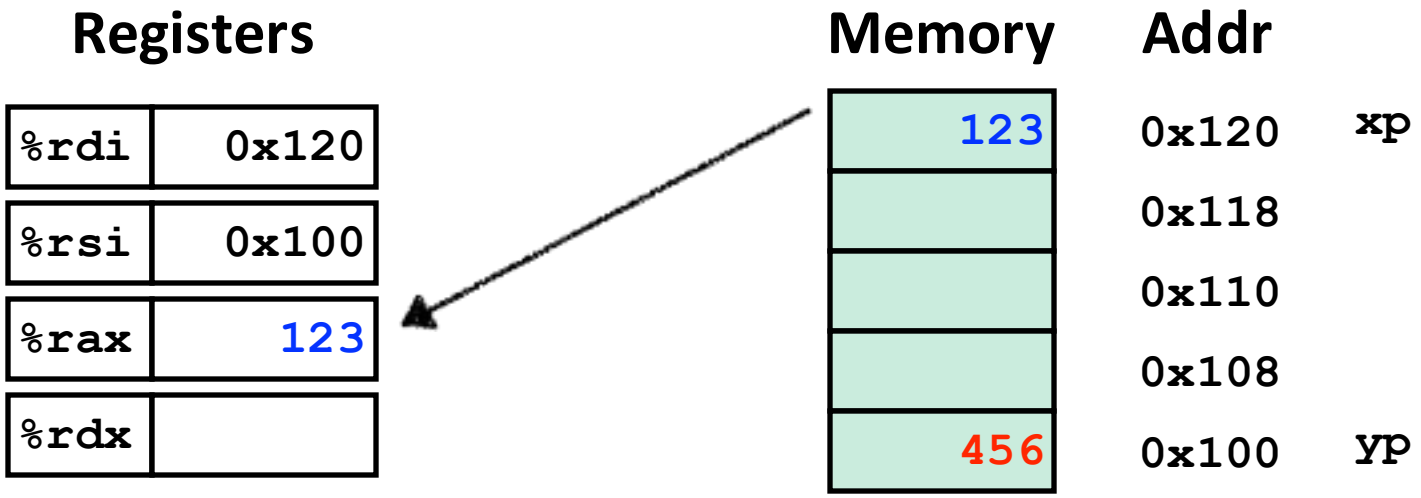


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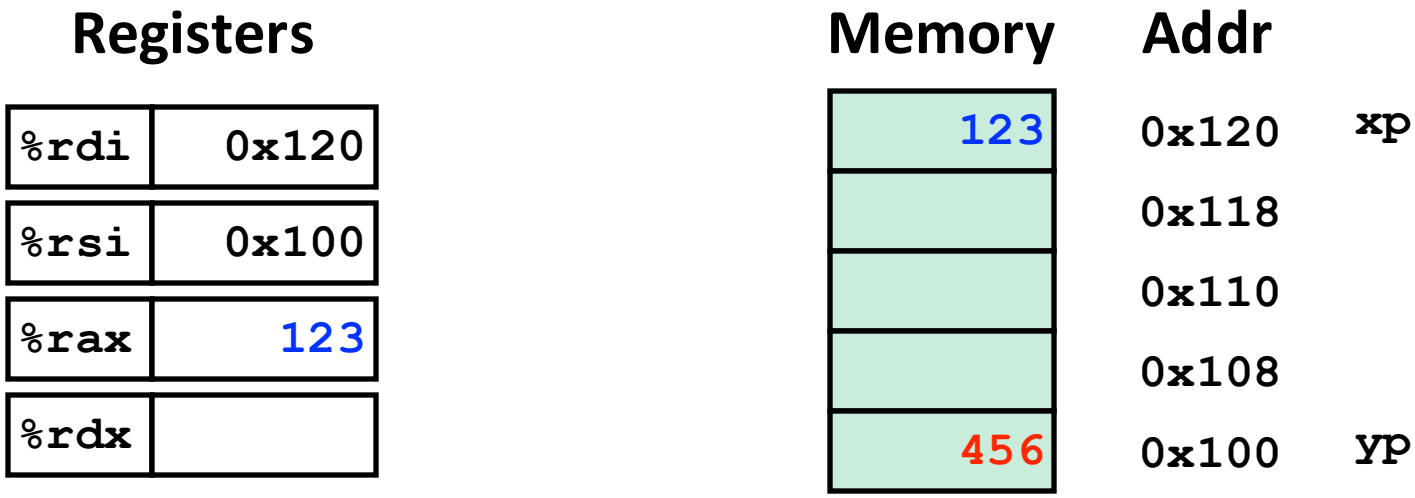


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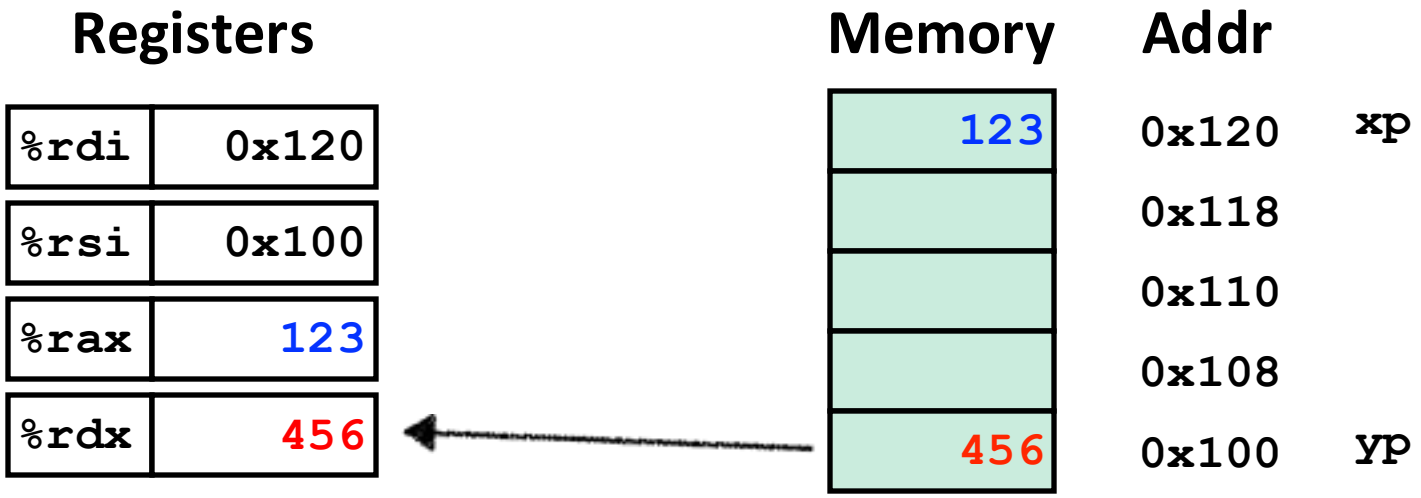


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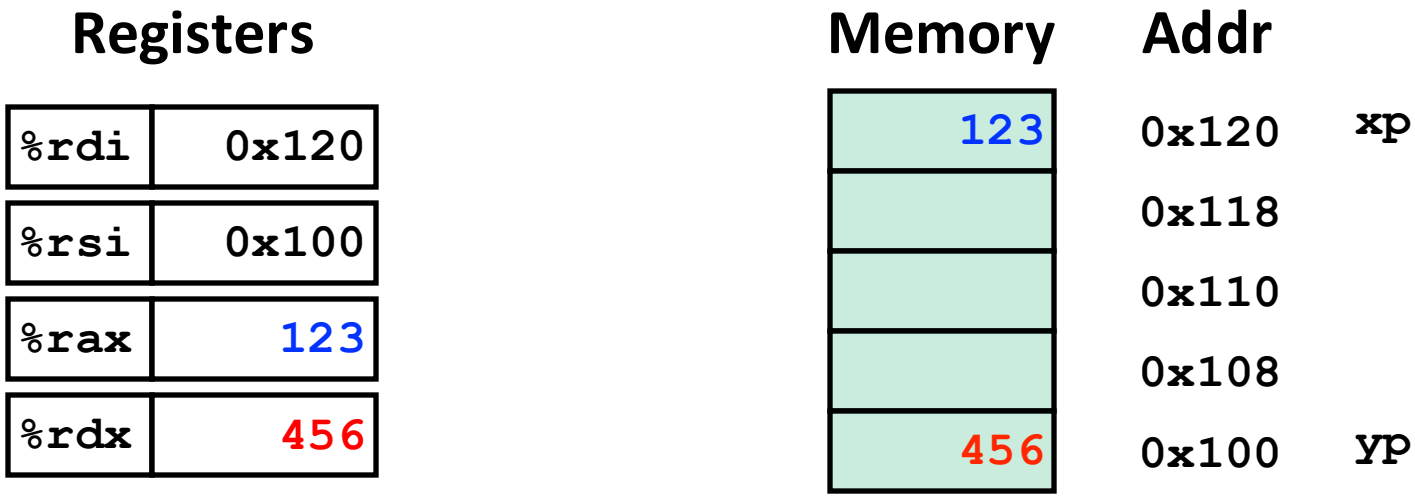


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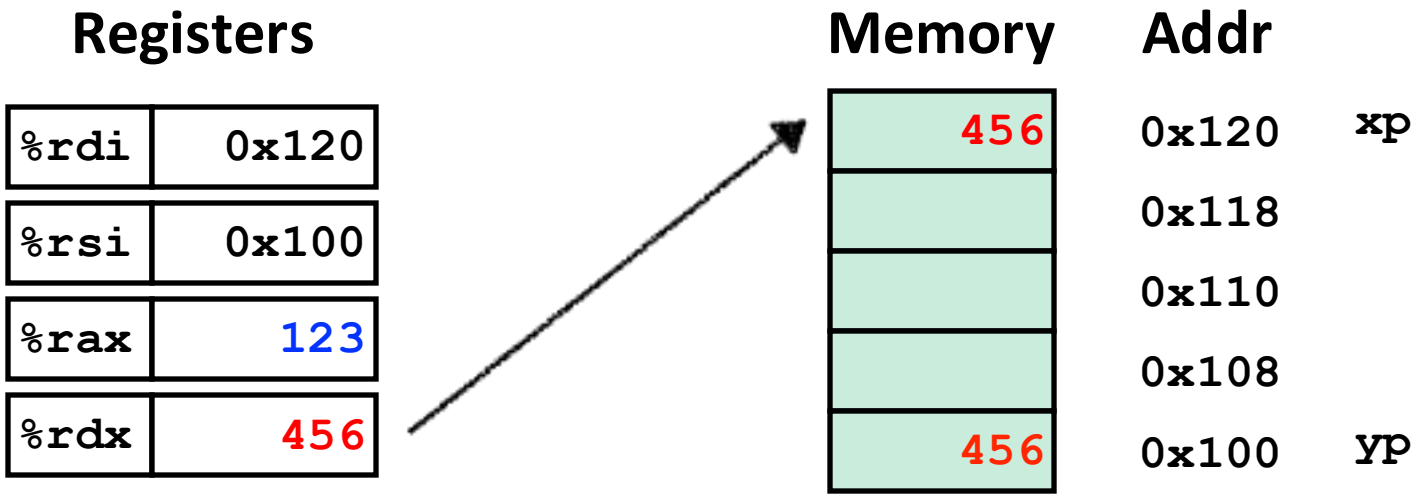


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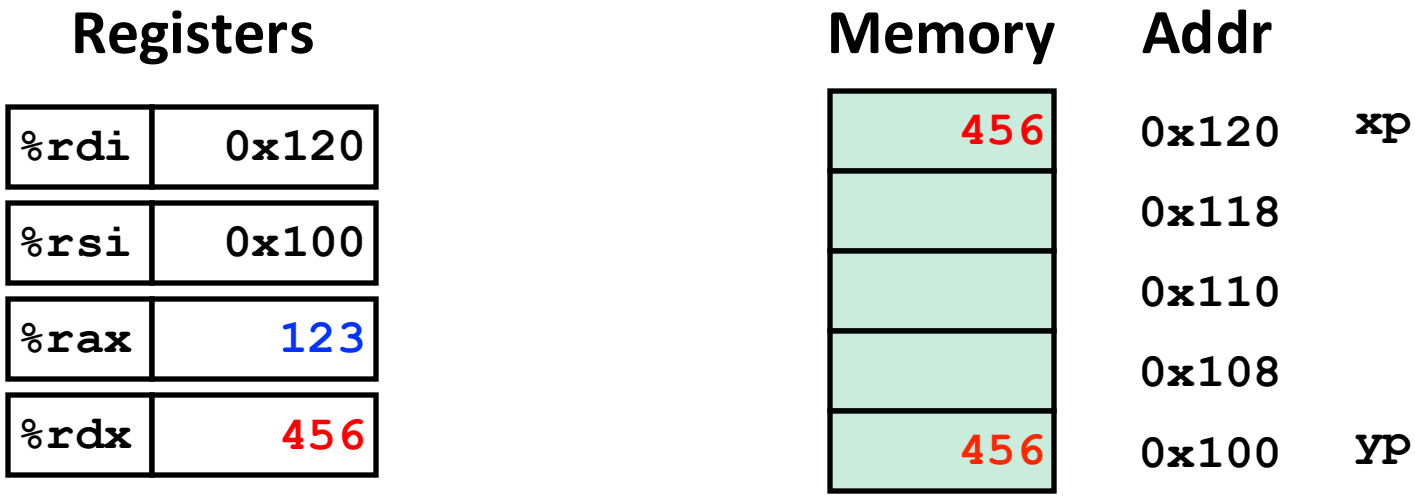


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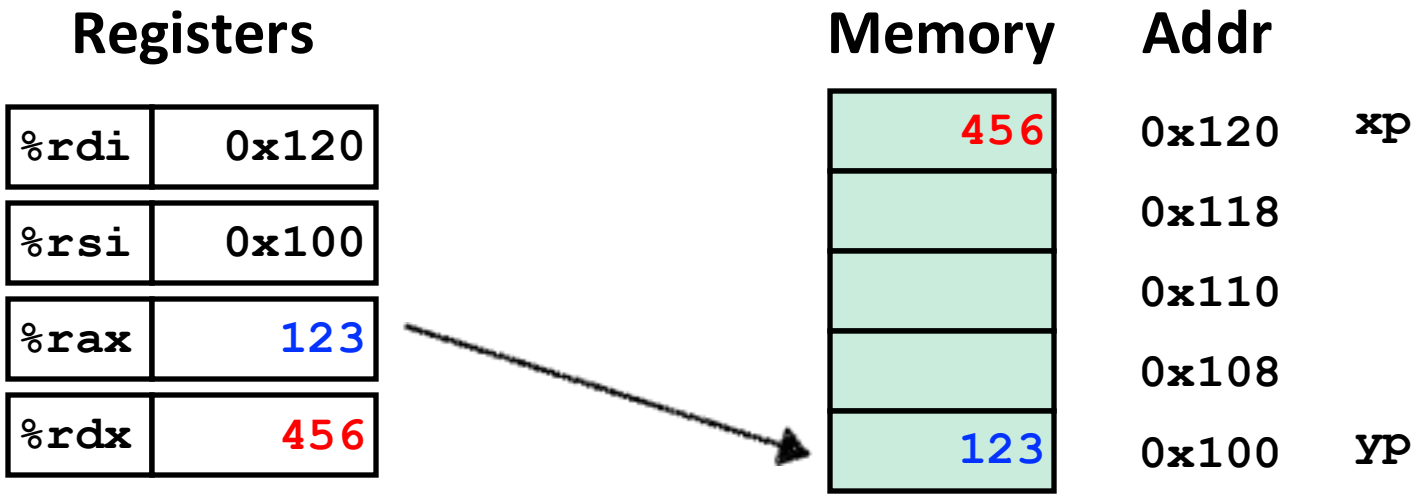
    movq    %rax, (%rsi)  # *yp = t0
    ret
```

Understanding `Swap()`




```
swap:
    movq    (%rdi), %rax  # t0 = *xp
    movq    (%rsi), %rdx  # t1 = *yp
    movq    %rdx, (%rdi)  # *xp = t1
    movq    %rax, (%rsi)  # *yp = t0
    ret
```

Memory Addressing Modes

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  - Pointer dereferencing in C

```
movq (%rcx),%rax; // address = %rcx
```

- Displacement: D(R)
  - Memory address: **Reg[R]+D**
  - Register R specifies start of memory region
  - Constant displacement D specifies offset

```
movq 8(%rbp),%rdx; // address = %rbp + 8
```

Complete Memory Addressing Modes

- The General Form: D(Rb,Ri,S)
  - Memory address: Reg[Rb] + S * Reg[Ri] + D
  - E.g., **`8(%eax, %ebx, 4)`**; // address = **`%eax`** + 4 * **`%ebx`** + 8
  - D: Constant "displacement"
  - Rb: Base register: Any of 16 integer registers
  - Ri: Index register: Any, except for %rsp
  - S: Scale: 1, 2, 4, or 8

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- What is **`8(%eax, %ebx, 4)`** used for?
- Special Cases

(Rb,Ri)	address = Reg[Rb]+Reg[Ri]
D(Rb,Ri)	address = Reg[Rb]+Reg[Ri]+D
(Rb,Ri,S)	address = Reg[Rb]+S*Reg[Ri]

Address Computation Examples

`%rdx`	`0xf000`
`%rcx`	`0x0100`

Expression	Address Computation	Address
`0x8(%rdx)`		
`(%rdx,%rcx)`		
`(%rdx,%rcx,4)`		
`0x80(,%rdx,2)`		

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`0x80(,%rdx,2)`	`2*0xf000 + 0x80`	`0x1e080`

Address Computation Instruction

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leaq 4(%rsi,%rdi,2), %rax
```

Address Computation Instruction

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  - *Src* is address mode expression
  - Set *Dst* to address denoted by expression
  - No actual memory reference is made
- Uses
  - Computing addresses without a memory reference
    - E.g., translation of p = &x[i];

Address Computation Instruction

- Interesting Use
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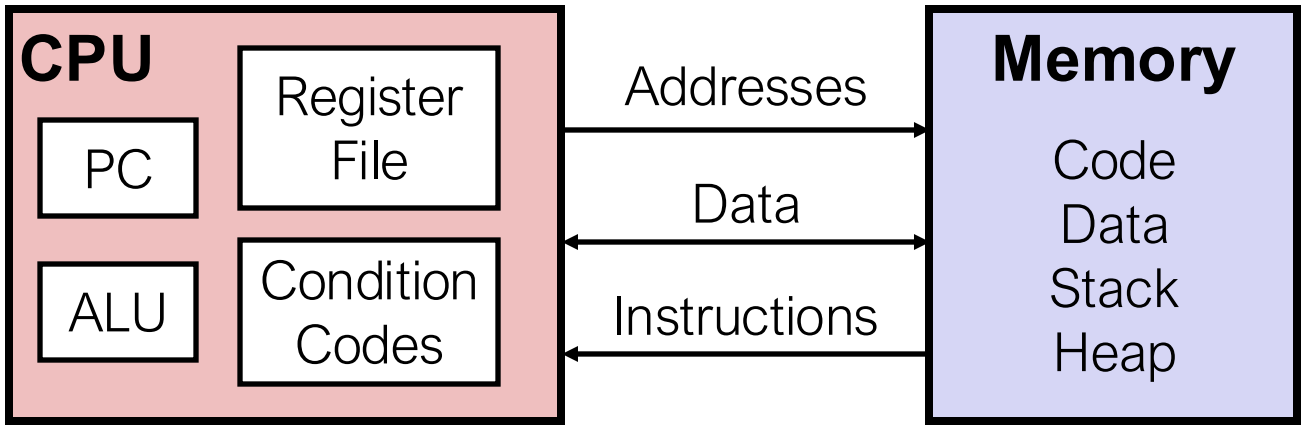
Converted to
assembly by compiler:

```
leaq (%rdi,%rdi,2), %rax # t <- x+x*2
salq $2, %rax            # return t<<2
```

Assembly Program Instructions

Assembly Programmer's Perspective of a Computer



- *Data Movement Instruction*: Transfer data between memory and register
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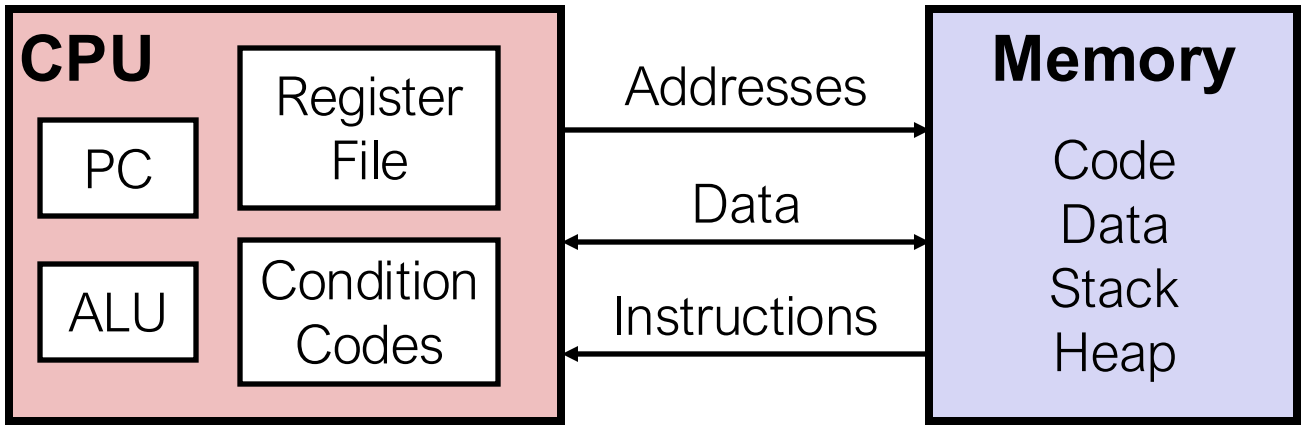

- *Data Movement Instruction*: Transfer data between memory and register
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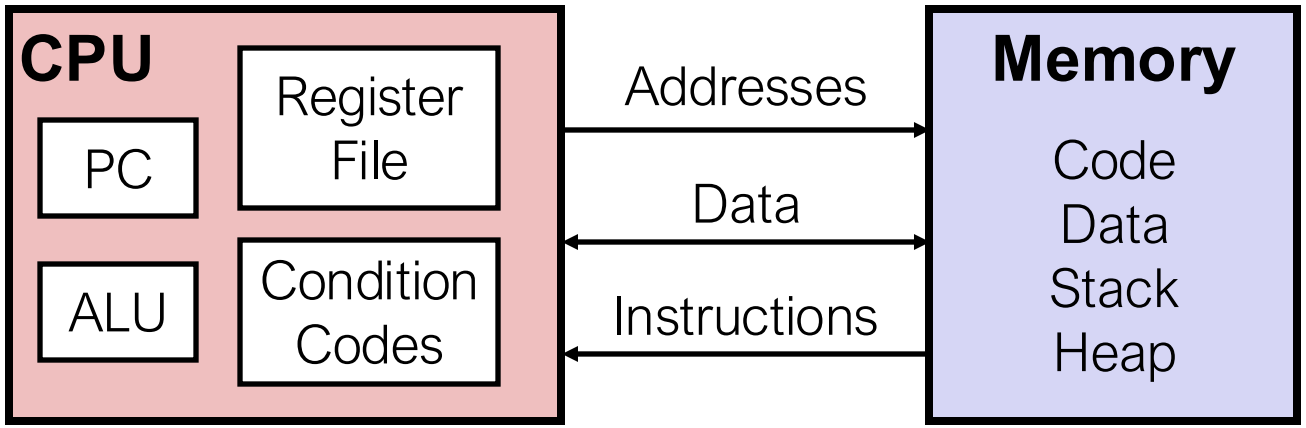

- *Data Movement Instruction*: Transfer data between memory and register
  - **`movq %eax, (%ebx)`**
- *Compute Instruction*: Perform arithmetics on register or memory data
  - **`addq %eax, %ebx`**
  - C constructs: +, -, >>, etc.
- *Control Instruction*: Alter the sequence of instructions (by changing PC)
  - **`jmp`**, **`call`**
  - C constructs: **`if-else`**, **`do-while`**, function call, etc.

Today: Compute and Control Instructions

- Move operations (and addressing modes)
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Some Arithmetic Operations (2 Operands)

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`addq` `src, dest`	Dest = Dest + Src	

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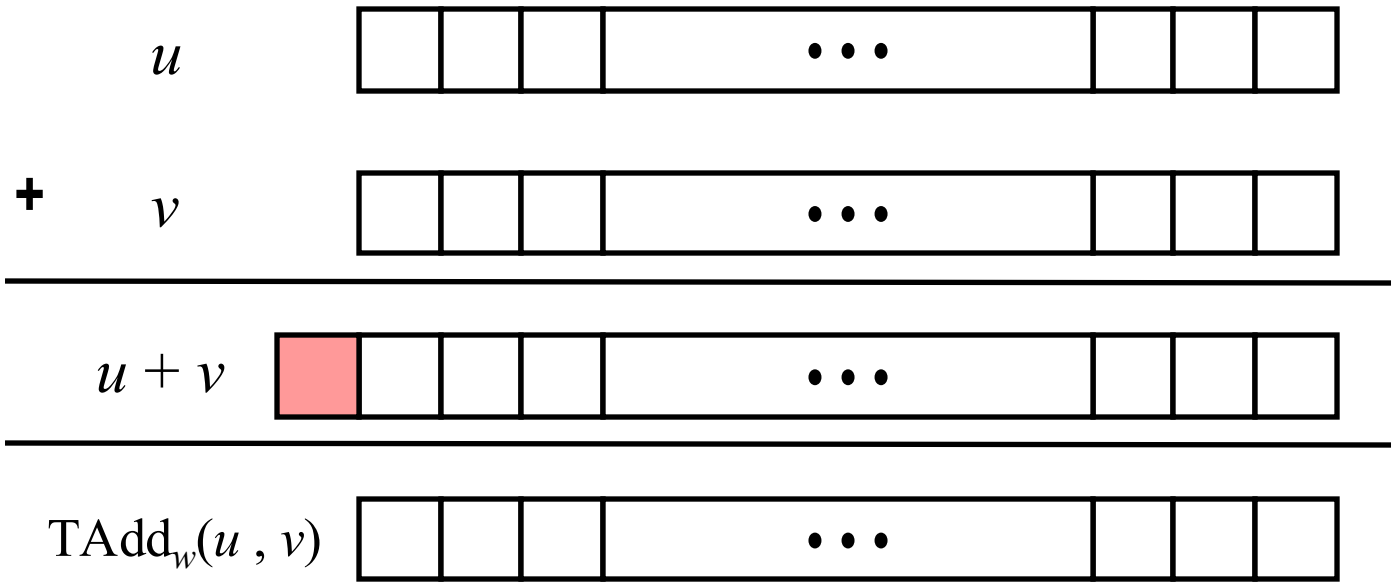

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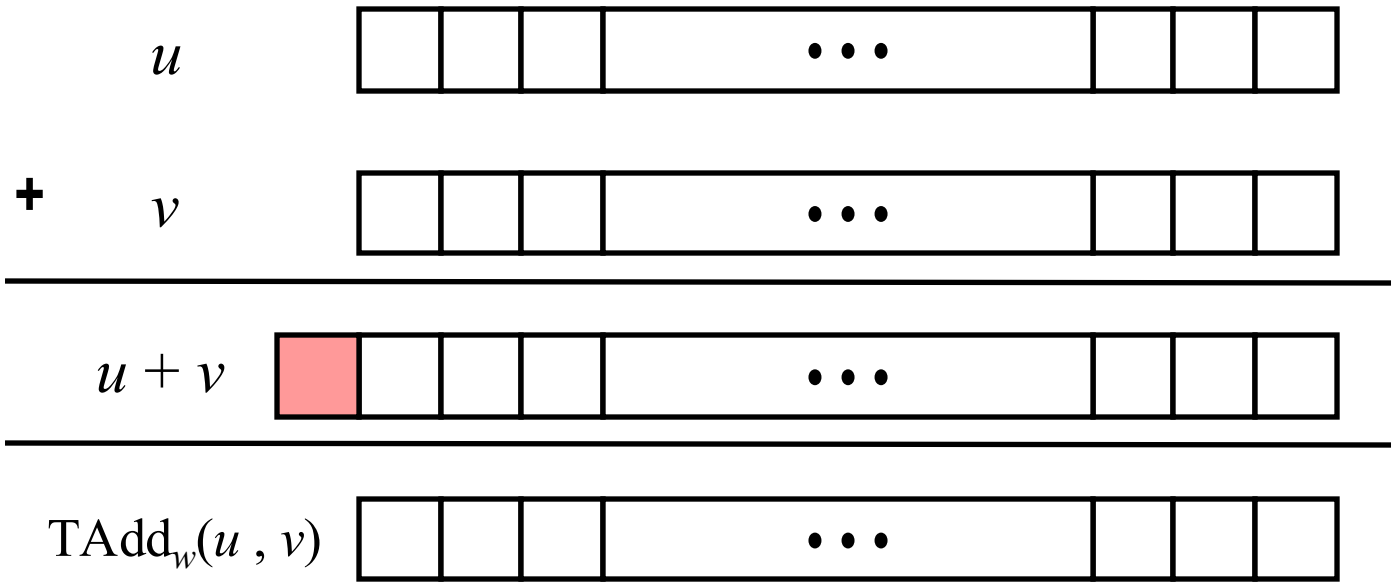

addq %rax, %rbx

%rbx = %rax + %rbx

Truncation if overflow,
set carry bit (more later…)

Some Arithmetic Operations (2 Operands)

Format	Computation	Notes
addq src, dest	Dest = Dest + Src	
subq src, dest	Dest = Dest - Src	
imulq src, dest	Dest = Dest * Src	
salq src, dest	Dest = Dest << Src	Also called **shlq**
sarq src, dest	Dest = Dest >> Src	Arithmetic shift
shrq src, dest	Dest = Dest >> Src	Logical shift
xorq src, dest	Dest = Dest ^ Src	
andq src, dest	Dest = Dest & Src	
orq src, dest	Dest = Dest | Src	

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  - Bit level behaviors for signed and unsigned arithmetic are exactly the same — assuming truncation

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```
long signed_add
(long x, long y)
{
  long res = x + y;
  return res;
}
```

```
 #x in %rdx, y in %rax
 addq    %rdx, %rax
```

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```
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addq    %rdx, %rax
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Bit-level

```
   010
+) 101
-------
   111
```

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Bit-level	**Signed**
010	2
+) 101	+) -3
111	-1

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Bit-level	Signed	Unsigned
010	2	2
+) 101	+) -3	+) 5
111	-1	7

```
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(long x, long y)
{
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  return res;
}
```

```
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addq    %rdx, %rax
```

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  return res;
}
```

```
#x in %rdx, y in %rax
addq    %rdx, %rax
```

Some Arithmetic Operations (1 Operand)

- Unary Instructions (one operand)

Format	Computation
`incq` `dest`	Dest = Dest + 1
`decq` `dest`	Dest = Dest - 1
`negq` `dest`	Dest = -Dest
`notq` `dest`	Dest = ~Dest

Arithmetic Expression Example

```
long arith
(long x, long y, long z)
{
  long t1 = x+y;
  long t2 = z+t1;
  long t3 = x+4;
  long t4 = y * 48;
  long t5 = t3 + t4;
  long rval = t2 * t5;
  return rval;
}
```

```
arith:
  leaq    (%rdi,%rsi), %rax
  addq    %rdx, %rax
  leaq    (%rsi,%rsi,2), %rdx
  salq    $4, %rdx
  leaq    4(%rdi,%rdx), %rcx
  imulq   %rcx, %rax
  ret
```

Interesting Instructions

- `leaq`: address computation
- `salq`: shift
- `imulq`: multiplication
  - But, only used once

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  leaq    4(%rdi,%rdx), %rcx   # t5
  imulq   %rcx, %rax           # rval
  ret
```

Register	Use(s)
%rdi	Argument x
%rsi	Argument y
%rdx	Argument z
%rax	t1, t2, rval
%rdx	t4
%rcx	t5

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- Condition Codes
- Control: Conditional branches (if… else…)
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- **ZF** set if %rax + %rbx == 0

ZF set when

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SF set when

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Bit-level

```
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+) 010
------
  1001
```

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Bit-level	**Signed**
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1001	1

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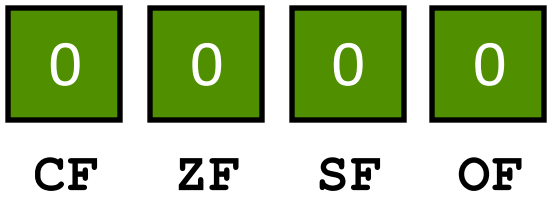
Bit-level	Signed	Unsigned
111	-1	7
+) 010	+) 2	+) 2
1001	1	9



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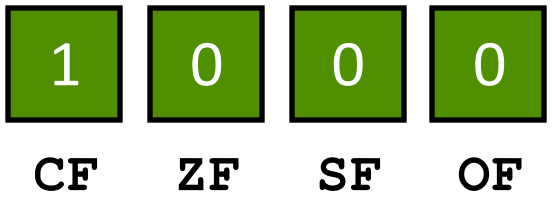

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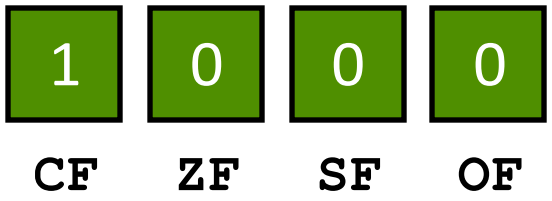

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Bit-level

```
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+) 001
-------
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Bit-level	Signed
011	3
+) 001	+) 1
100	-4

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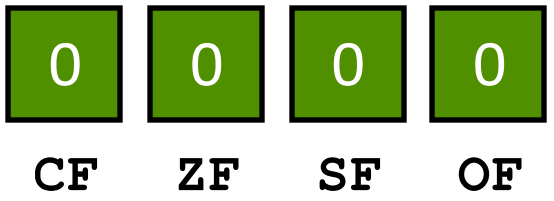
Bit-level	Signed	Unsigned
011	3	3
+) 001	+) 1	+) 1
100	-4	4



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`addq %rax, %rbx`

Arithmetic instructions implicitly set condition codes (think of it as side effect)

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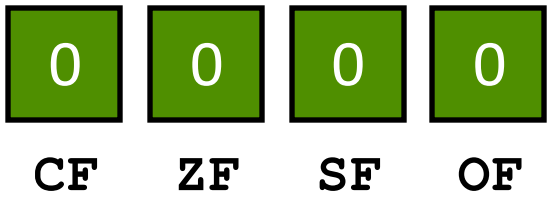

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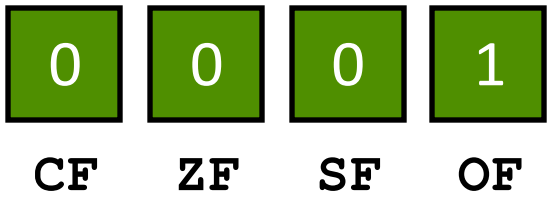

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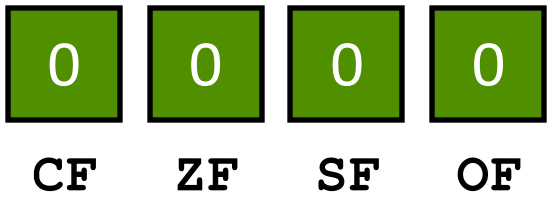
```
   100
+) 111
-------
  c011
```



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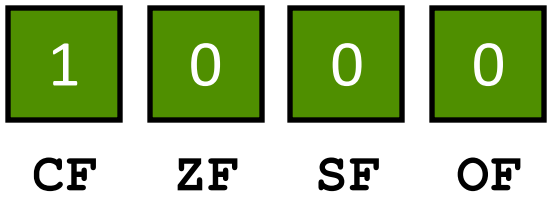

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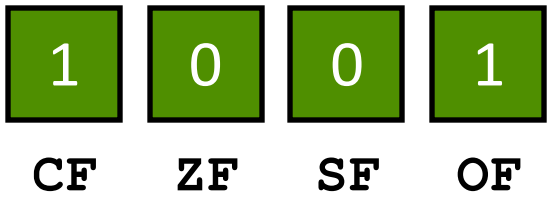

Compare Instruction

- **`cmpq a, b`**
  - Computes $b - a$ (just like **sub**)
  - Sets condition codes based on result, but…
  - **Does not change b**
  - All it does is setting condition codes!

How Should **`cmpq`** Set Condition Codes?

```
cmpq    %rsi, %rdi
```

```
cmpq 0xFF, 0x80
```

How Should **`cmpq`** Set Condition Codes?

`cmpq` **`%rsi, %rdi`**

`cmpq` *0xFF, 0x80*

```
   10000000      -128
-) 11111111   -)   -1
   --------   --------
   10000001      -127
```

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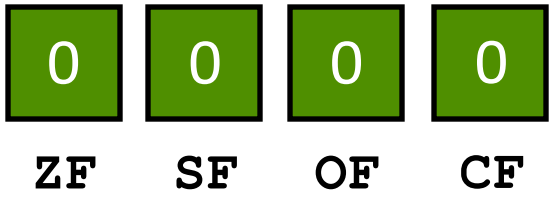

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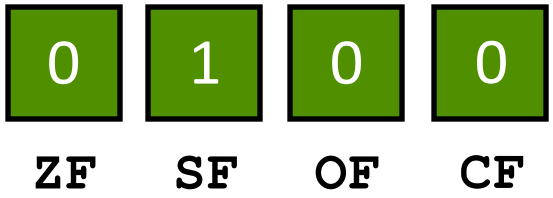

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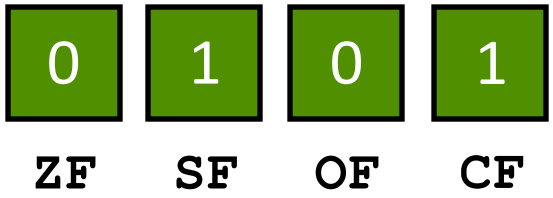

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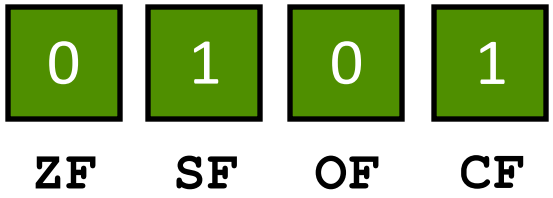

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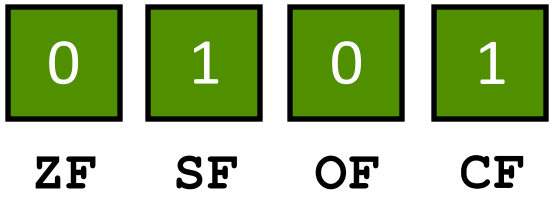

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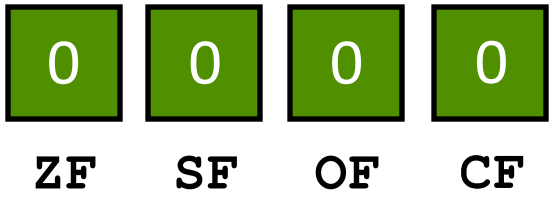

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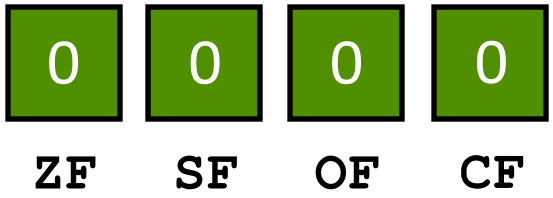

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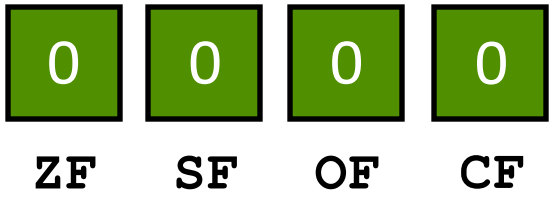

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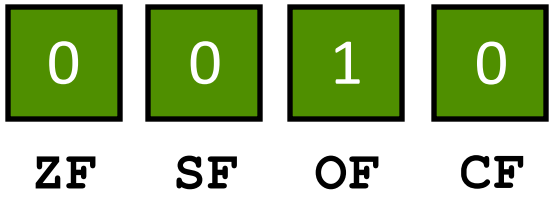

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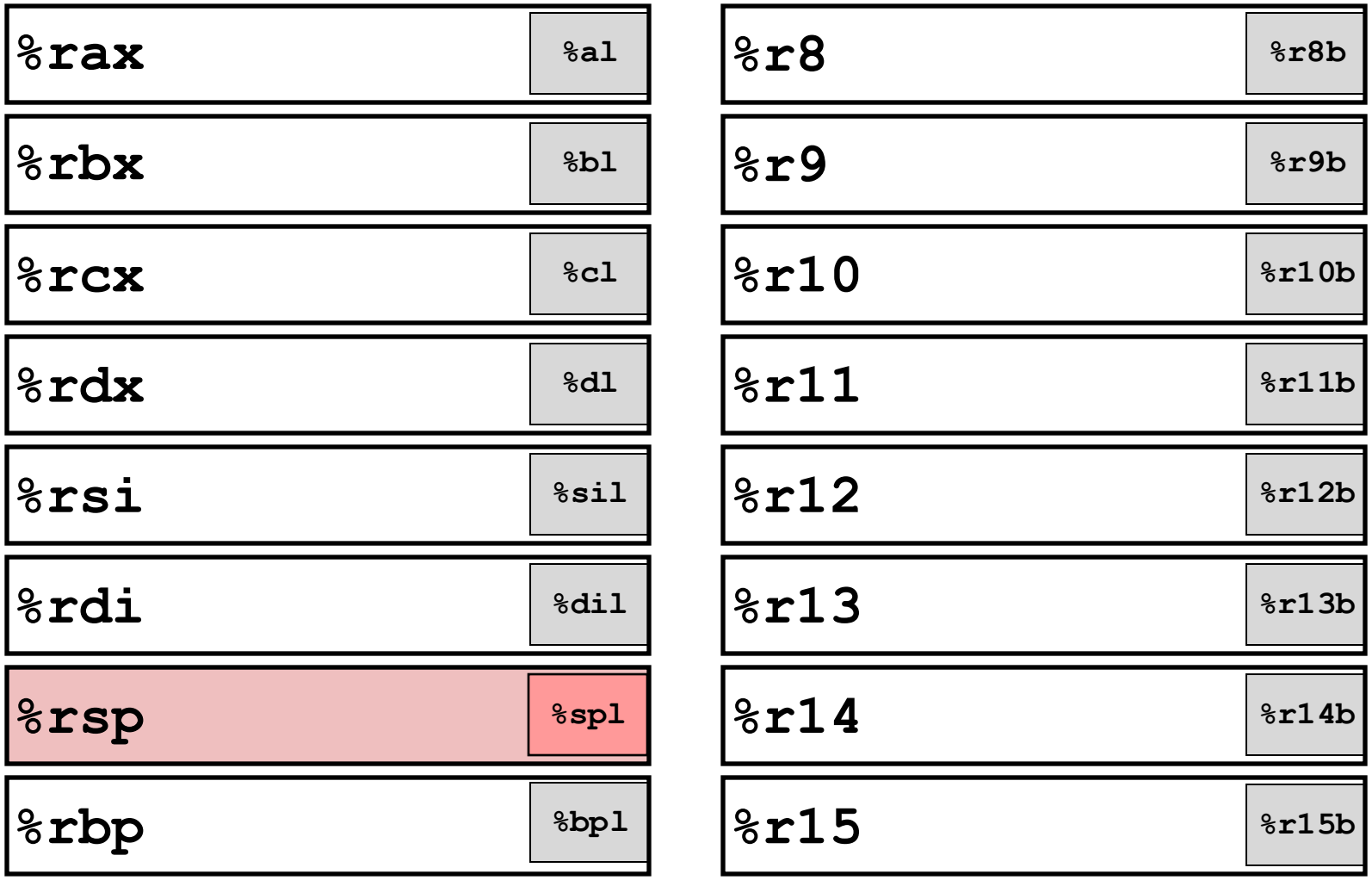
Reading Condition Codes

- SetX Instructions
  - Set low-order byte of destination to 0 or 1 based on combinations of condition codes
  - Does not alter remaining 7 bytes

SetX	Condition	Description
`sete`	`ZF`	Equal / Zero
`setne`	`~ZF`	Not Equal / Not Zero
`sets`	`SF`	Negative
`setns`	`~SF`	Nonnegative
`setg`	`~(SF^OF)&~ZF`	Greater (Signed)
`setge`	`~(SF^OF)`	Greater or Equal (Signed)
`setl`	`(SF^OF)`	Less (Signed)
`setle`	`(SF^OF)|ZF`	Less or Equal (Signed)
`seta`	`~CF&~ZF`	Above (unsigned)
`setb`	`CF`	Below (unsigned)

x86-64 Integer Registers



- SetX argument is always a low byte (%al, %r8b, etc.)

Reading Condition Codes (Cont.)

- **`SetX` Instructions:**
  - Set single byte based on combination of condition codes
- One of addressable byte registers
  - Does not alter remaining bytes
  - Typically use **`movzbl`** to finish job
    - 32-bit instructions also set upper 32 bits to 0

```
int gt (long x, long y)
{
  return x > y;
}
```

Register	Use(s)
`%rdi`	Argument `x`
`%rsi`	Argument `y`
`%rax`	Return value

```
      cmpq   %rsi, %rdi    # Compare x:y
      setg   %al           # Set when >
      movzbl %al, %eax     # Zero rest of %rax
      ret
```

Reading Condition Codes (Cont.)

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  - Set single byte based on combination of condition codes
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ret
```

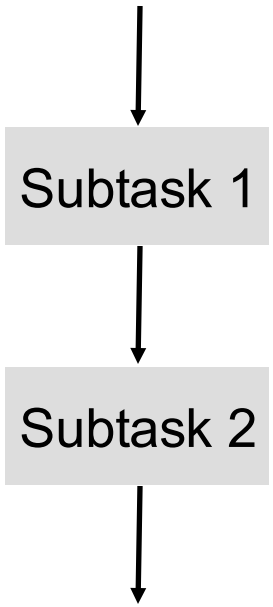
Today: Compute and Control Instructions

- Move operations (and addressing modes)
- Arithmetic & logical operations
- Condition Codes
- Control: Conditional branches (if… else…)
- Control: Loops (for, while)
- Control: Switch Statements (case… switch…)

Three Basic Programming Constructs

Three Basic Programming Constructs

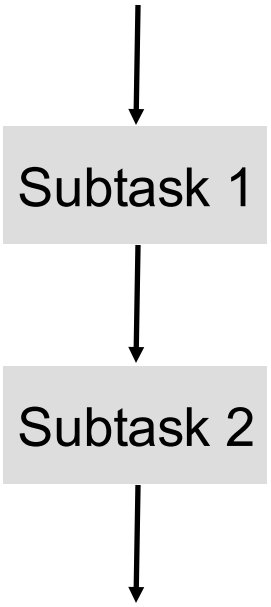
Sequential




```
a = x + y;
y = a - c;
…
```

Three Basic Programming Constructs

Sequential

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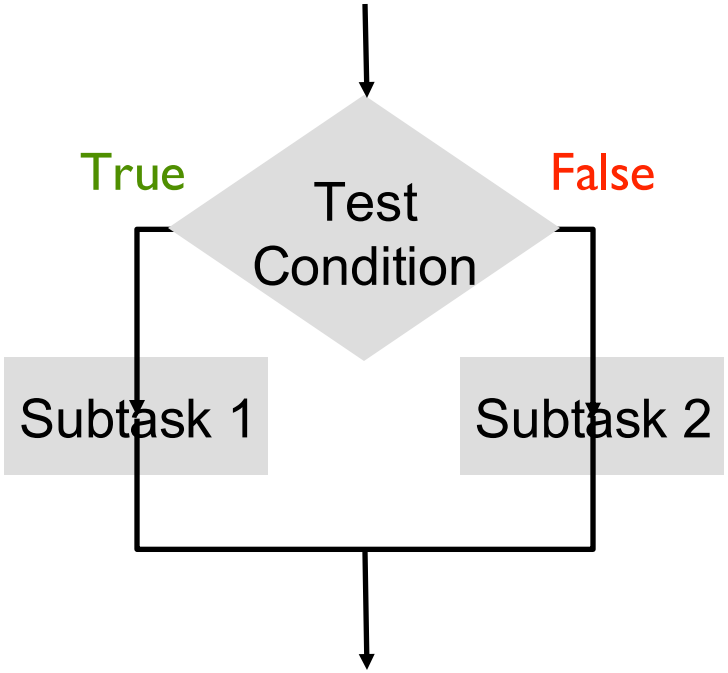
Conditional




```
if (x > y) r = x - y;
else r = y - x;
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Three Basic Programming Constructs

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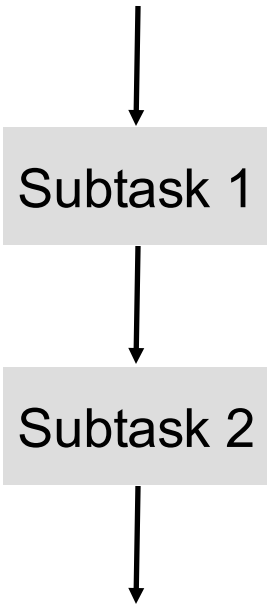


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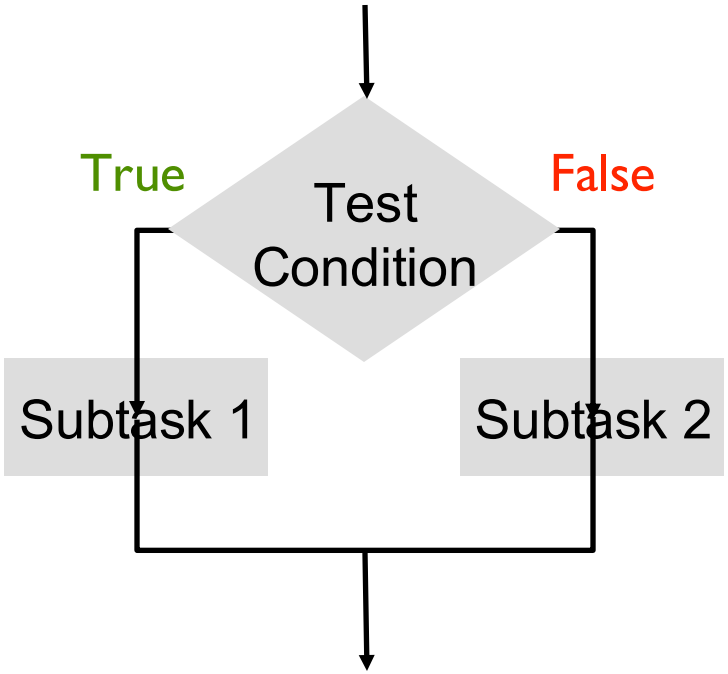


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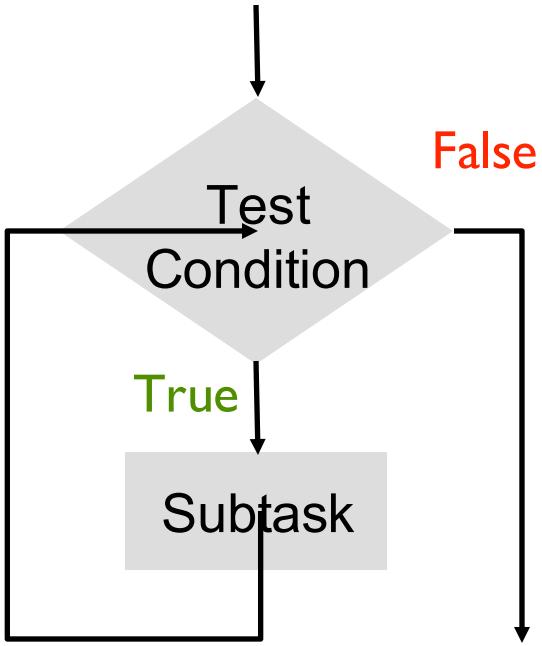
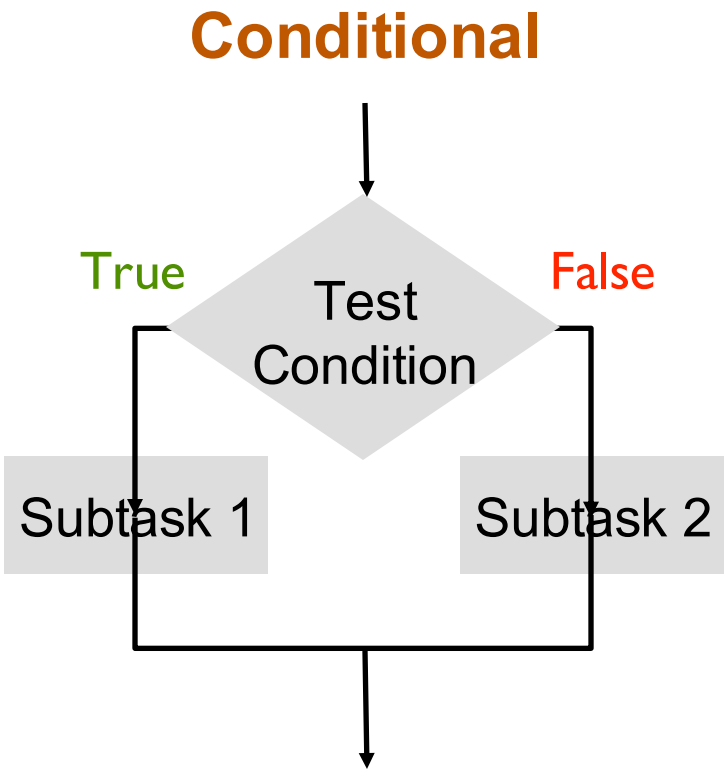
```

Iterative




```
while (x > 0) {
  x--;
}
```

Three Basic Programming Constructs

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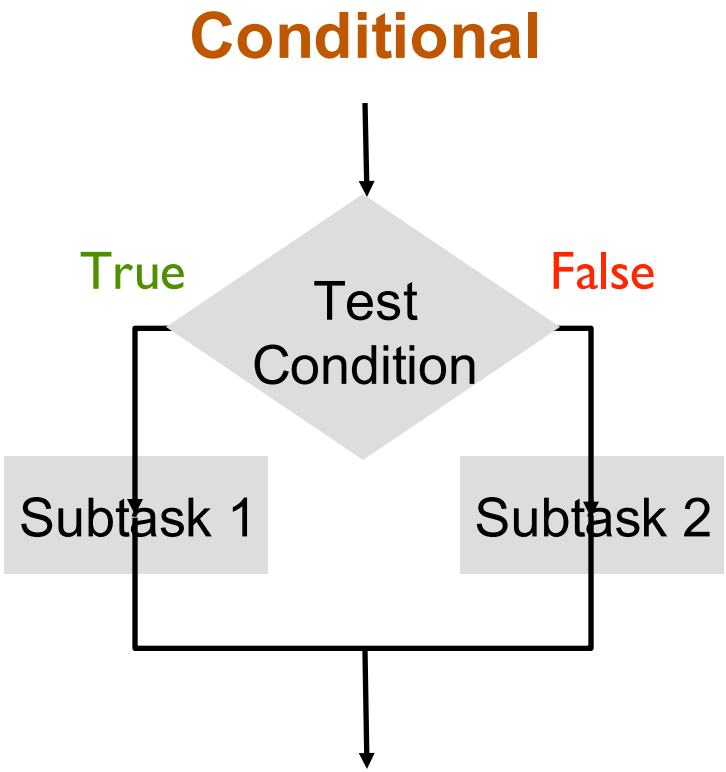
Three Basic Programming Constructs

- Both conditional and iterative programming requires altering the sequence of instructions (control flow)

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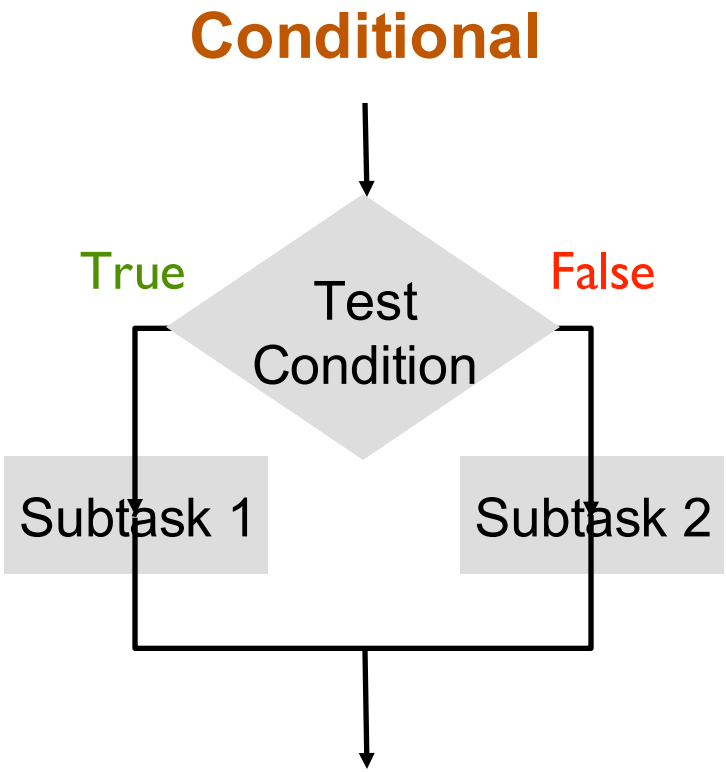


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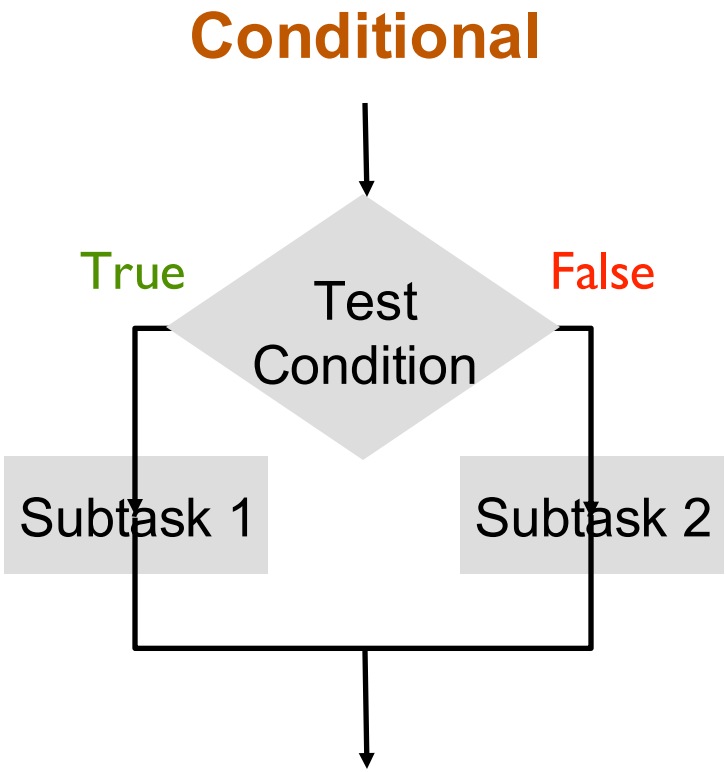
Three Basic Programming Constructs

- Both conditional and iterative programming requires altering the sequence of instructions (control flow)
- We need a set of *control instructions* to do so
- Two fundamental questions:
  - How to test condition and how to represent test results?
  - How to alter control flow according to the test results?




```
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```

Jumping

- `jX` Instructions
  - Jump to different part of code depending on condition codes

jX	Condition	Description
`jmp`	`1`	Unconditional
`je`	`ZF`	Equal / Zero
`jne`	`~ZF`	Not Equal / Not Zero
`js`	`SF`	Negative
`jns`	`~SF`	Nonnegative
`jg`	`~(SF^OF)&~ZF`	Greater (Signed)
`jge`	`~(SF^OF)`	Greater or Equal (Signed)
`jl`	`(SF^OF)`	Less (Signed)
`jle`	`(SF^OF)|ZF`	Less or Equal (Signed)
`ja`	`~CF&~ZF`	Above (unsigned)
`jb`	`CF`	Below (unsigned)

Conditional Branch Example

Conditional Branch Example

```
long absdiff
  (long x, long y)
{
  long result;
  if (x > y)
    result = x-y;
  else
    result = y-x;
  return result;
}
```

Conditional Branch Example

```
gcc –Og –S –fno-if-conversion control.c
```

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long absdiff
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```

```
absdiff:
    cmpq    %rsi,%rdi # x:y
    jle     .L4
    movq    %rdi,%rax
    subq    %rsi,%rax
    ret
.L4:                  # x <= y
    movq    %rsi,%rax
    subq    %rdi,%rax
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Register	Use(s)
%rdi	x
%rsi	y
%rax	Return value

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```

Labels are symbolic names used to refer to instruction addresses.

Conditional Branch Example

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```

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unsigned long absdiff
  (unsigned long x,
unsigned long y)
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    subq    %rsi,%rax
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    subq    %rdi,%rax
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Conditional Jump Instruction

```
cmpq    %rsi, %rdi
jle     .L4
```

Conditional Jump Instruction

```
cmpq    %rsi, %rdi
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Jump to label if less than or equal to

Conditional Jump Instruction

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- Semantics:
  - If **`%rdi`** is less than or equal to **`%rsi`** (both interpreted as **signed value**), jump to the part of the code with a label **`.L4`**

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- Under the hood:

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- Under the hood:
  - **`cmpq`** instruction sets the condition codes
  - **`jle`** reads and checks the **condition codes**
  - If condition met, modify the Program Counter to point to the address of the instruction with a label **`.L4`**

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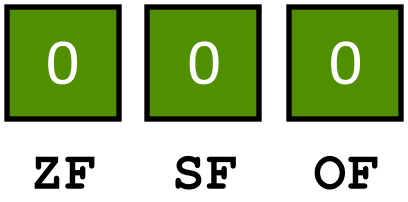
```



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    subq    %rsi,%rax
    ret
.L4:                  # x <= y
    movq    %rsi,%rax
    subq    %rdi,%rax
    ret
```

`cmpq` sets ZF, SF, OF

`jle` checks ZF | (SF ^ OF)