CSC 252: Computer Organization
Spring 2019: Lecture 19

Instructor: John Criswell

Department of Computer Science
University of Rochester

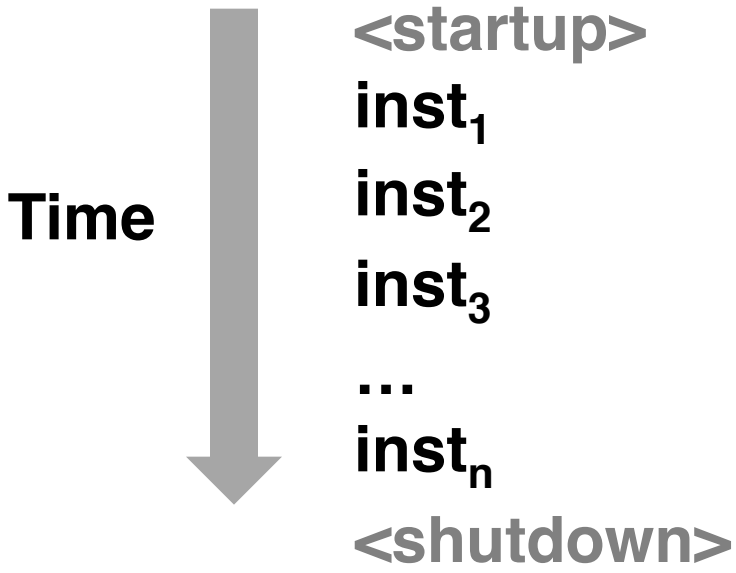
Action Items:

- **Programming Assignment 5 is out**
- **Trivia 5 is out**

So Far in CSC252…

- Processors do only one thing:
  - From startup to shutdown, a CPU simply reads and executes (interprets) a sequence of instructions, one at a time
  - This sequence is the CPU's *control flow* (or flow of control)

Physical control flow



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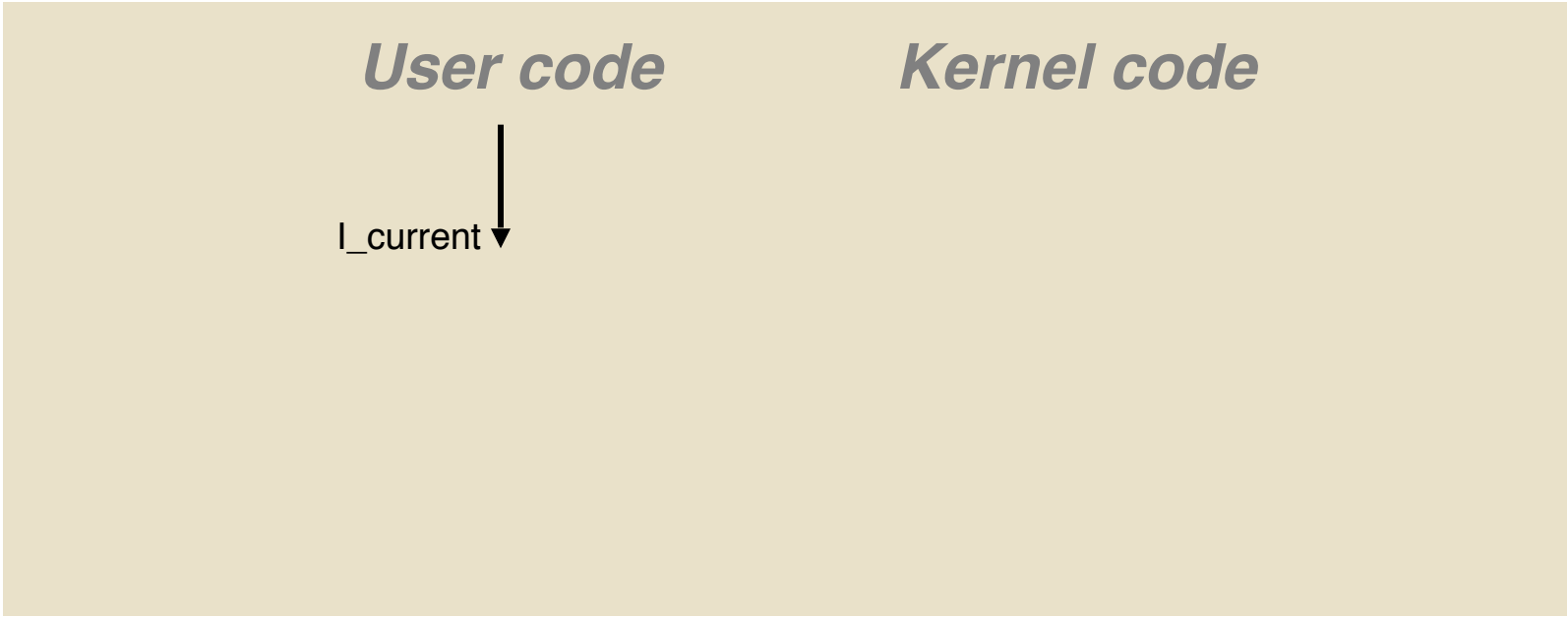
- System needs mechanisms for “exceptional control flow”

Today

- Exceptions/Interrupts

Exceptions

- An *exception* is a transfer of control to the OS *kernel* in response to some *event* (i.e., change in processor state)
  - Kernel is the memory-resident part of the OS
  - Examples of events: Divide by 0, arithmetic overflow, page fault, I/O request completes, typing Ctrl-C



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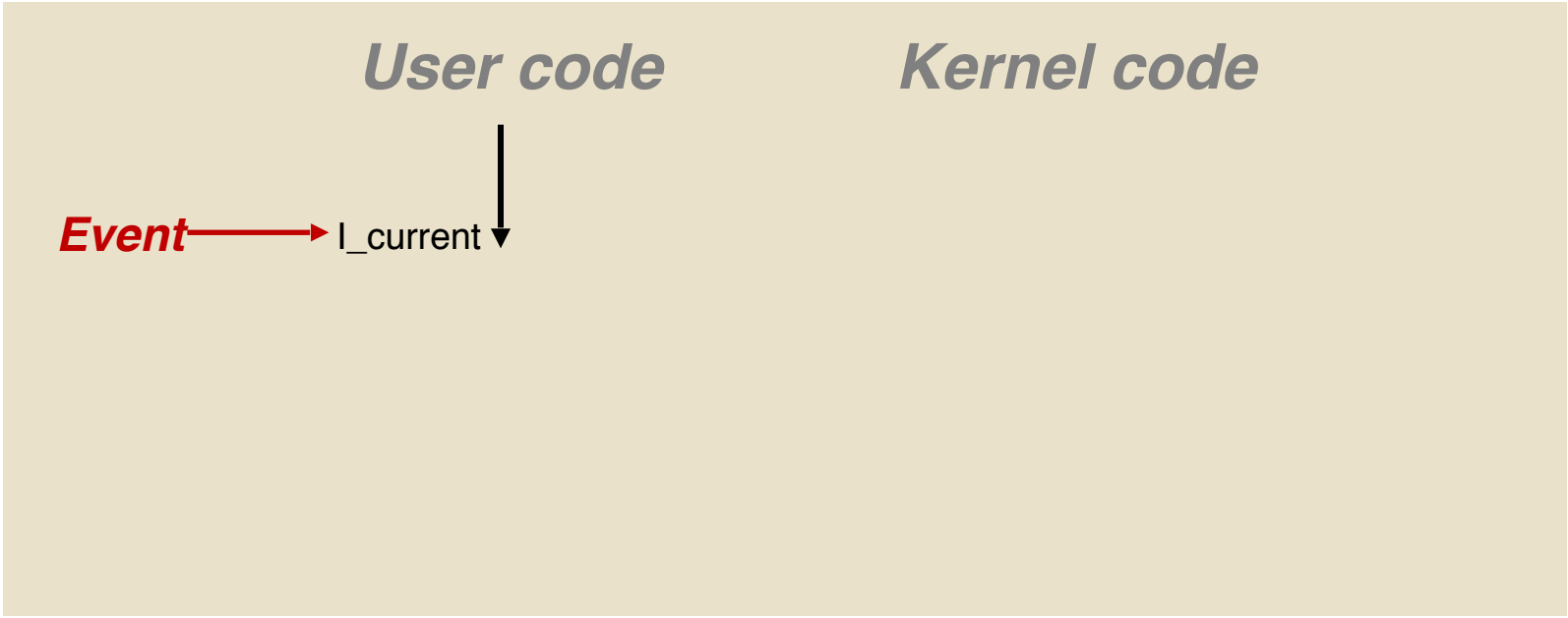

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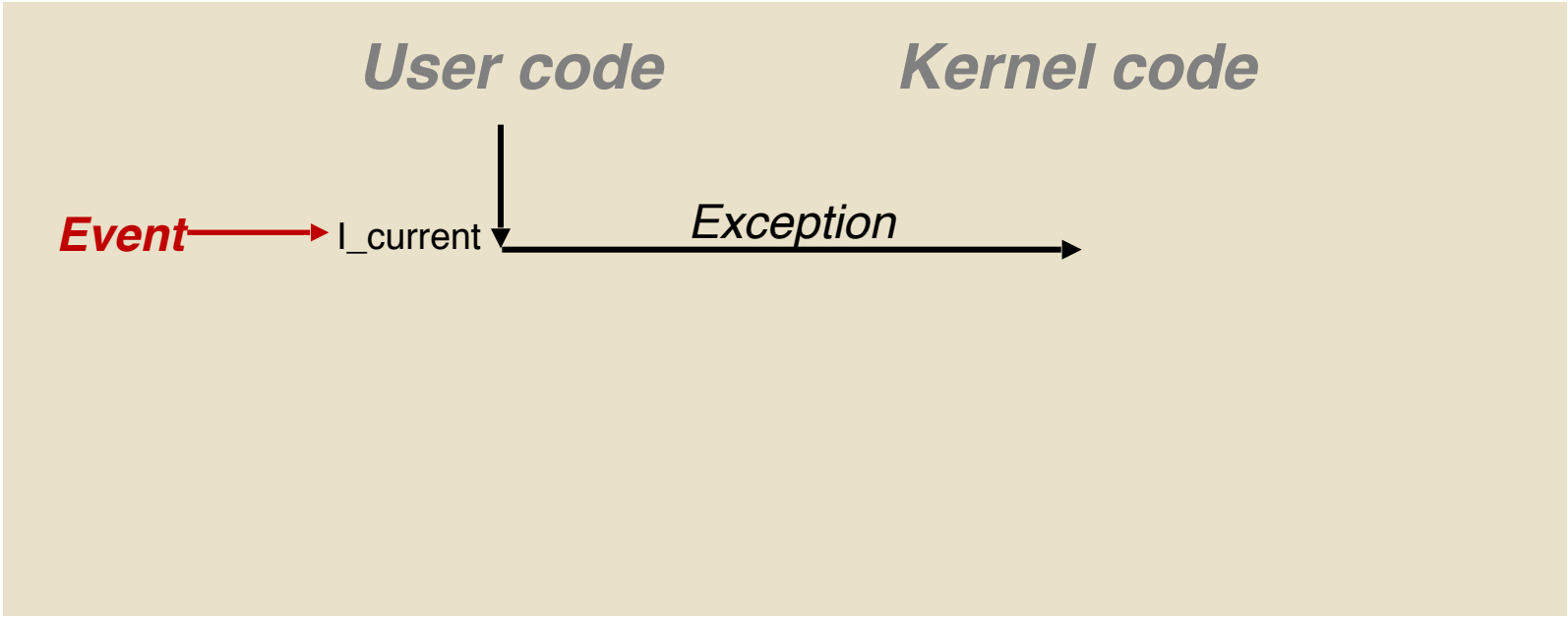

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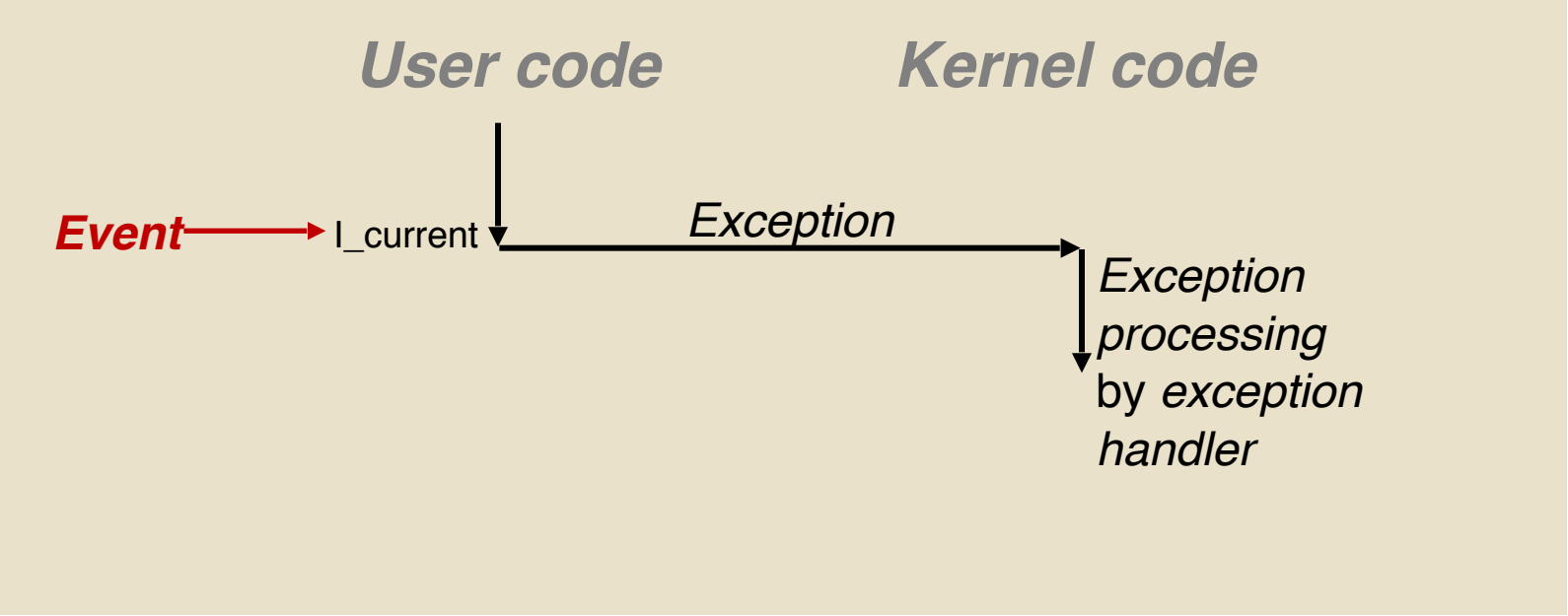

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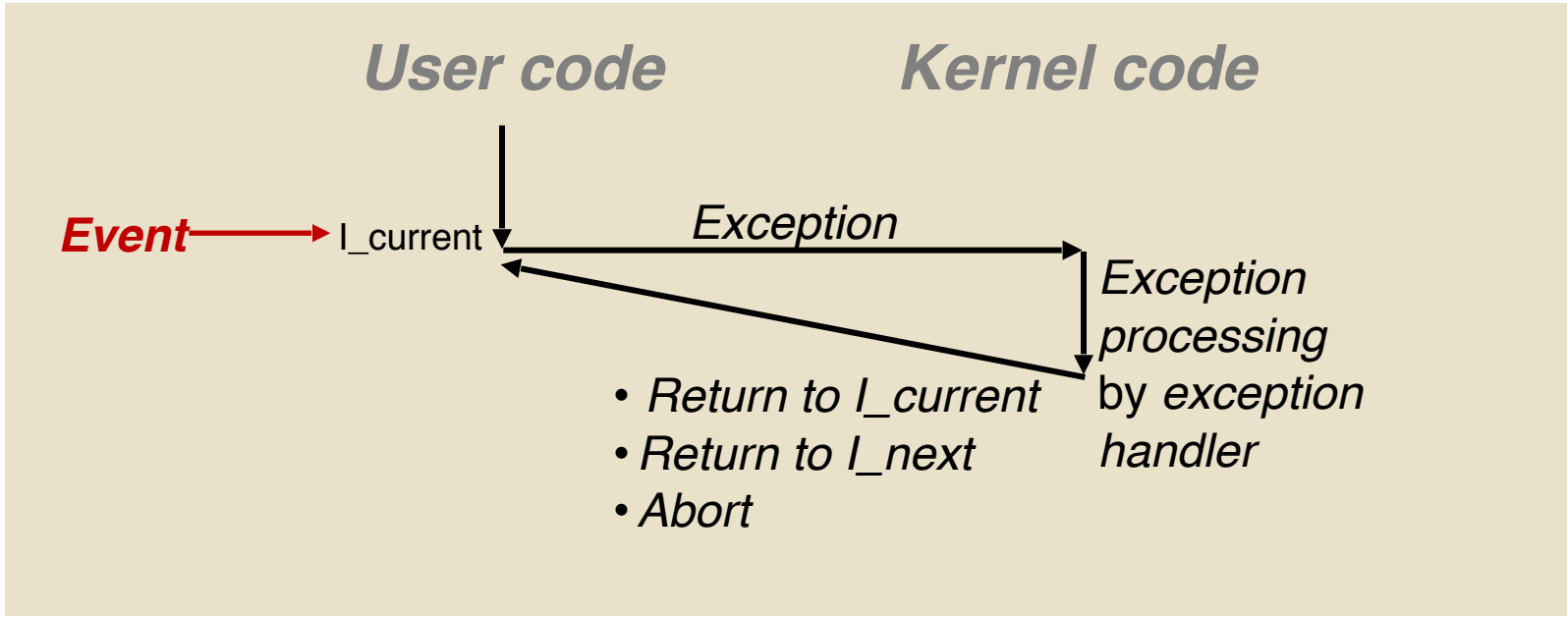

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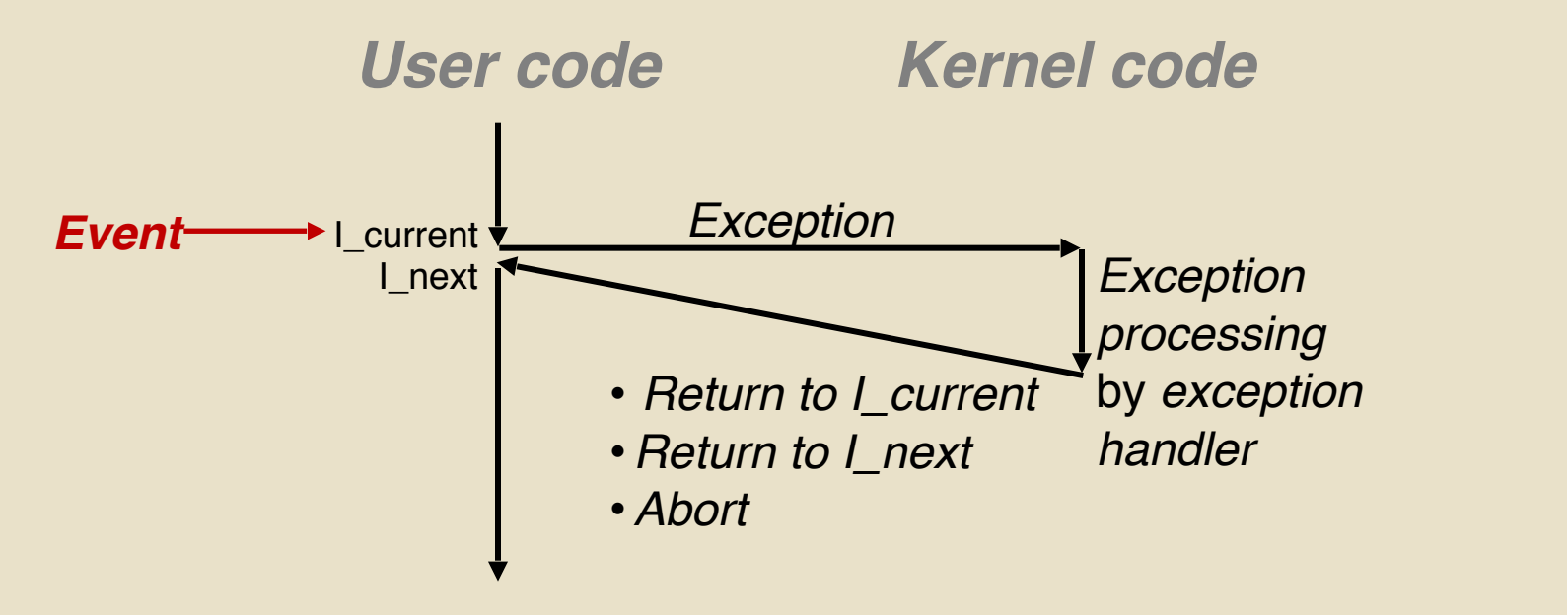

Asynchronous Exceptions (Interrupts)

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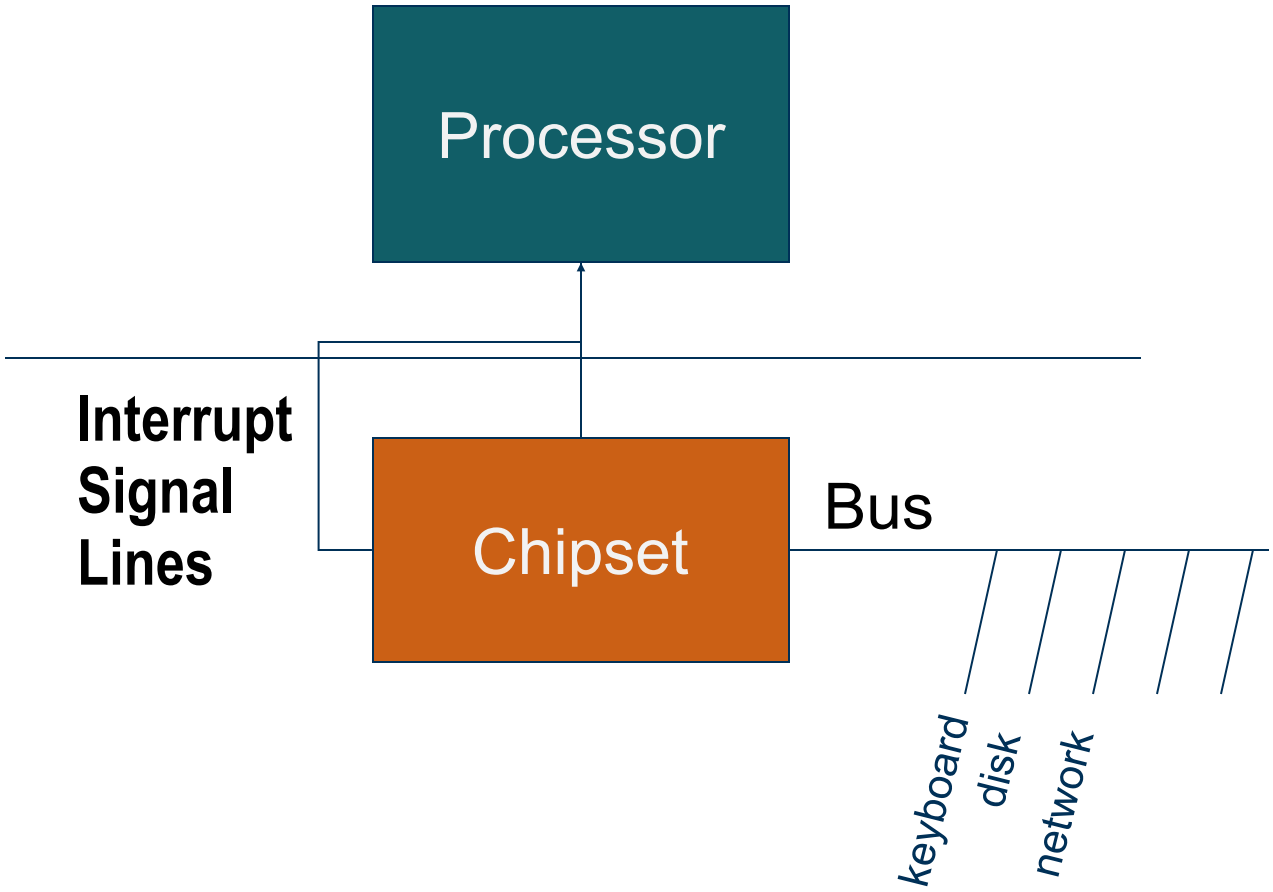
- Examples:
  - Timer interrupt
    - Every few ms, an external timer chip triggers an interrupt
    - Used by the kernel to take back control from user programs
  - I/O interrupt from external device
    - Hitting Ctrl-C at the keyboard
    - Arrival of a packet from a network
    - Arrival of data from a disk

Interrupts in a Processor



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  - *Aborts*
    - Unintentional and unrecoverable
    - Examples: parity error, machine check
    - Aborts current program

Fault Example: Page Fault

- User writes to memory location
- That memory location is not found in memory because it is currently on disk
- Trigger a Page Fault (recoverable), the exception handler loads the data from disk to memory (will discuss in detail later in the class)

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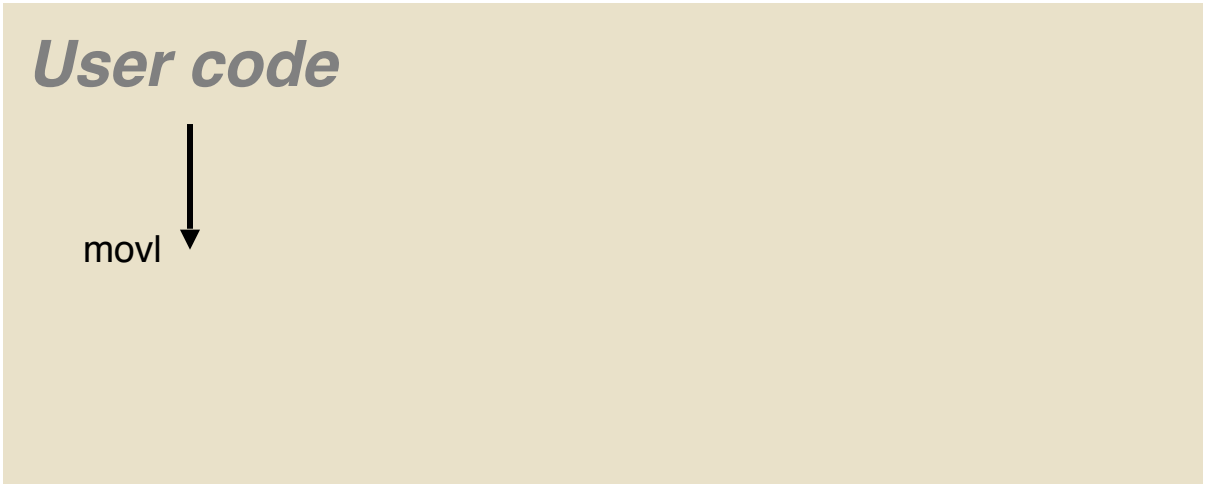

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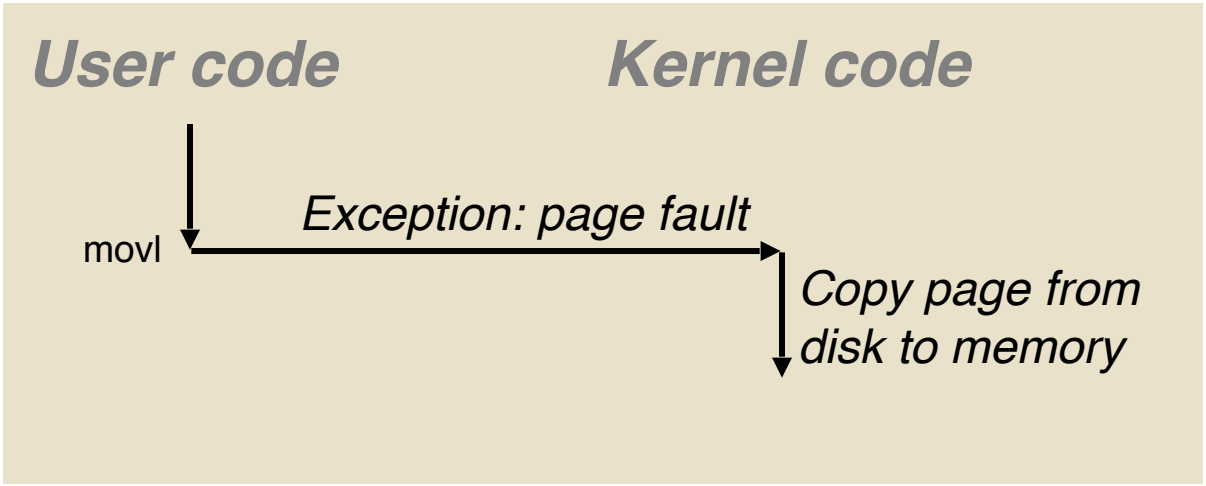

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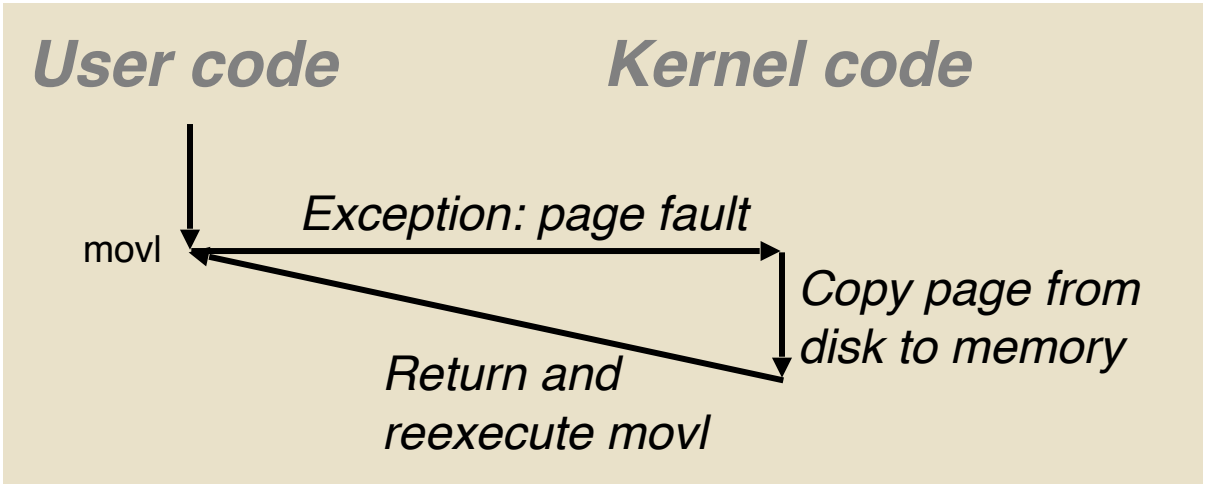

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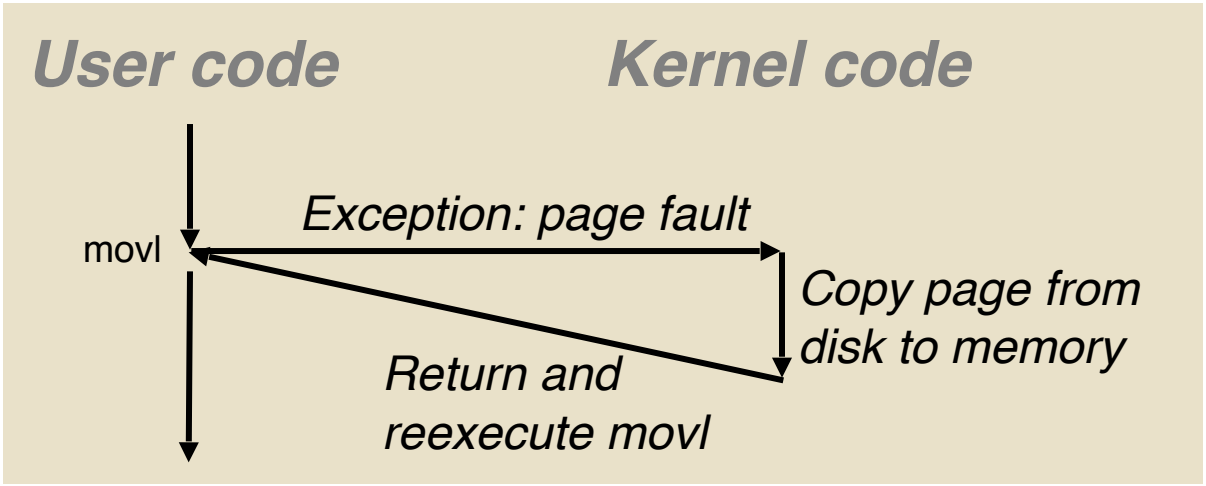

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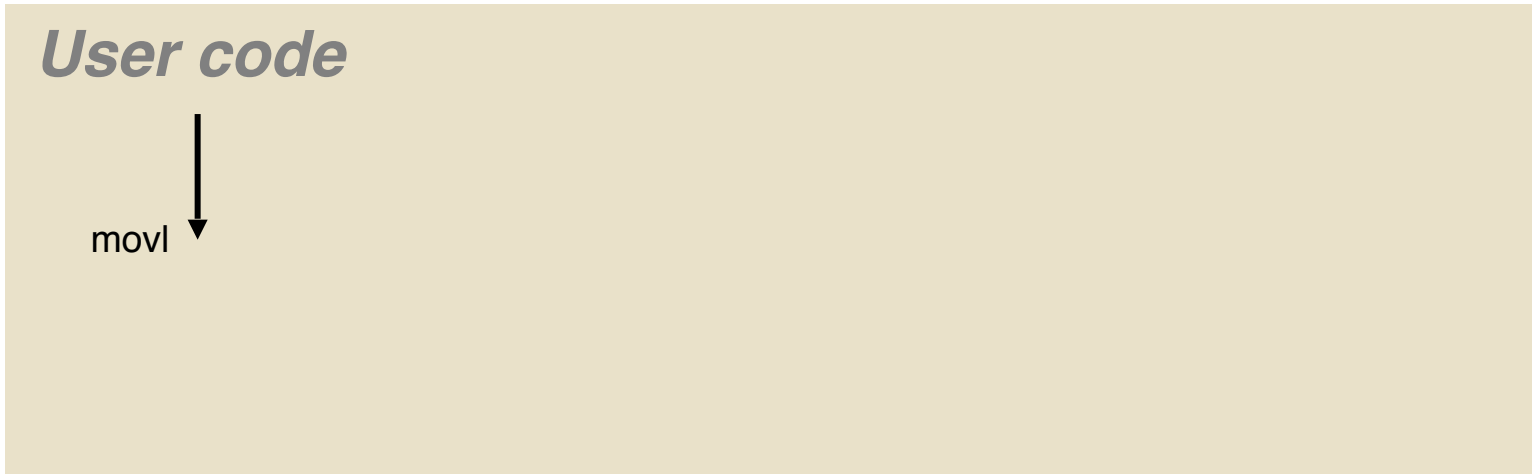

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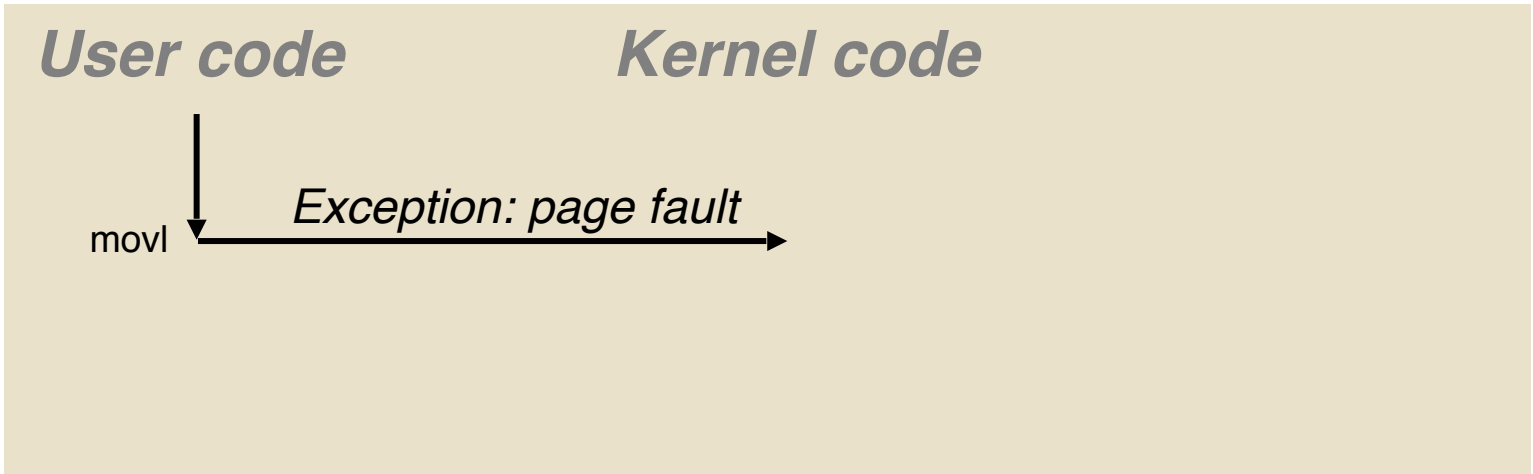

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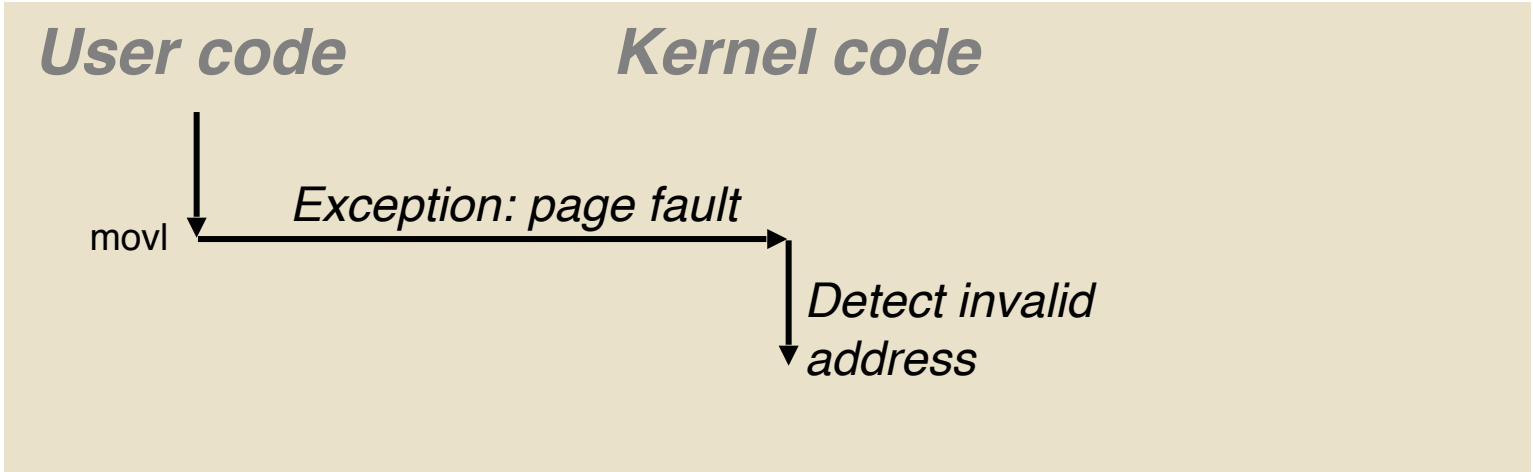

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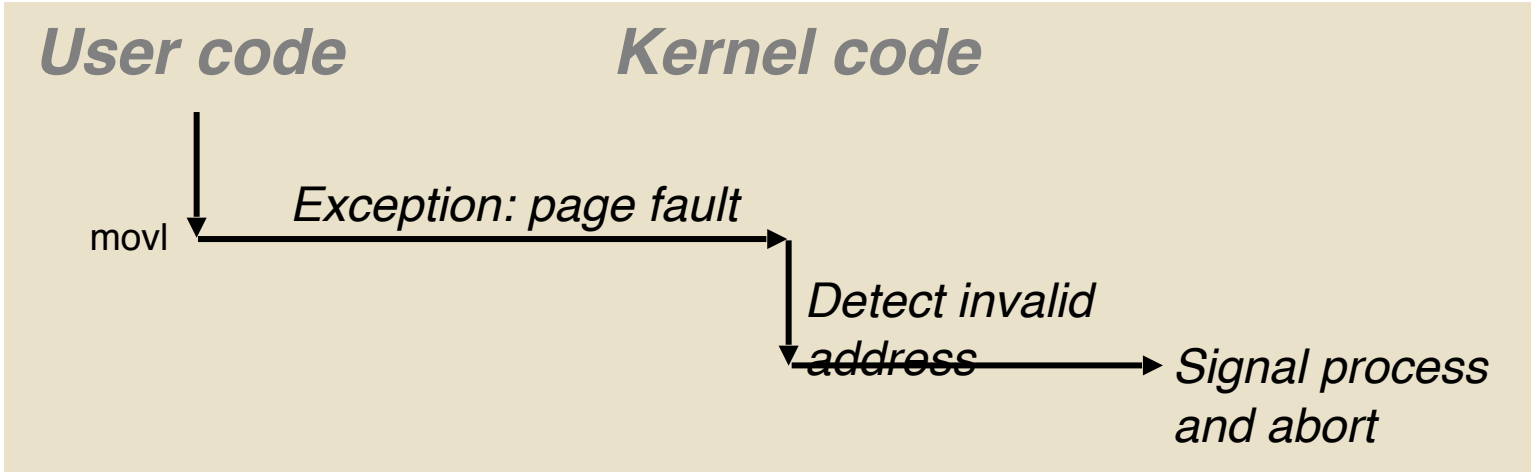

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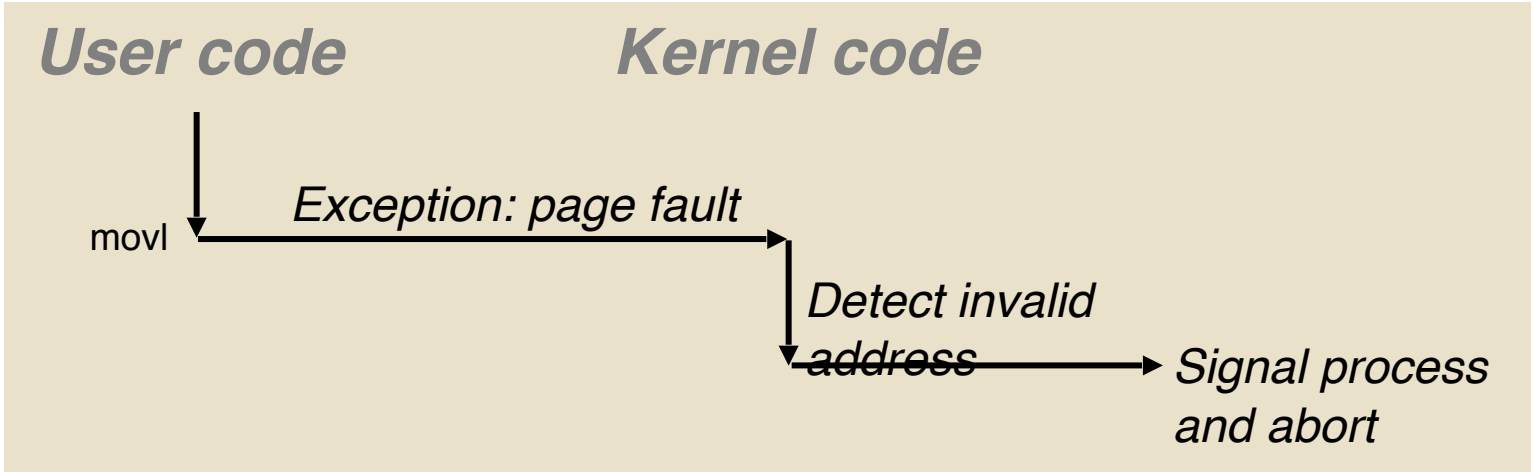

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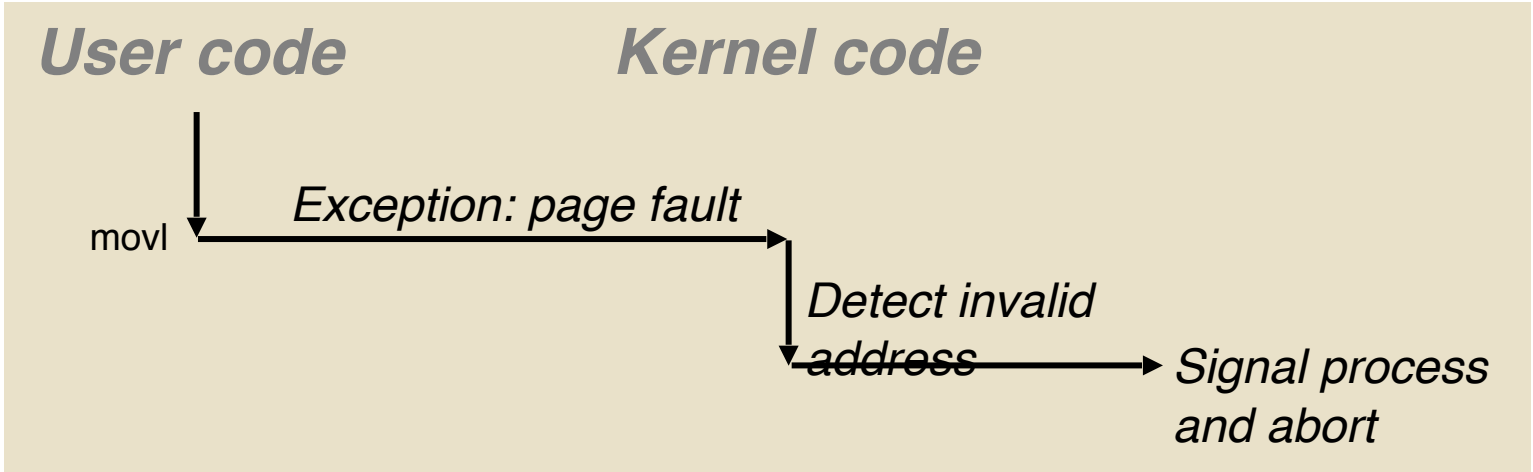

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- User process exits with “segmentation fault”

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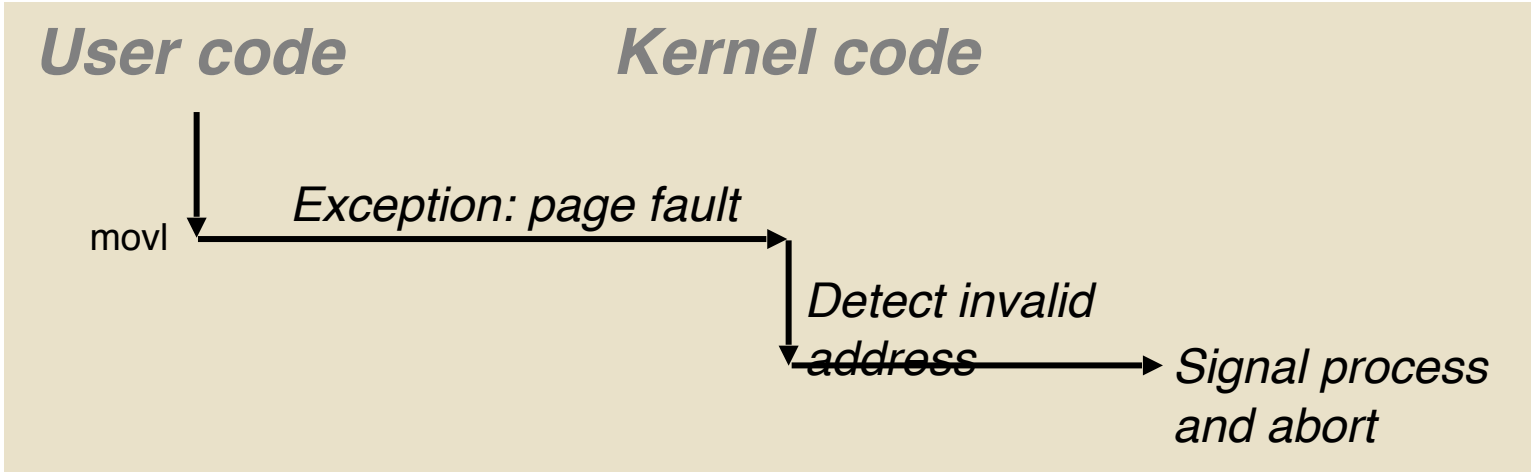

Others' Definitions

- The textbook's definitions are not universally accepted
- Intel (http://www.intel.com/cd/ids/developer/asmo-na/eng/microprocessors/ia32/xeon/19250.htm?page=2)
  - **Interrupt**: An exception that comes from outside of the processor. There are two kinds of exceptions: local and external. A local exception is generated from a program. External exceptions are usually generated by external I/O devices and received at exception pins.
- PowerPC Architecture
  - Interrupts "allow the processor to change state as a result of external signals, errors, or unusual conditions arising in the execution of instructions"
- PowerPC 604
  - Everything is an exception
- Motorola 68K
  - Everything is an exception
- VAX
  - Interrupts: device, software, urgent
  - Exceptions: faults, traps, aborts

When Do You Call the Handler?

- Interrupts: when convenient. Typically wait until the current instructions in the pipeline are finished
- Exceptions: typically immediately as programs can't continue without resolving the exception (think of page fault)
- Maskable verses Unmaskable
  - Interrupts can be individually masked (i.e., ignored by CPU)
  - Synchronous exceptions are usually unmaskable
- Some interrupts are intentionally unmaskable
  - Called non-maskable interrupts (NMI)
  - Indicating a critical error has occurred, and that the system is probably about to crash

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- Interrupts/Traps
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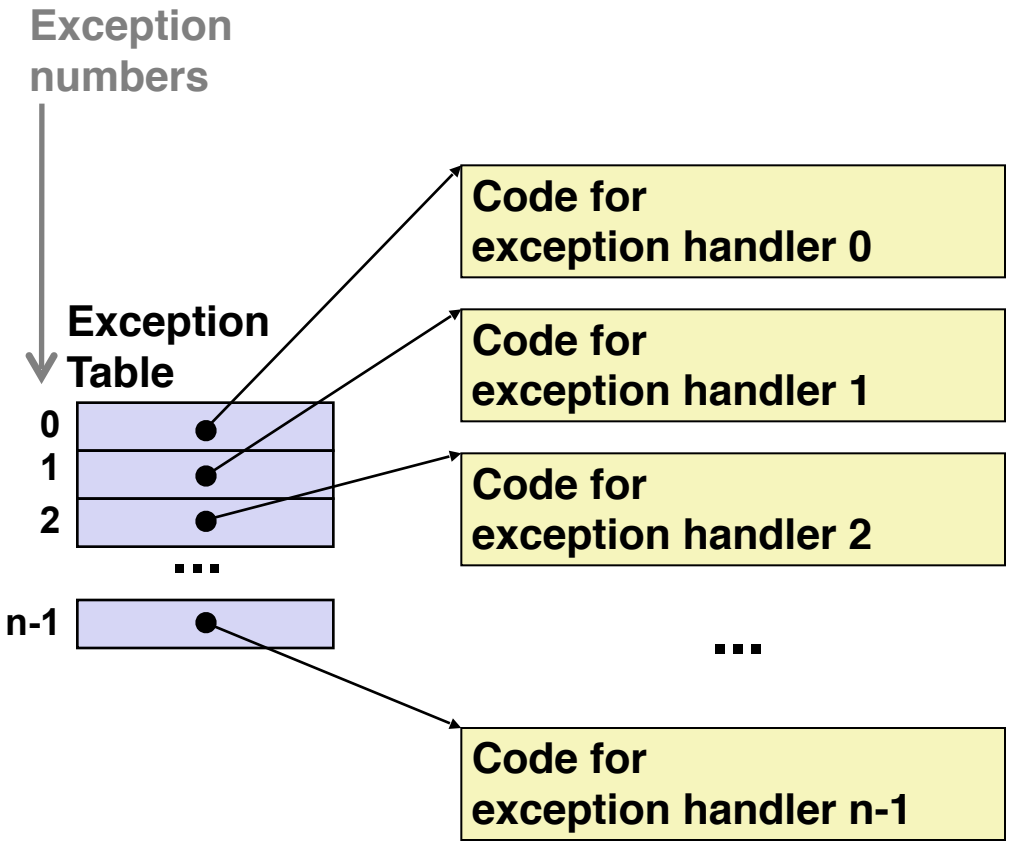
- Faults
  - Exception handler returns to the instruction that caused the exception, i.e., ***re-execute*** it!
- Aborts
  - Never returns to the program

Where to Find Exception Handlers?



- Each type of event has a unique exception number k
- k = index into exception table
- Exception table lives in memory. Its start address is stored in a special register
- Handler k is called each time exception k occurs

Nested Exceptions

- One interrupt/exception occurs when another is already active
- Priority maintained

- Can fundamentally do it
  - Subroutine calls within subroutine calls
  - Handlers need to save appropriate state

Concurrent Interrupts

- More than one interrupts happen at the same time
- Pre-defined priority
- The chipset arbitrates which one to respond to first