CSC 252: Computer Organization
Spring 2020: Lecture 16

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Announcements

- By default 252/452 will be pass/fail
- 4/10 is the deadline to opt-out and request a letter grade
- Mid-term solution has been posted
- Mid-term grades will be posted this weekend
- Lectures will be recorded and posted online
- Office hours will be held through Zoom; links on the website

The Problem

- Bigger is slower
  - Flip-flops/Small SRAM, sub-nanosec
  - SRAM, KByte~MByte, ~nanosec
  - DRAM, Gigabyte, ~50 nanosec
  - Hard Disk, Terabyte, ~10 millisec

- Faster is more expensive (dollars and chip area)
  - SRAM, < 10$ per Megabyte
  - DRAM, < 1$ per Megabyte
  - Hard Disk < 1$ per Gigabyte

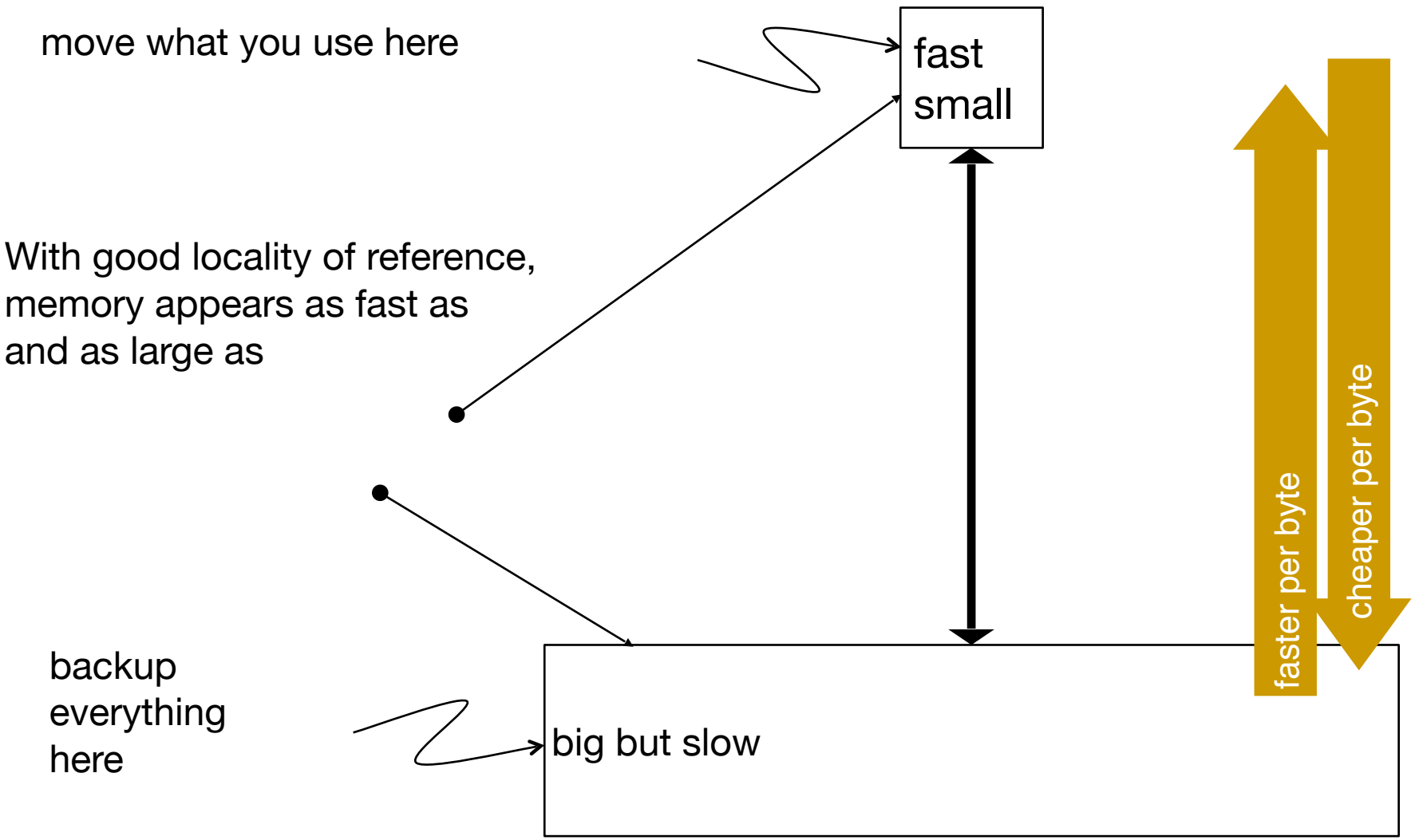
- Other technologies have their place as well
  - PC-RAM, MRAM, RRAM

We want both fast and large Memory

- But we cannot achieve both with a single level of memory

- Idea: Memory Hierarchy
  - Have multiple levels of storage (progressively bigger and slower as the levels are farther from the processor)
  - ensure most of the data the processor needs in the near future is kept in the fast(er) level(s)

Memory Hierarchy

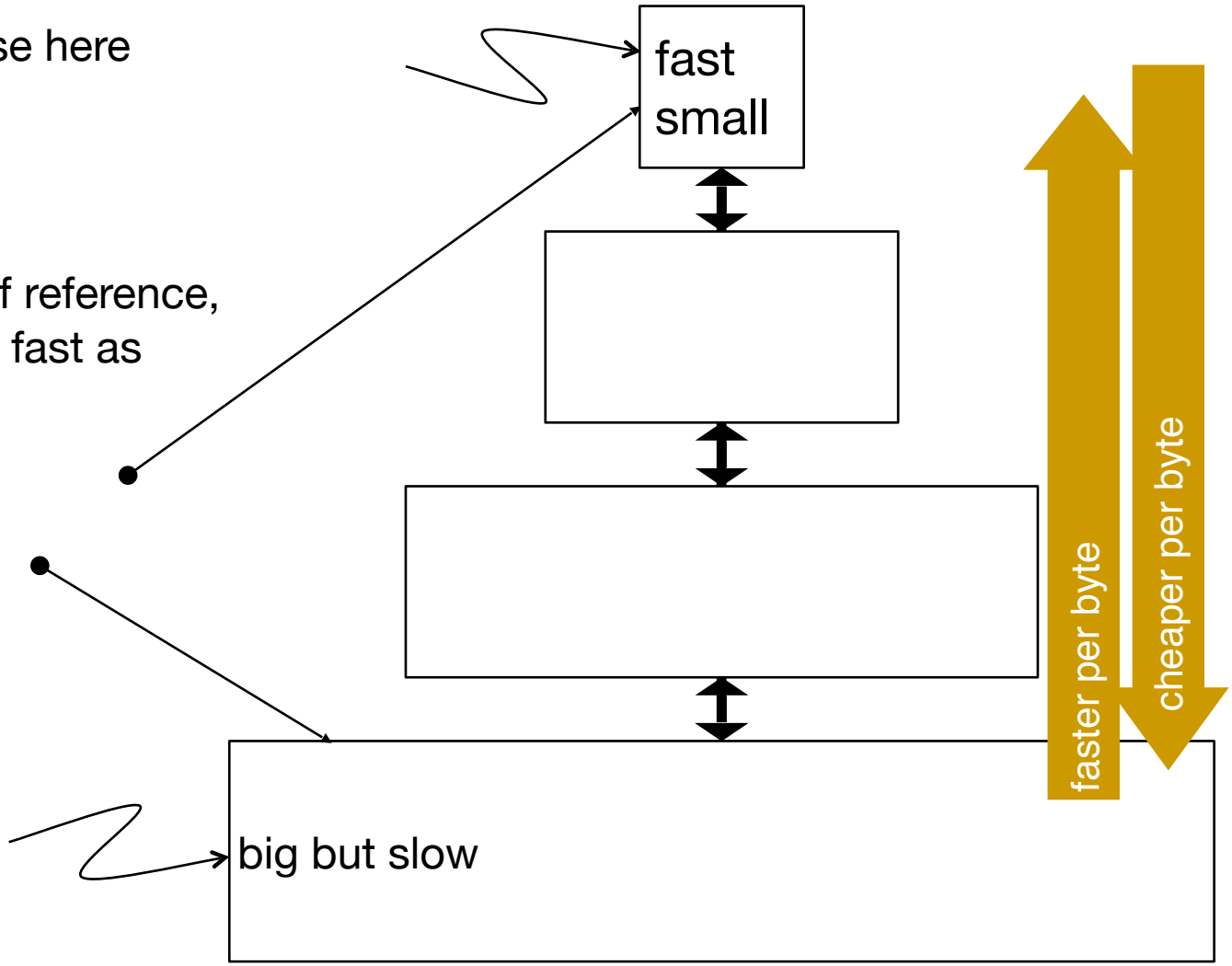


Memory Hierarchy

move what you use here

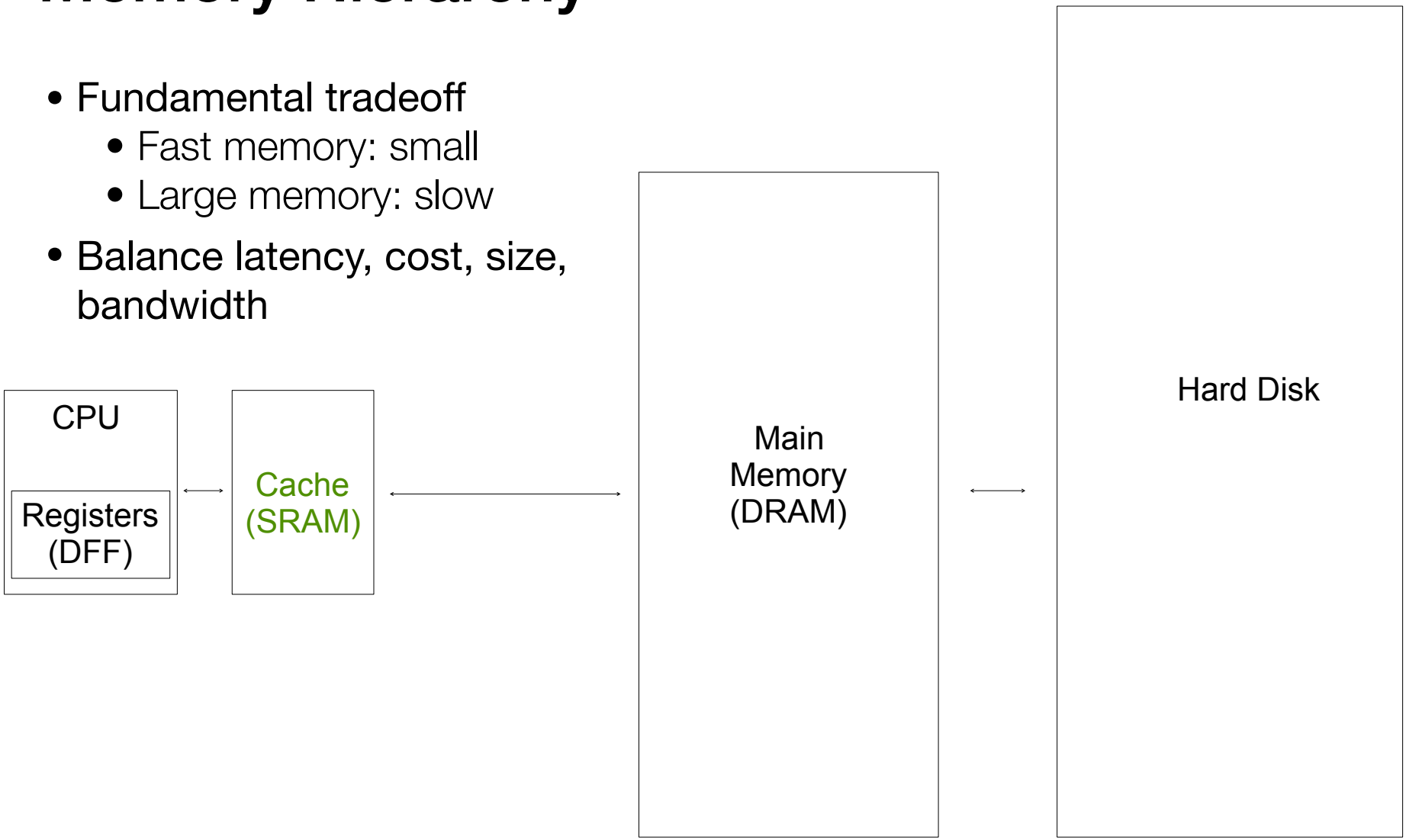
With good locality of reference, memory appears as fast as and as large as

backup everything here



Memory Hierarchy

- Fundamental tradeoff
  - Fast memory: small
  - Large memory: slow
- Balance latency, cost, size, bandwidth

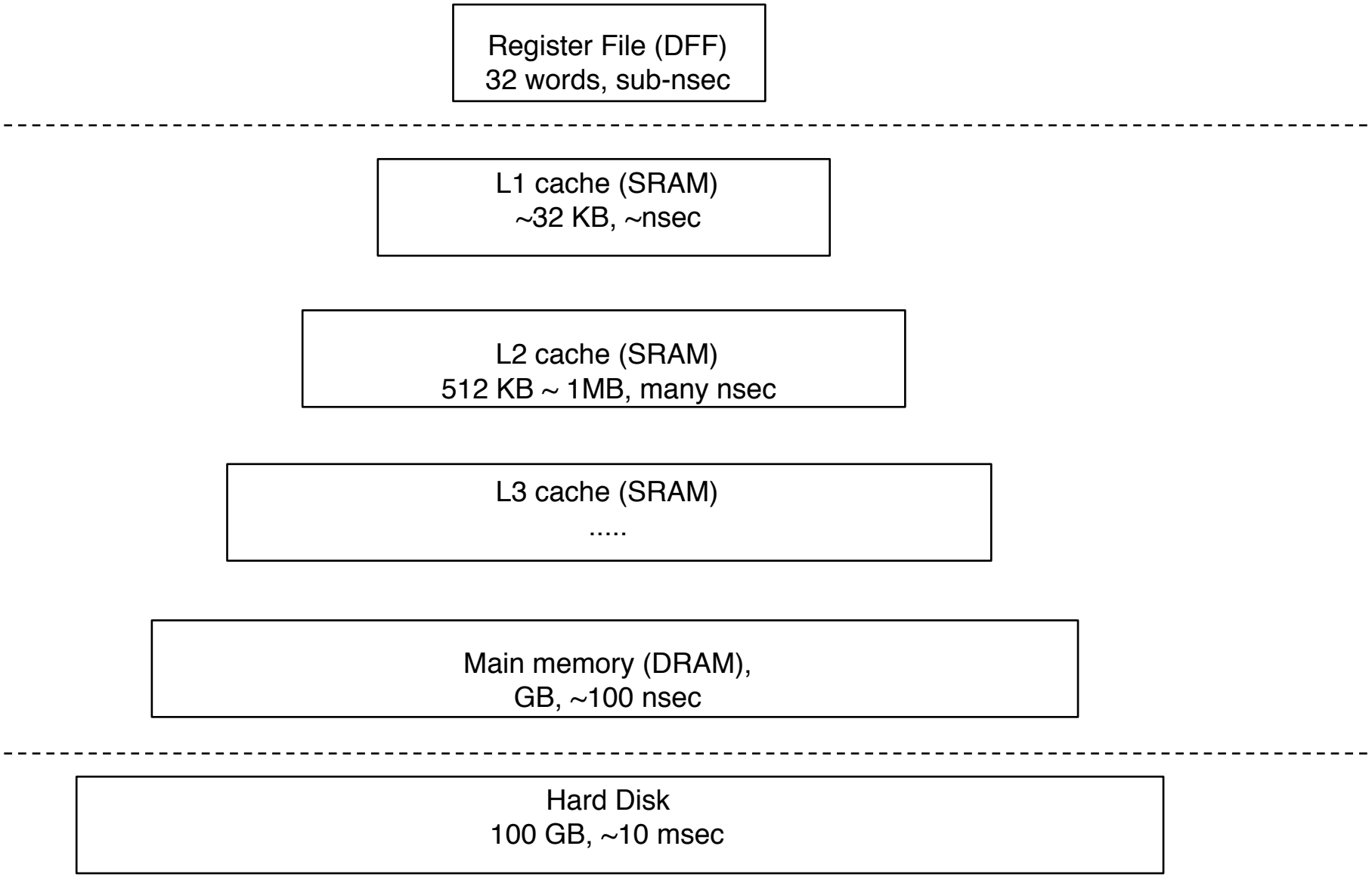


The Bookshelf Analogy

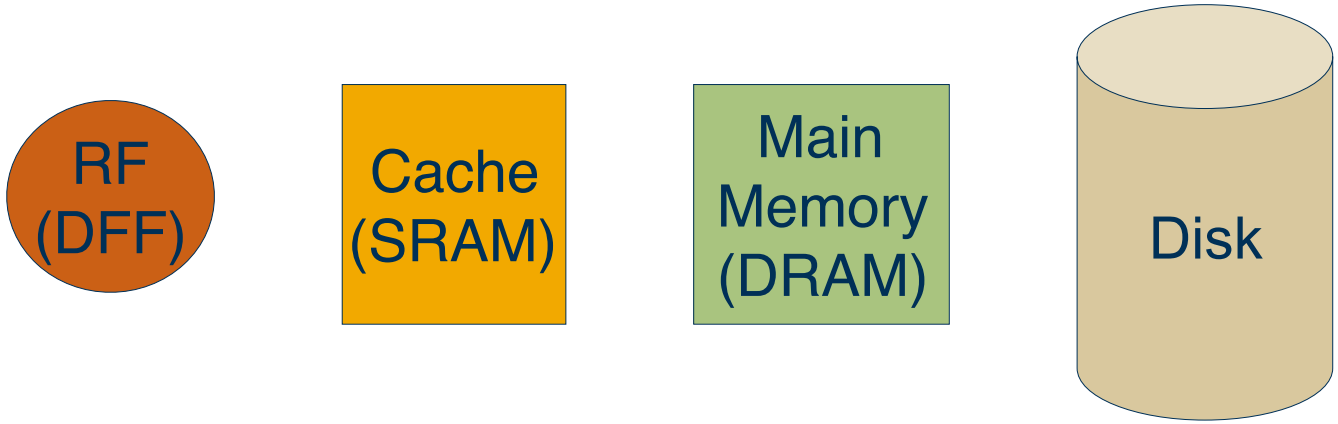
- Book in your hand
- Desk
- Bookshelf
- Boxes at home
- Boxes in storage

- Recently-used books tend to stay on desk
  - Comp Org. books, books for classes you are currently taking
  - Until the desk gets full
- Adjacent books in the shelf needed around the same time

A Modern Memory Hierarchy



How Things Have Progressed

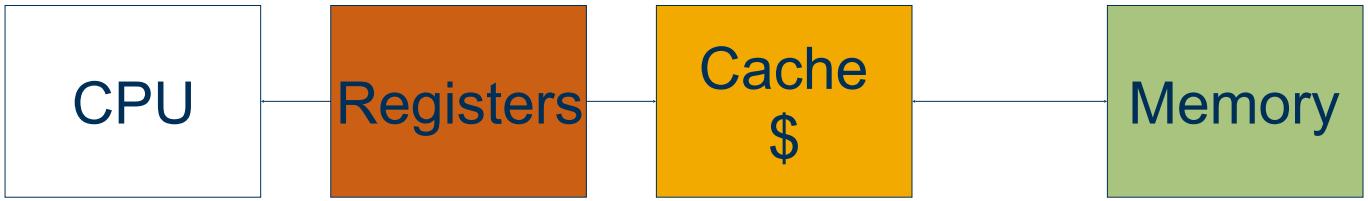


1995 low-mid range Hennessy & Patterson, Computer Arch., 1996	200B 5ns	64KB 10ns	32MB 100ns	2GB 5ms
2009 low-mid range www.dell.com, $449 including 17" LCD flat panel	~200B 0.33ns	8MB 0.33ns	4GB <100ns	750GB 4ms
2015 mid range	~200B 0.33ns	8MB 0.33ns	16GB <100ns	**256GB** **10us**

How to Make Effective Use of the Hierarchy

- Fundamental question: how do we know what data to put in the fast and small memory?
- Answer: ensure most of the data the processor needs in the near future is kept in the fast(er) level(s)
- How do we know what data will be needed in the future?
  - Do we know before the program runs?
    - If so, programmers or compiler can place the right data at the right place
  - Do we know only after the program runs?
    - If so, only the hardware can effectively place the data

How to Make Effective Use of the Hierarchy



- Modern computers provide both ways
- Register file: programmers explicitly move data from the main memory (slow but big DRAM) to registers (small, very fast)
  - `movq (%rdi), %rdx`
- Cache, on the other hand, is automatically managed by hardware
  - Sits between registers and main memory, “invisible” to programmers
  - The hardware automatically figures out what data will be used in the near future, and place in the cache.
  - How does the hardware know that??

Locality

- Principle of Locality: Programs tend to use data and instructions with addresses near or equal to those they have used recently

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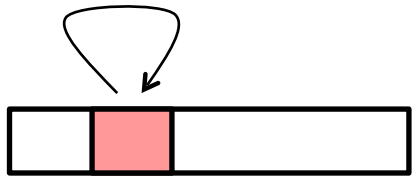
  - Recently referenced items are likely to be referenced again in the near future



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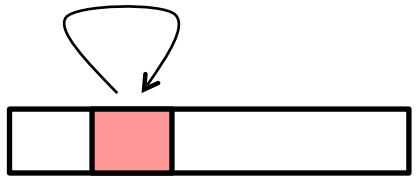
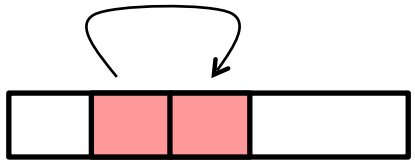


- Spatial locality:
  - Items with nearby addresses tend to be referenced close together in time



Locality Example

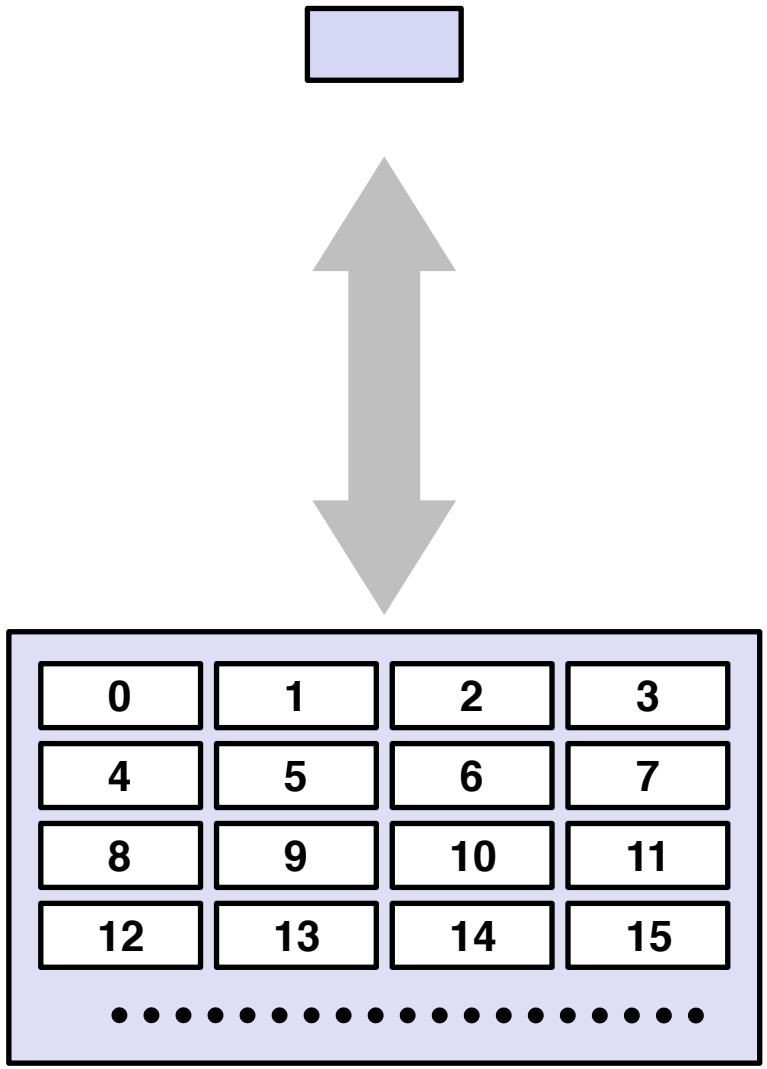
```
sum = 0;
for (i = 0; i < n; i++)
    sum += a[i];
return sum;
```

- Data references
  - **Spatial** Locality: Reference array elements in succession (stride-1 reference pattern)
  - **Temporal** Locality: Reference variable sum each iteration.

- Instruction references
  - **Spatial** Locality: Reference instructions in sequence.
  - **Temporal** Locality: Cycle through loop repeatedly.

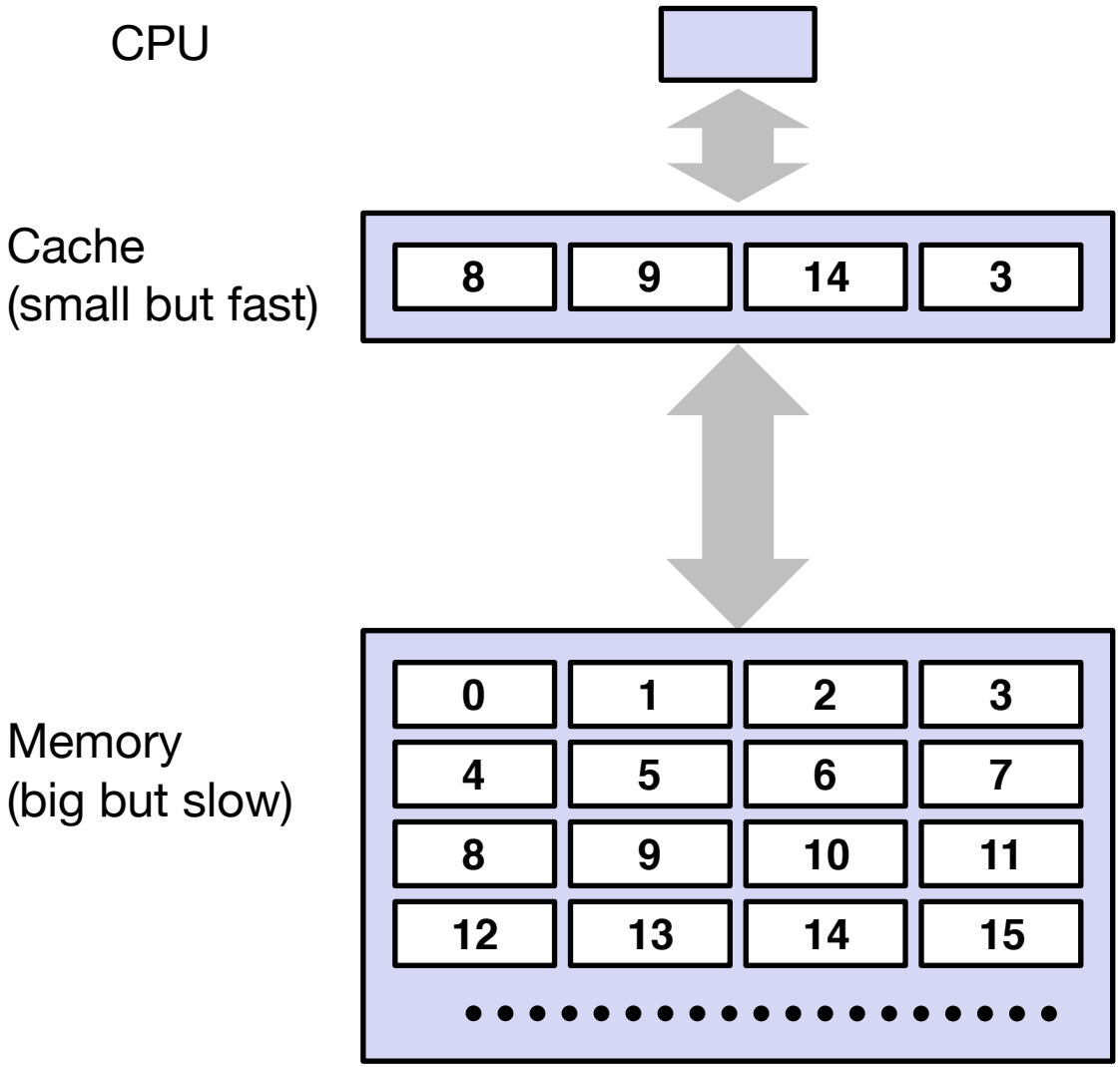
Cache Illustrations

CPU



Memory
(big but slow)

Cache Illustrations



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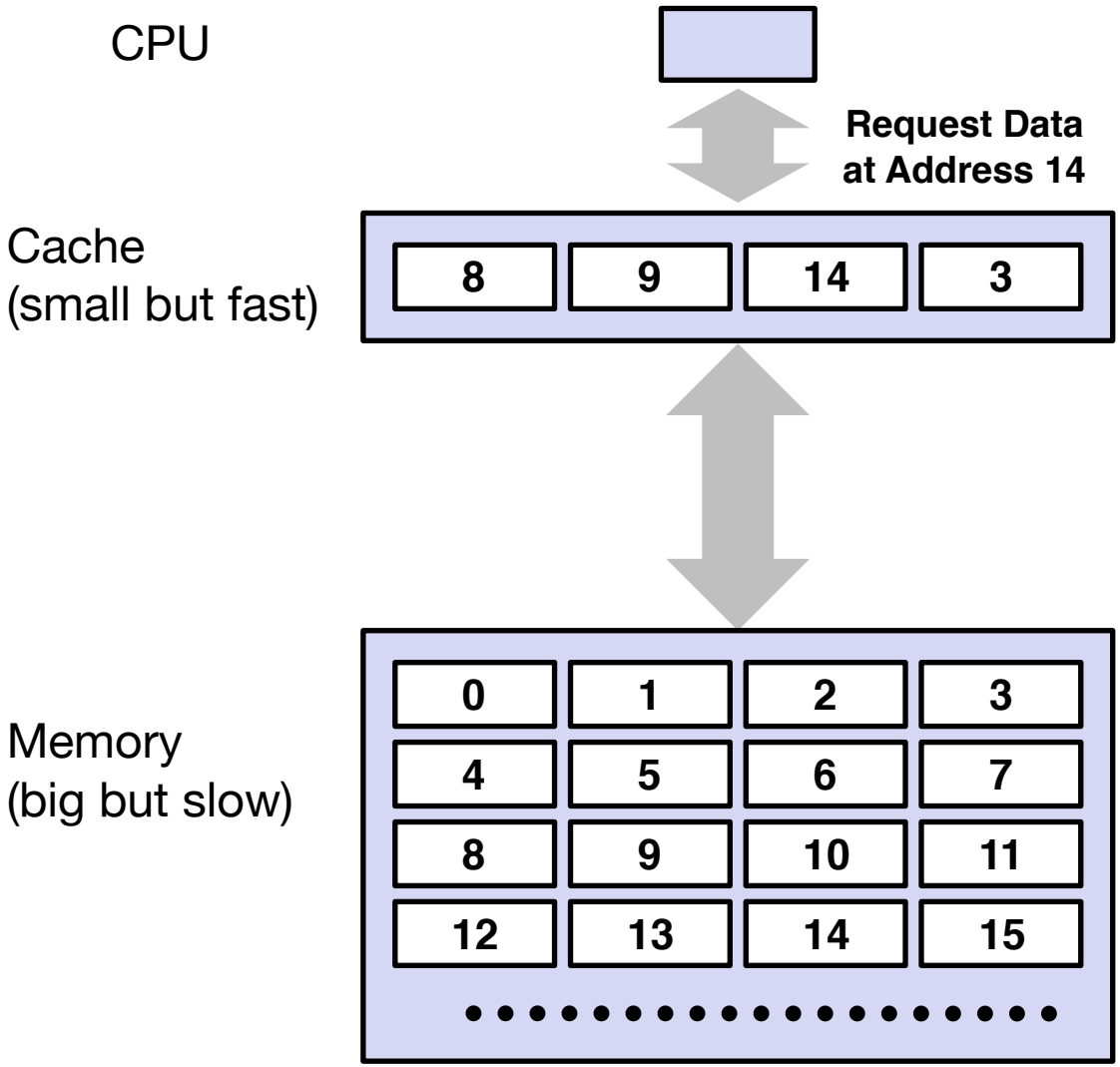
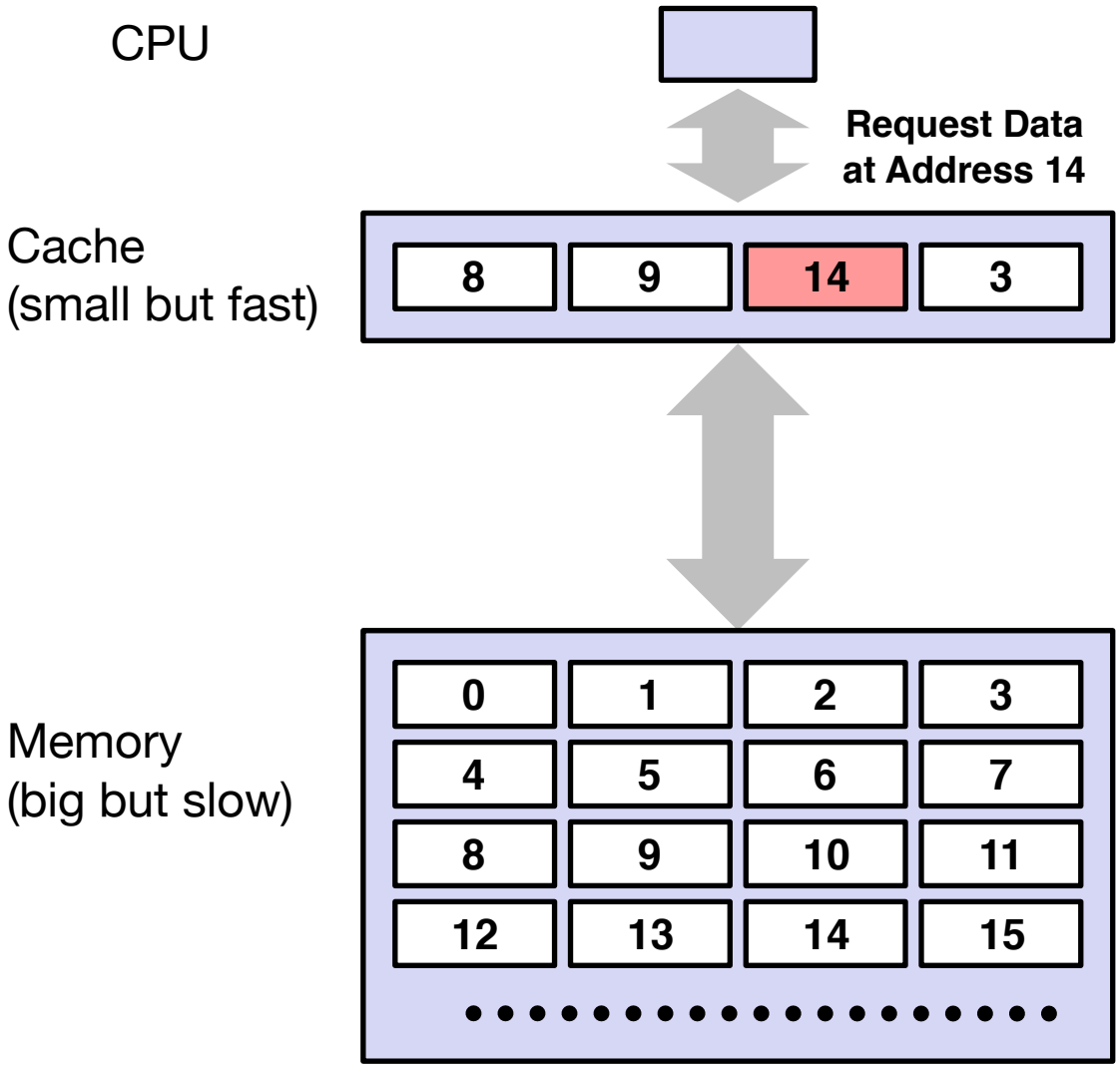


Data in address b is needed

Cache Illustrations



Data in address b is needed

Address b is in cache: Hit!

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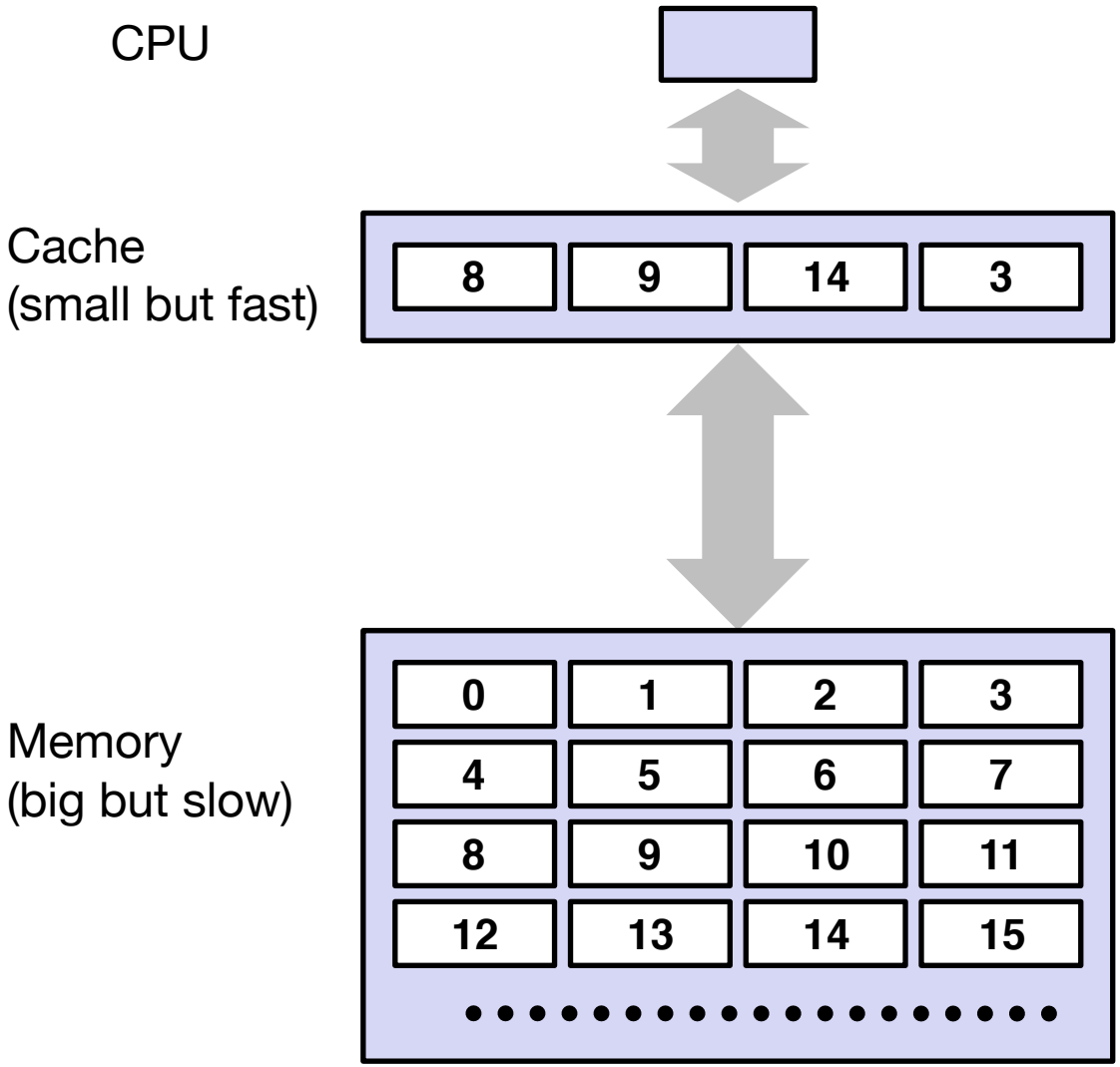

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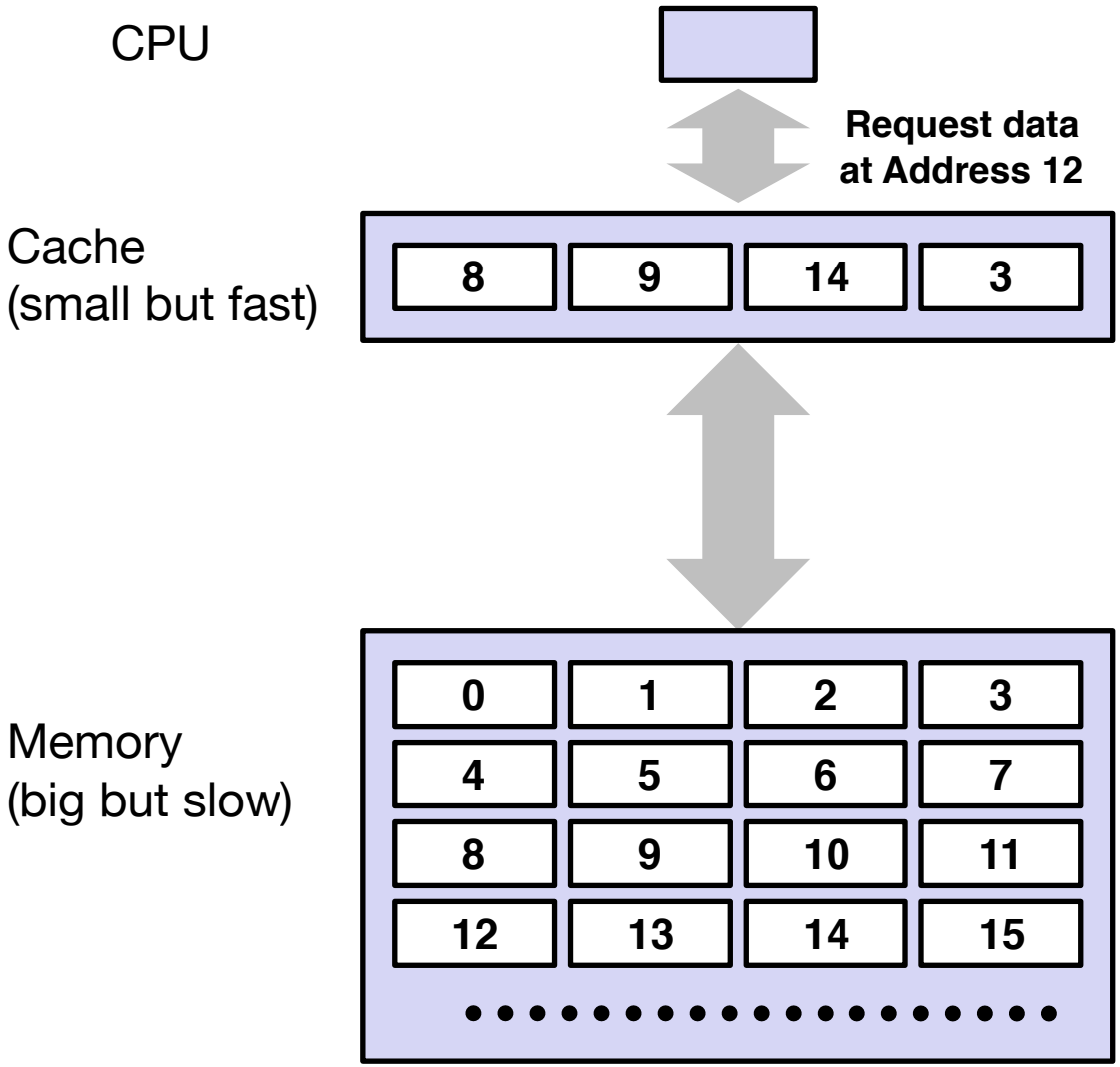

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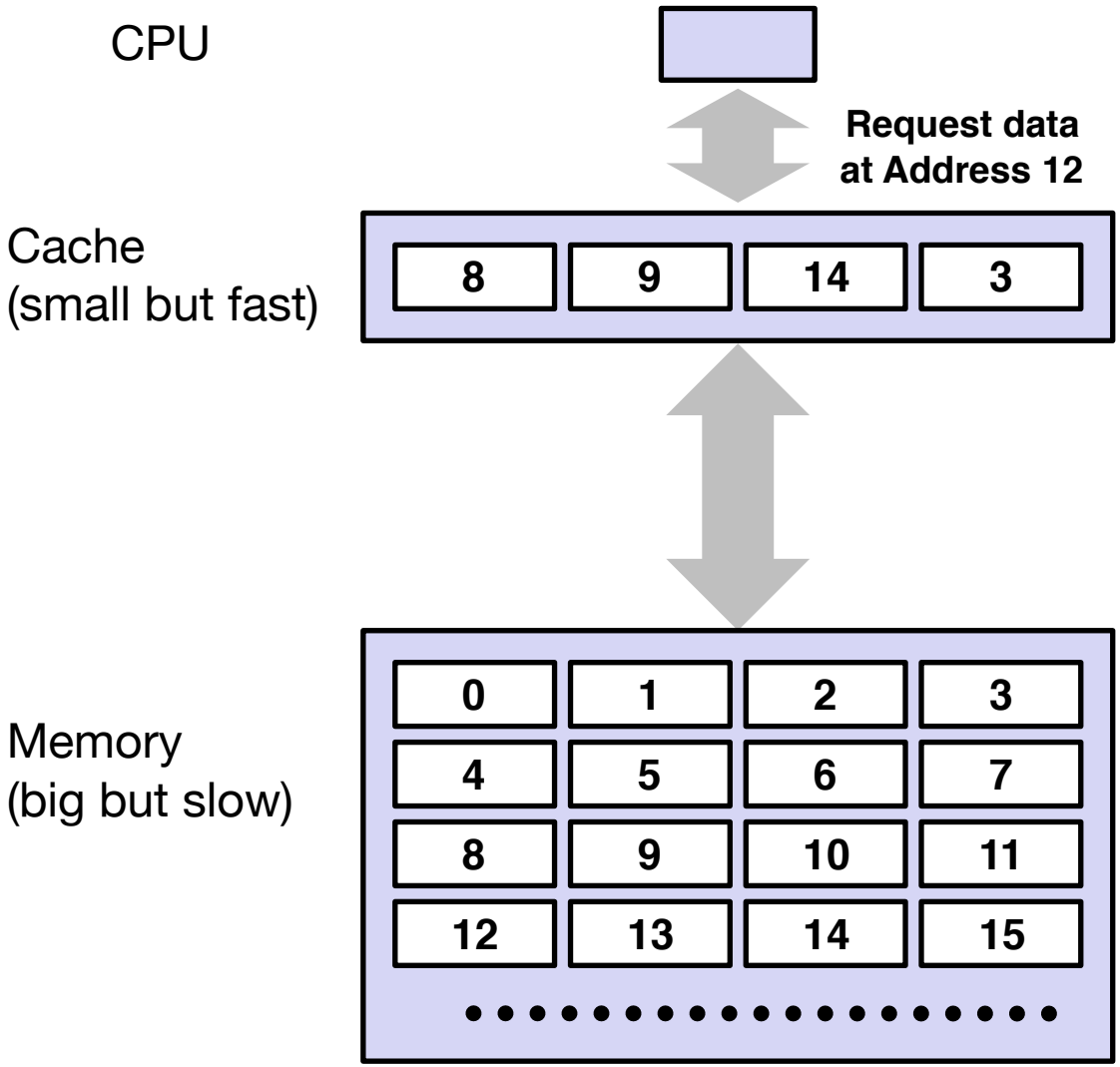

Data in address b is needed

Address b is not in cache: Miss!

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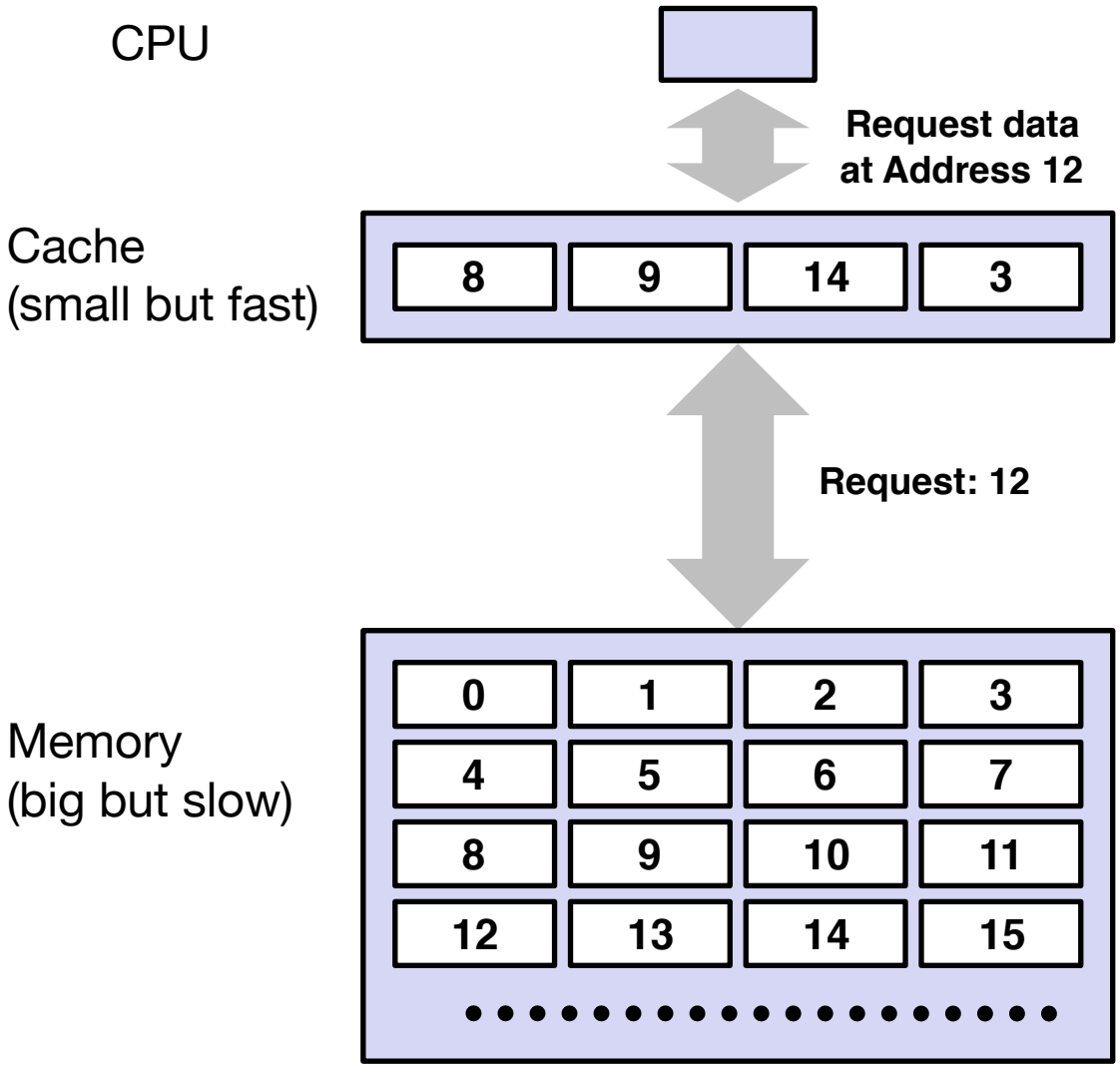

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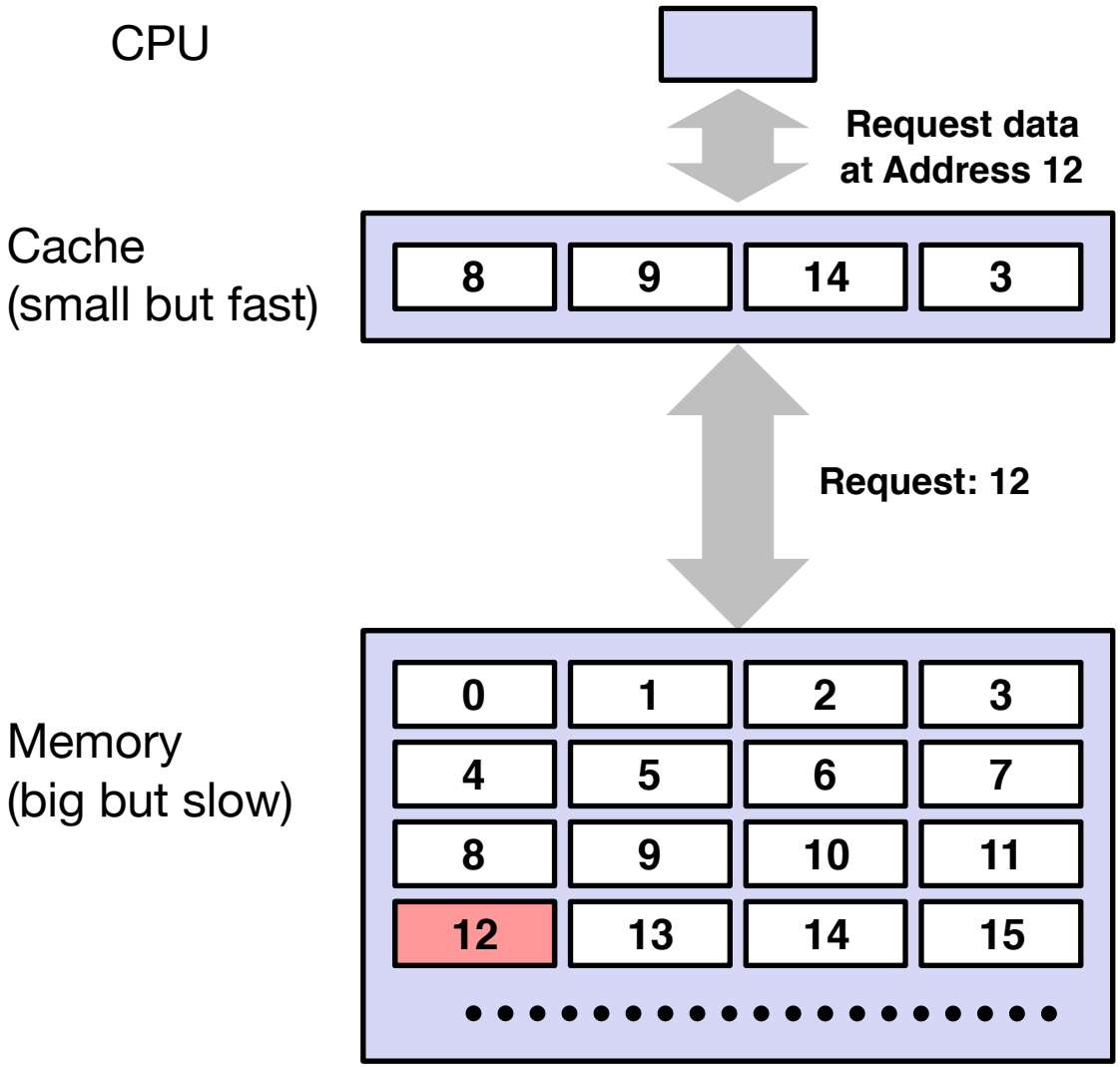

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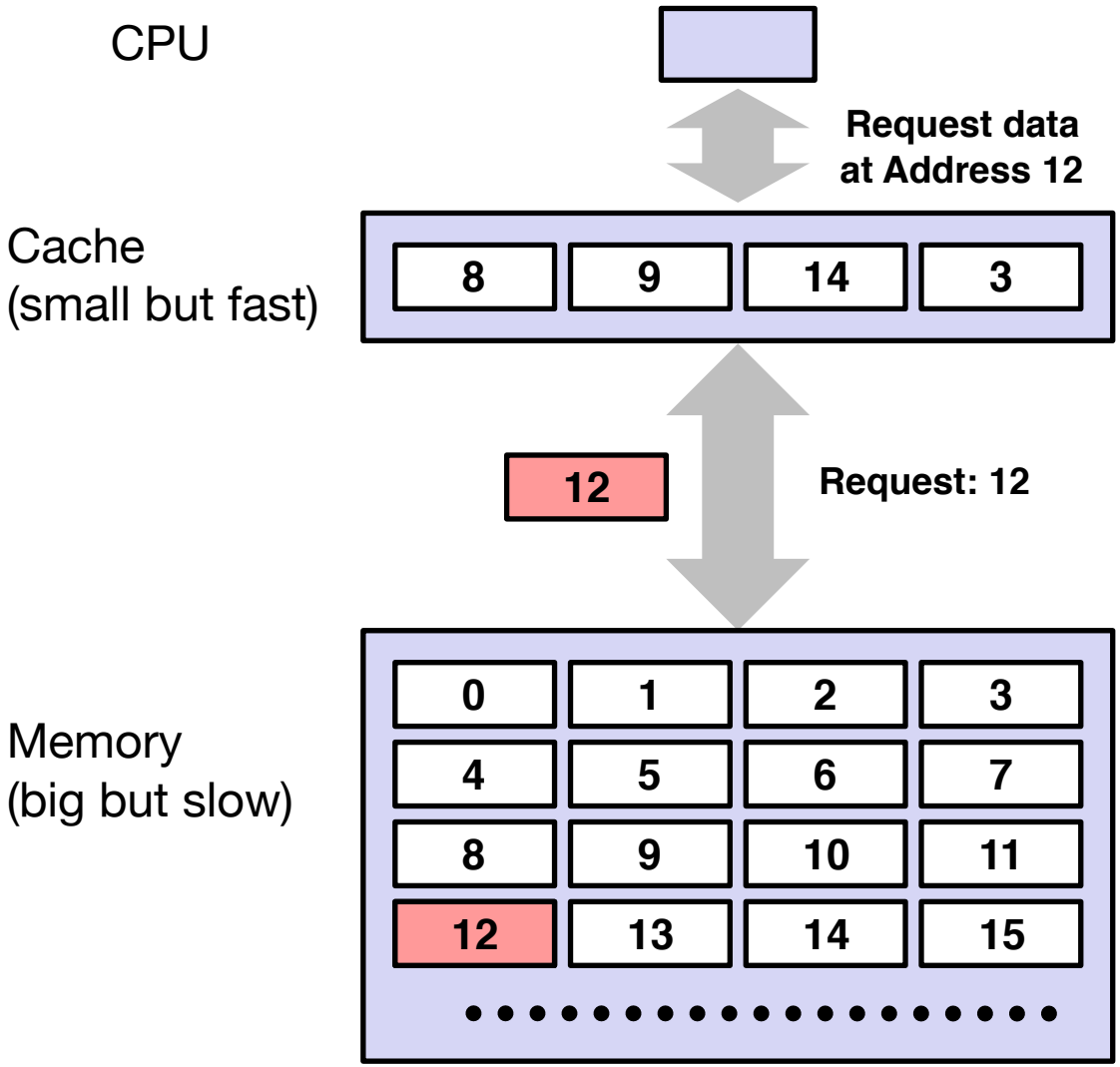

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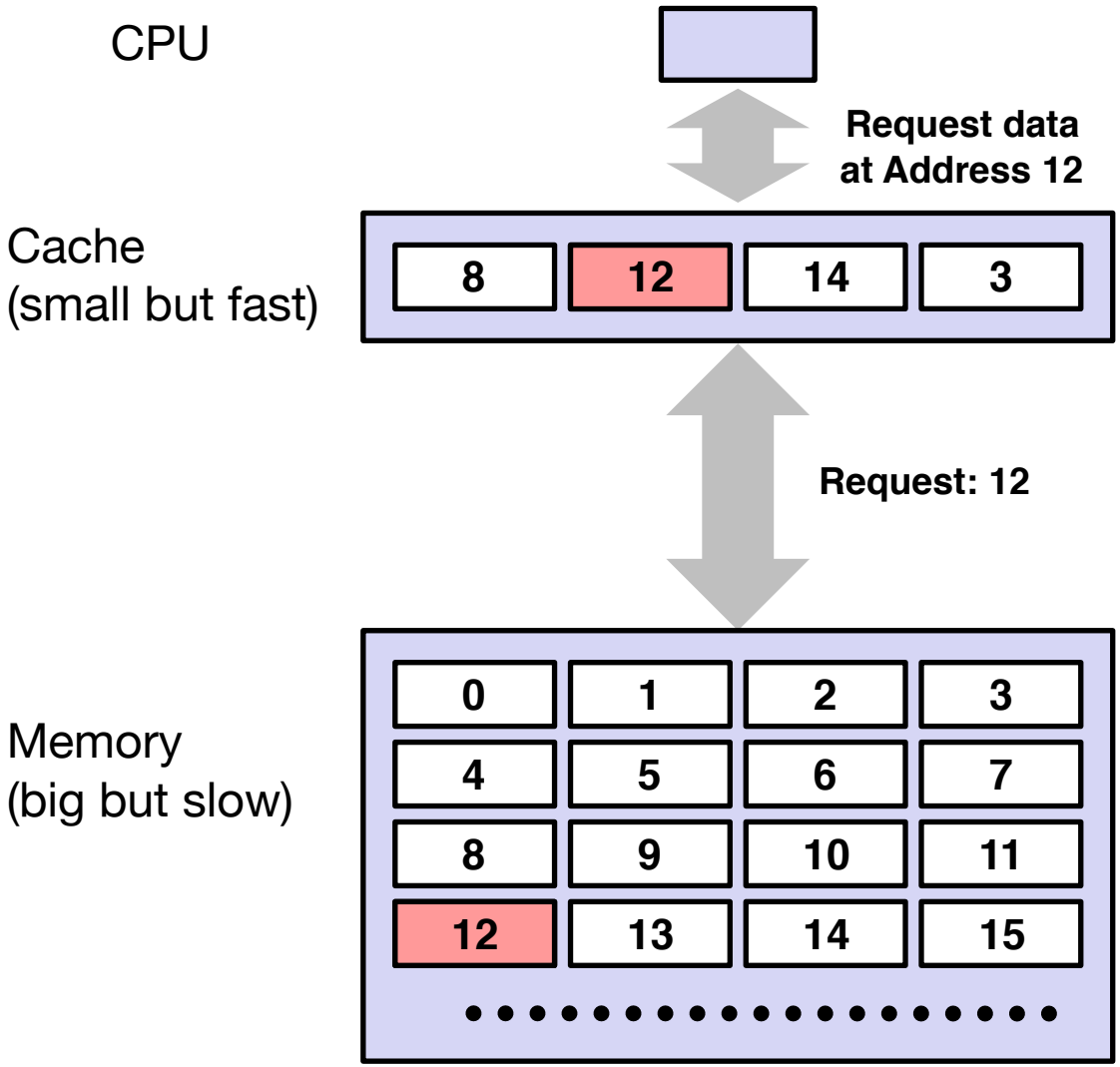


Data in address b is needed

Address b is not in cache: Miss!

Address b is fetched from memory

Address b is stored in cache

Cache Hit Rate

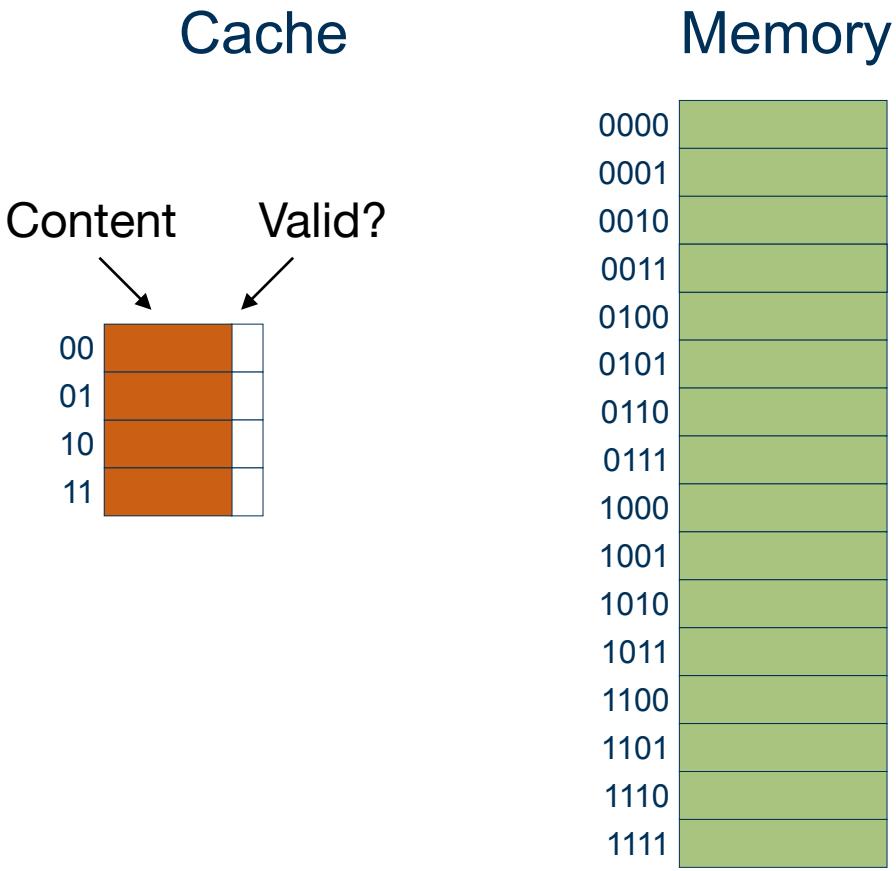
- Cache hit is when you find the data in the cache
- Hit rate indicates the effectiveness of the cache

$$\text{Hit Rate} = \frac{\#\ \text{Hits}}{\#\ \text{Accesses}}$$

Two Fundamental Issues in Cache Management

- Finding the data in the cache
  - Given an address, how do we decide whether it's in the cacher not?
- Kicking data out of the cache
  - Cache is small than memory, so when there's no place left in the cache, we need to kick something out before we can put new data into it, but who to kick out?

A Simple Cache



- 16 memory locations
- 4 cache locations

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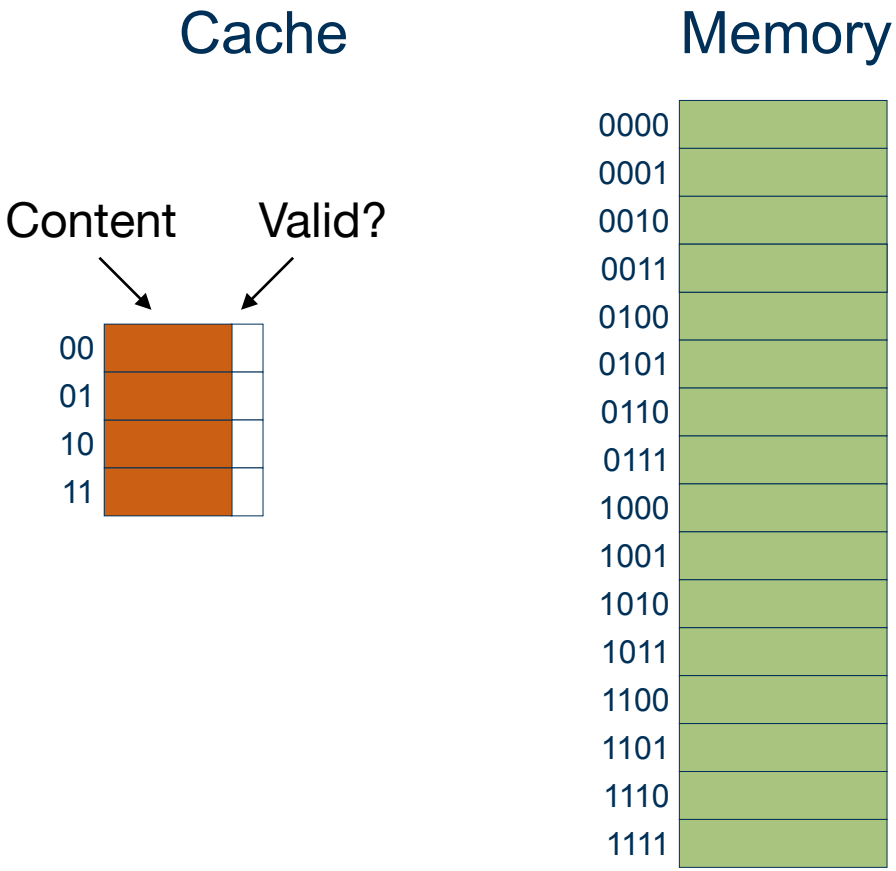

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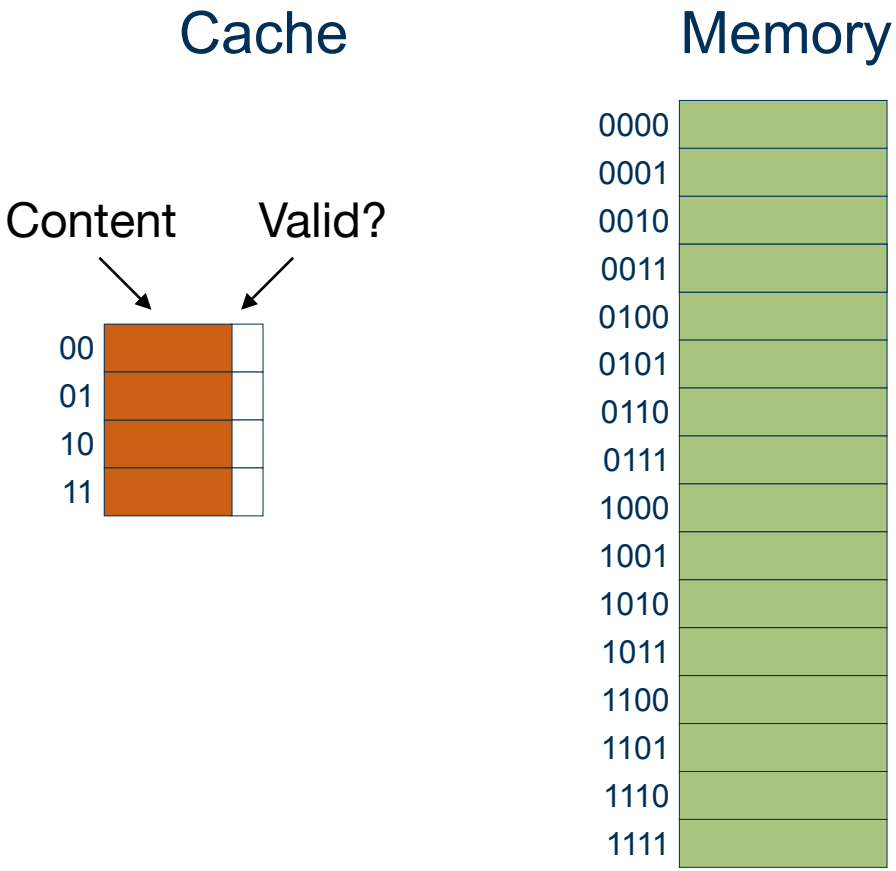

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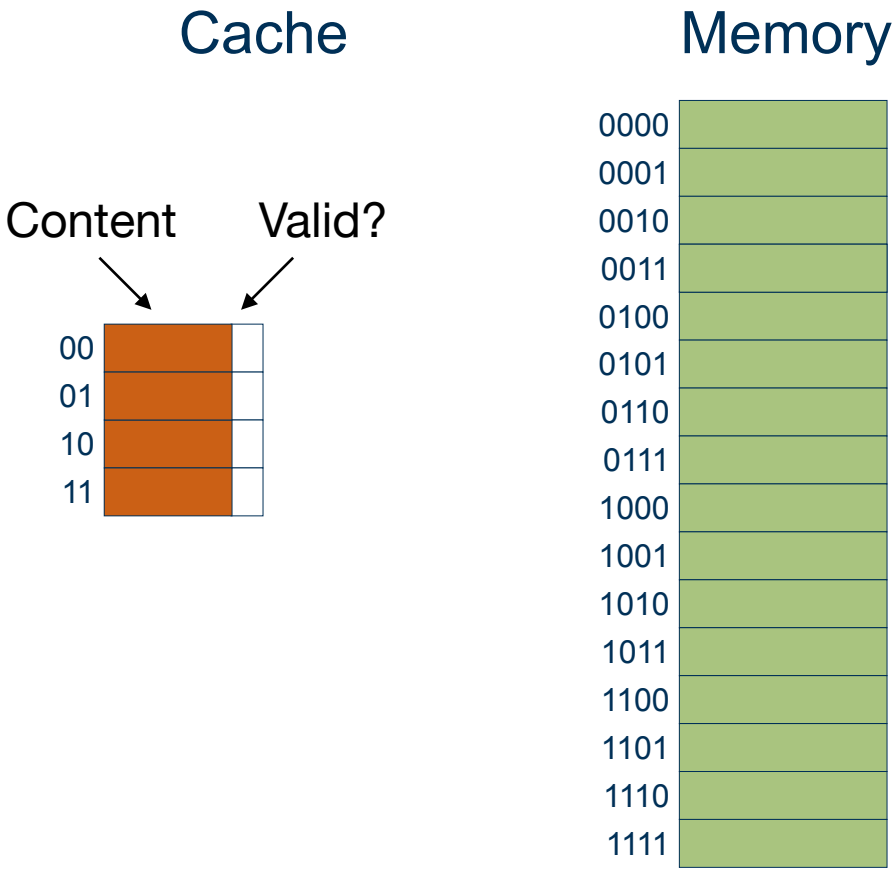

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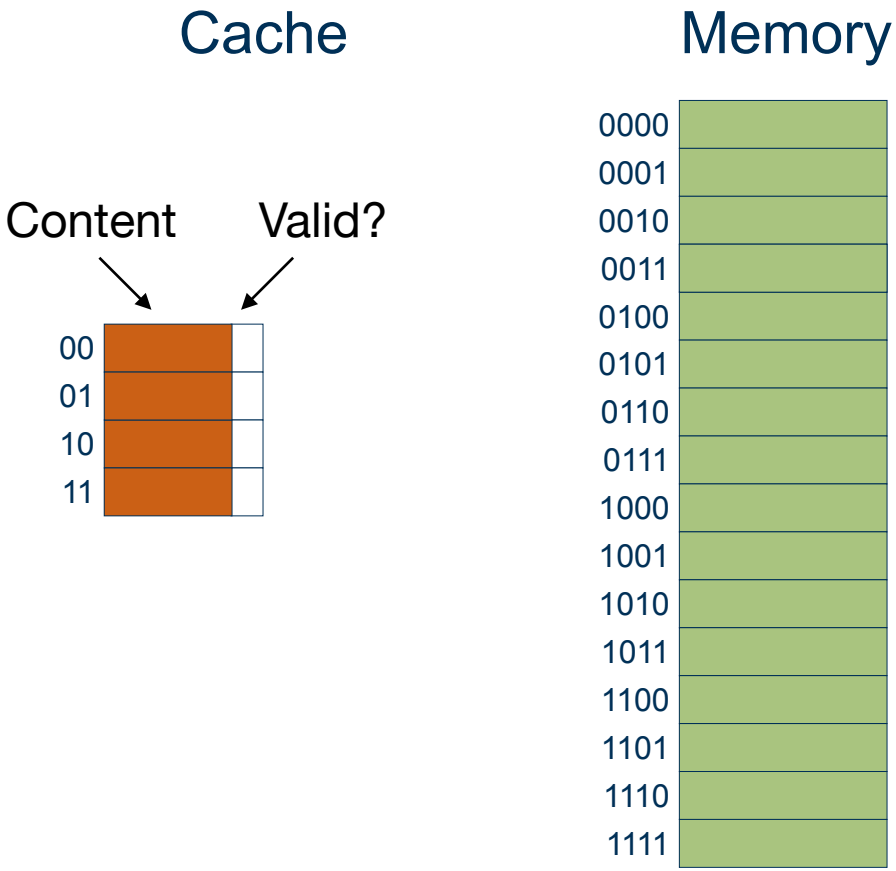

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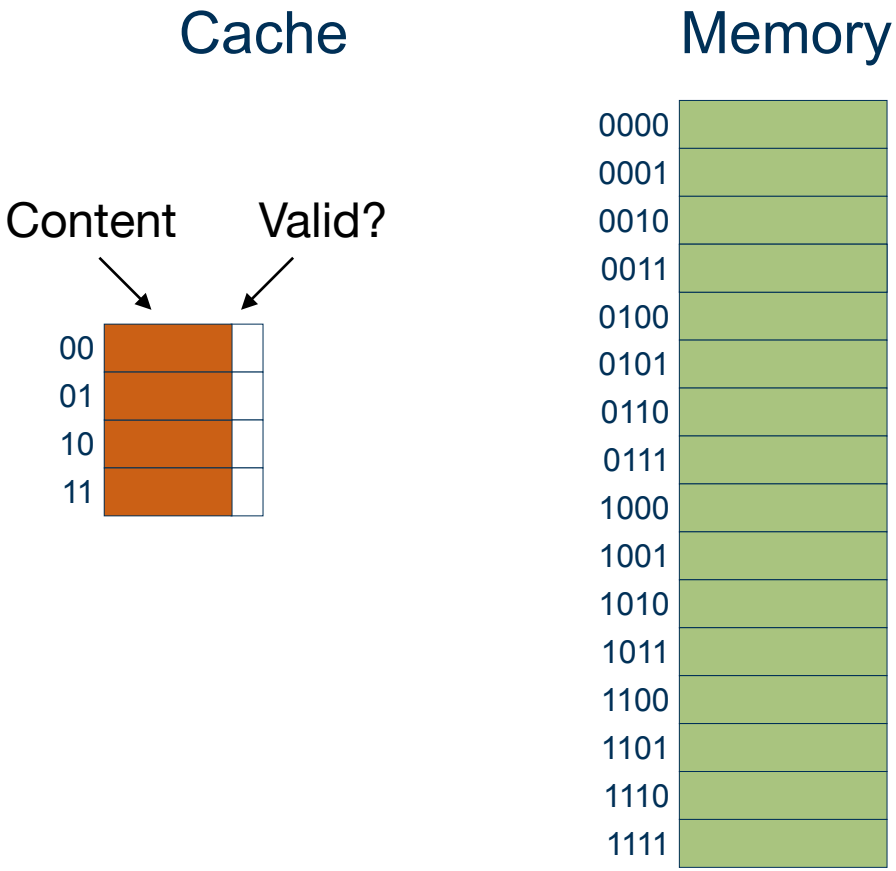

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- Cache is smaller than memory (obviously)

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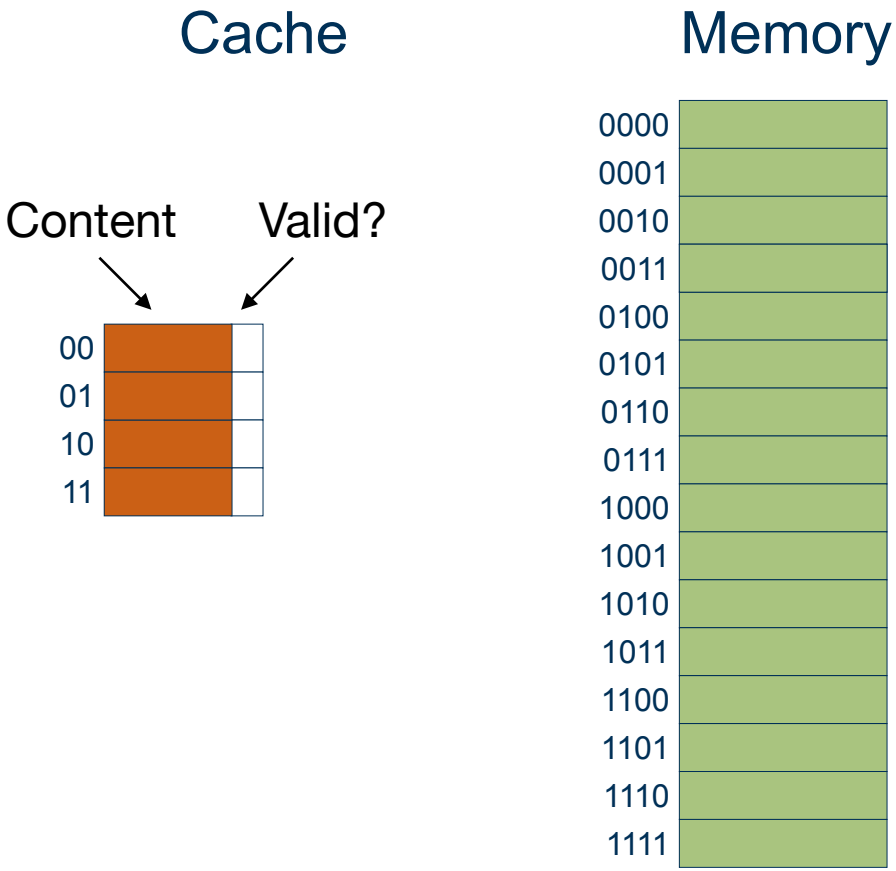

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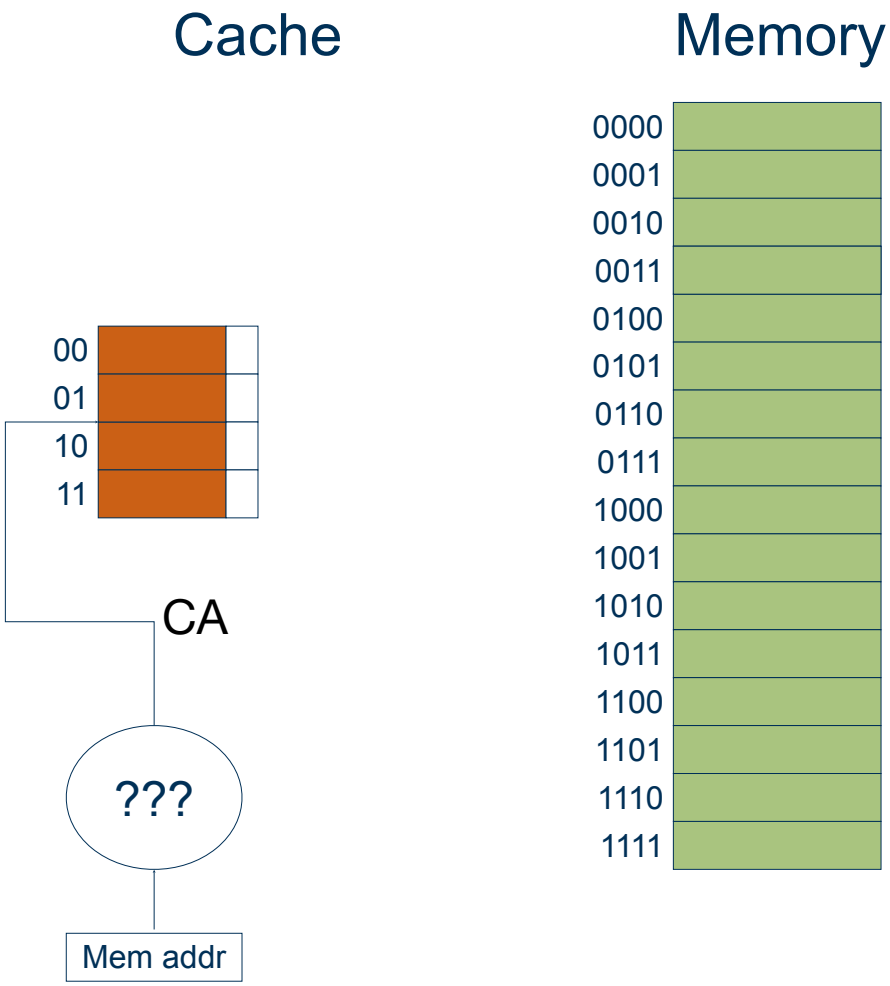
- Cache is smaller than memory (obviously)
  - Thus, not all memory locations can be cached at the same time

Cache Placement



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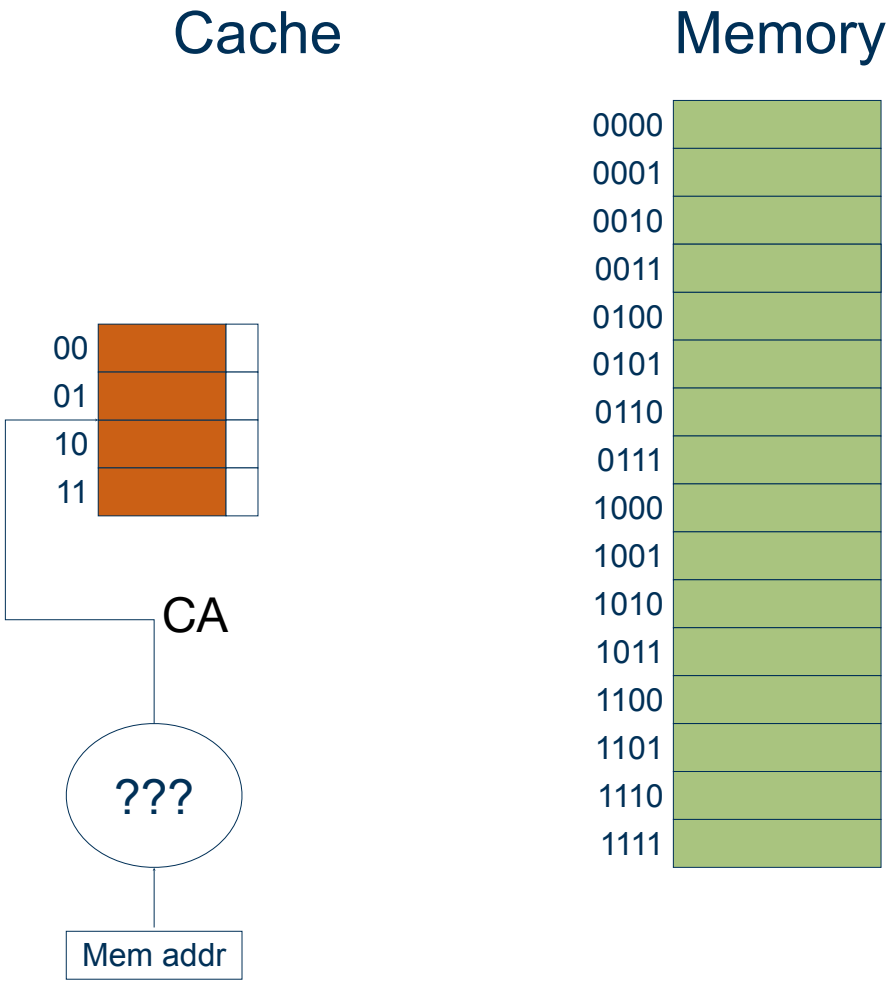
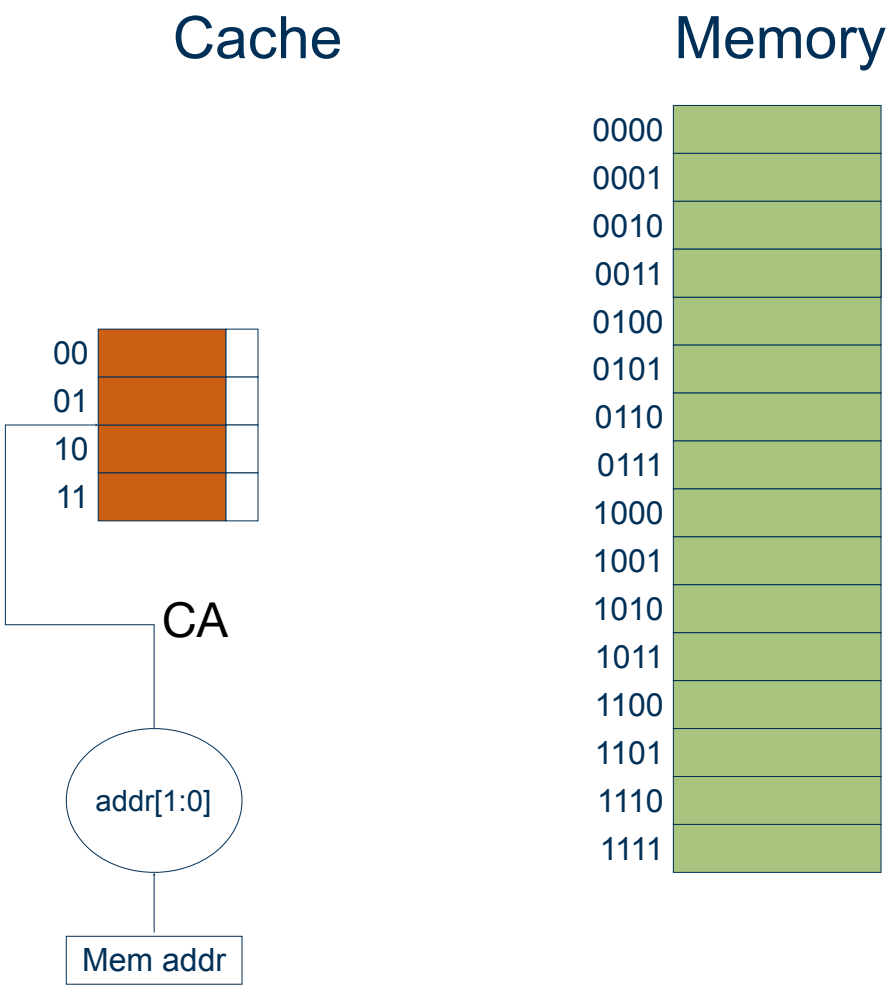


- Given a memory addr, say 0x0001, we want to put the data there into the cache; where does the data go?

Function to Address Cache



- Simplest way is to take a subset of address bits
- Six combinations in total
  - CA = ADDR[3],ADDR[2]
  - CA = ADDR[3],ADDR[1]
  - CA = ADDR[3],ADDR[0]
  - CA = ADDR[2],ADDR[1]
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- Direct-Mapped Cache
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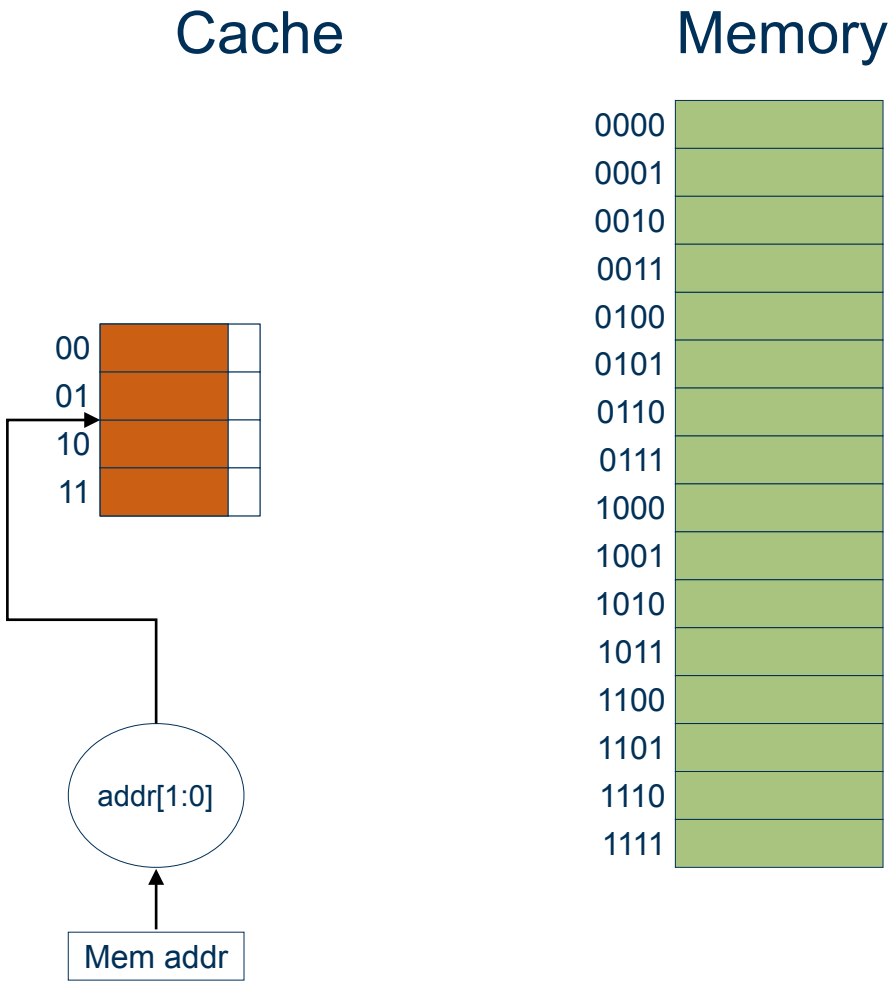
Direct-Mapped Cache



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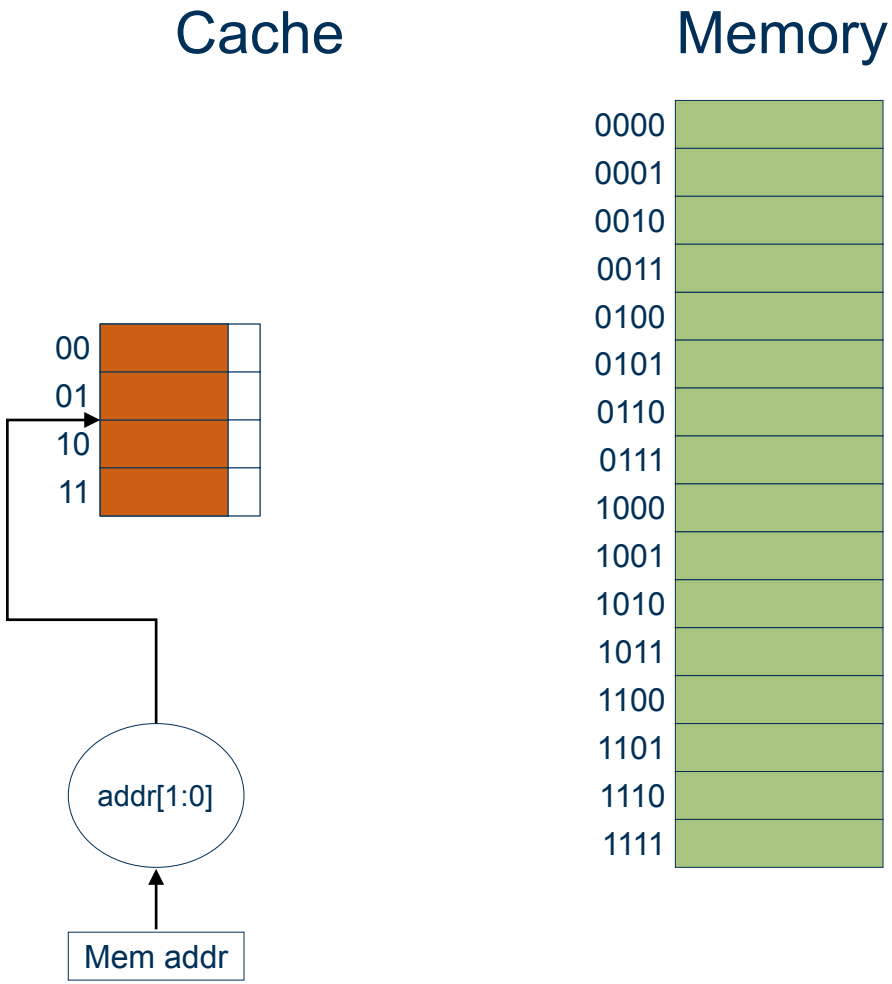

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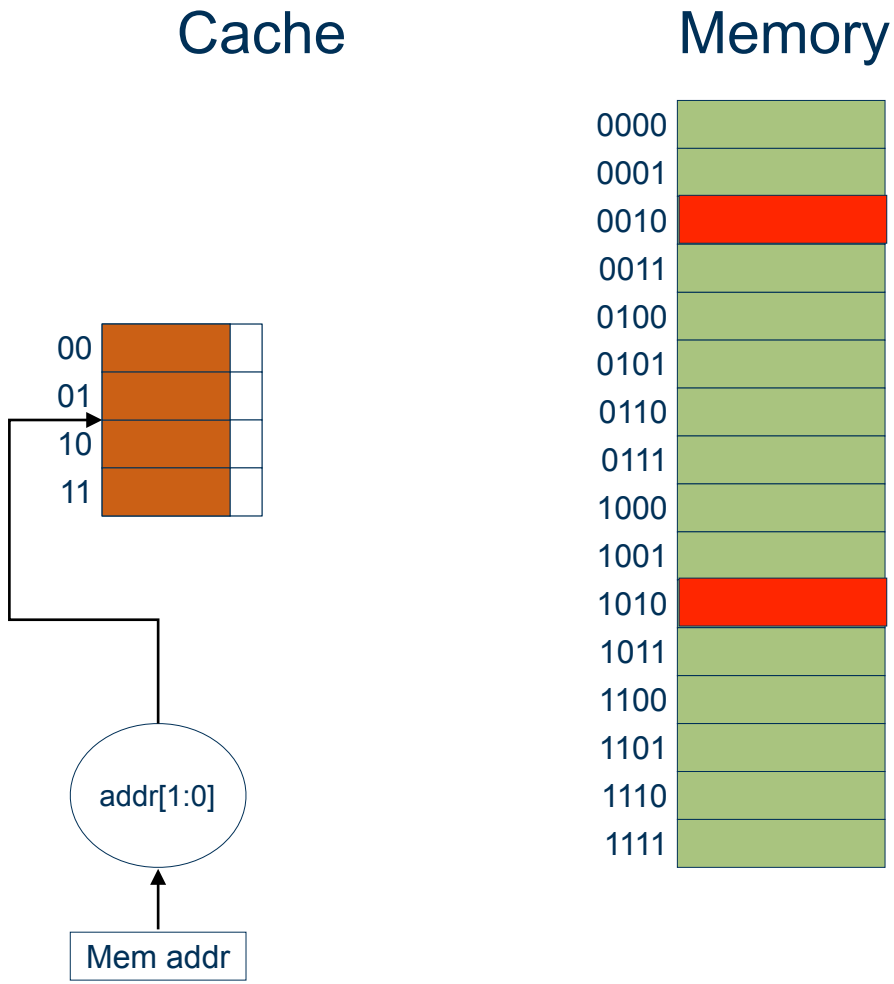

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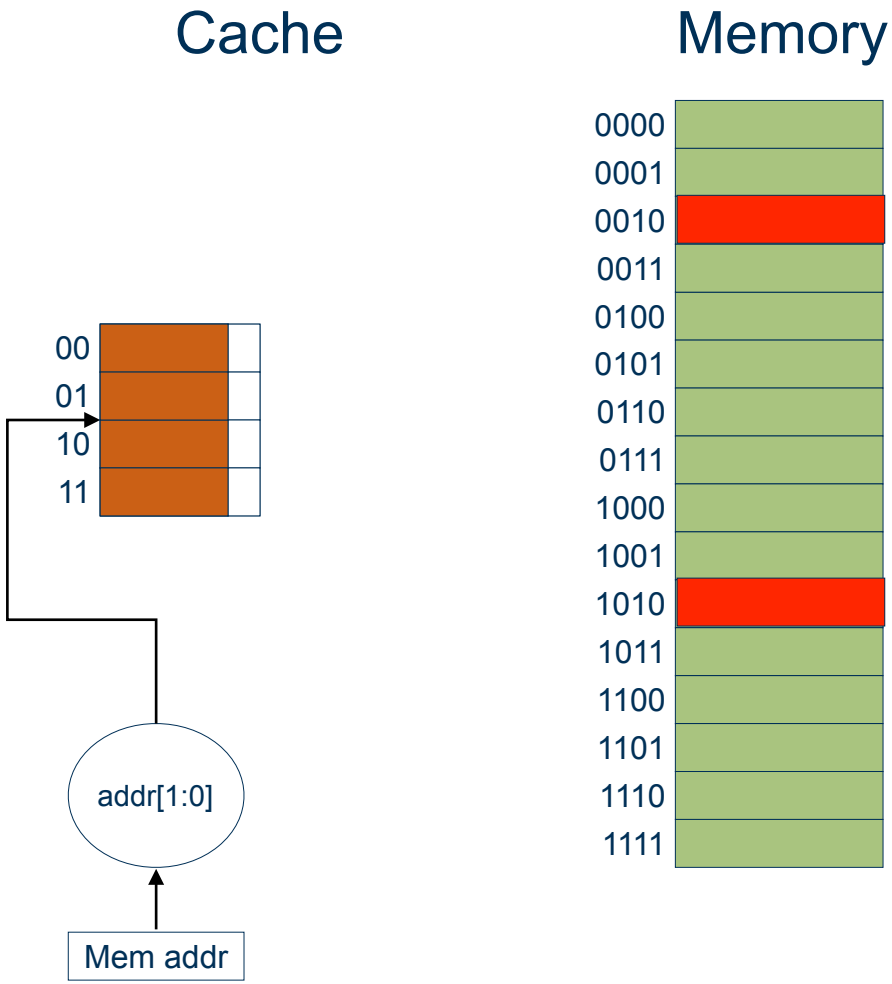

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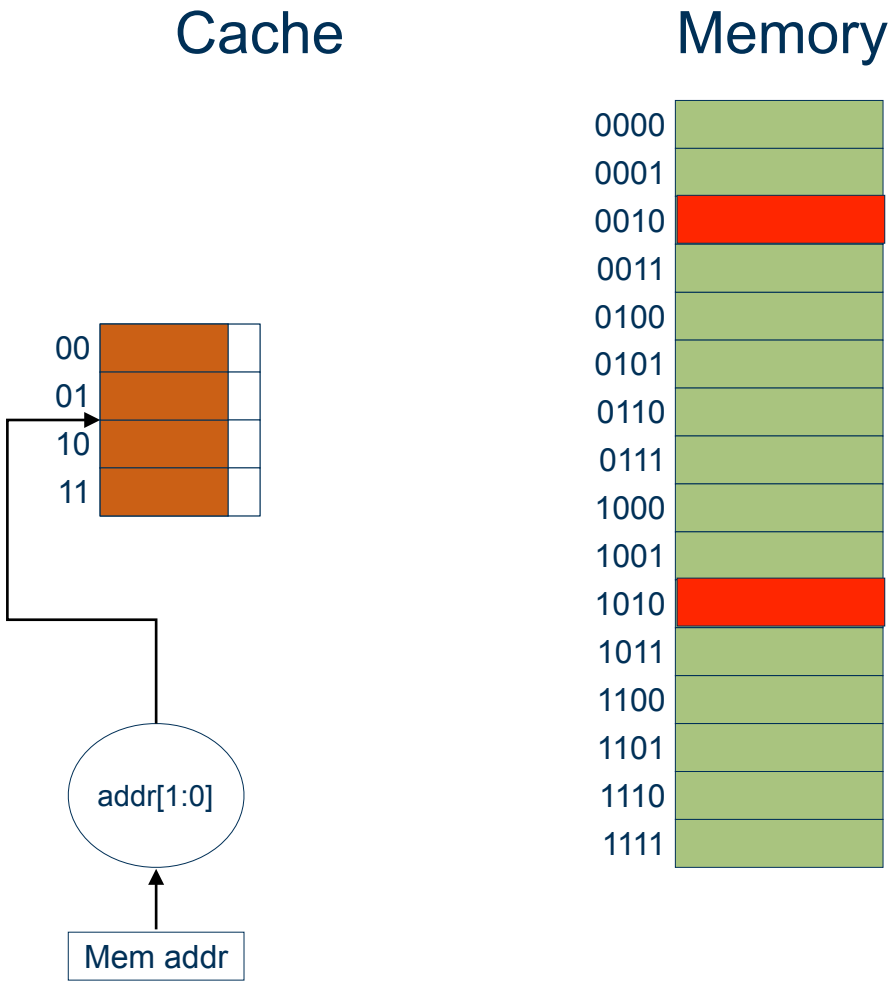
Direct-Mapped Cache



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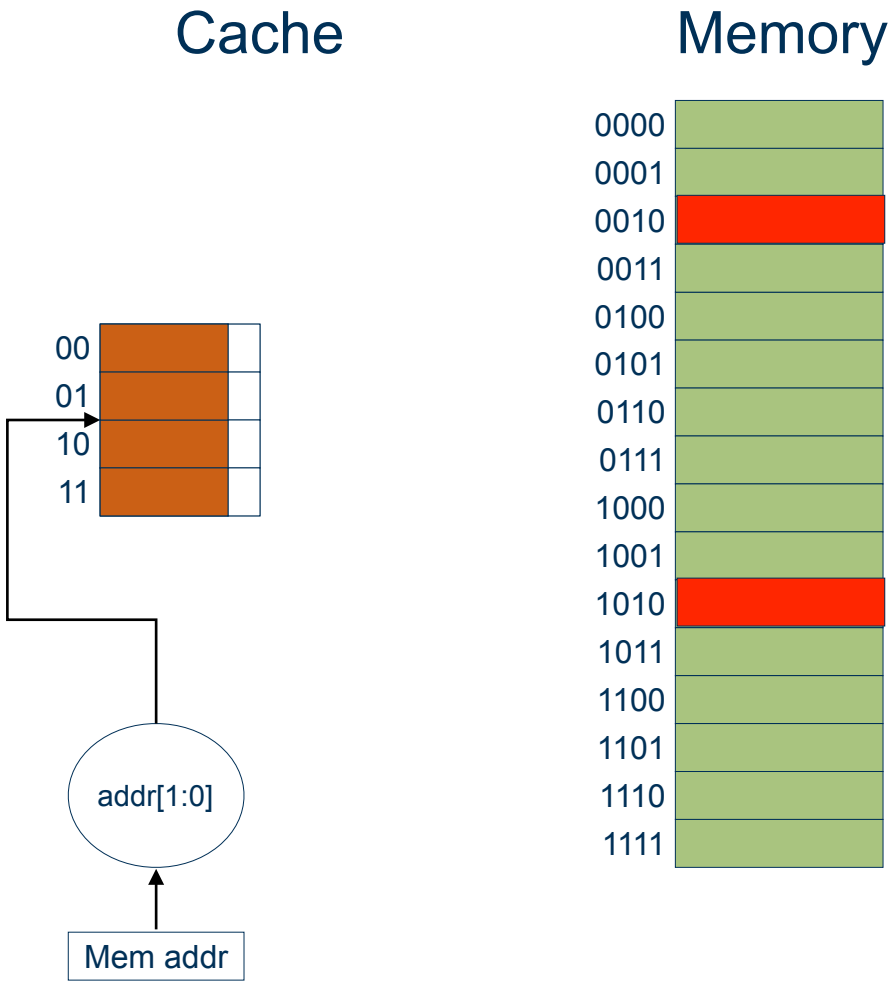
Direct-Mapped Cache



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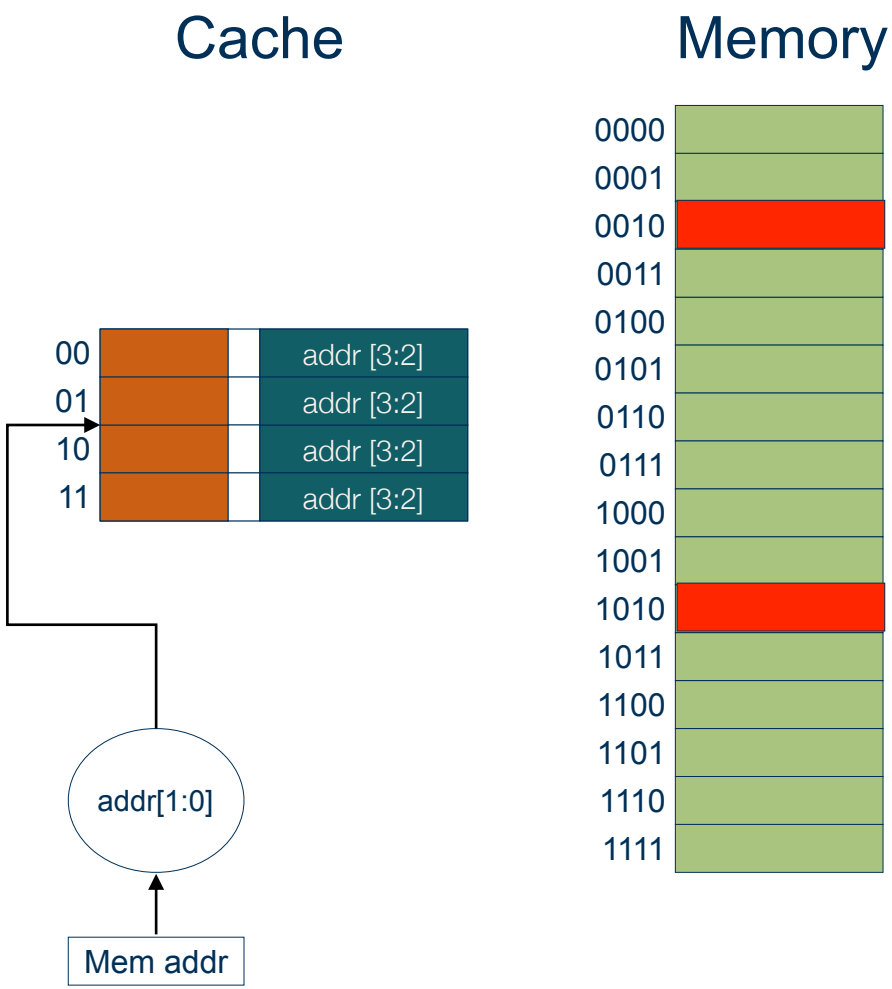

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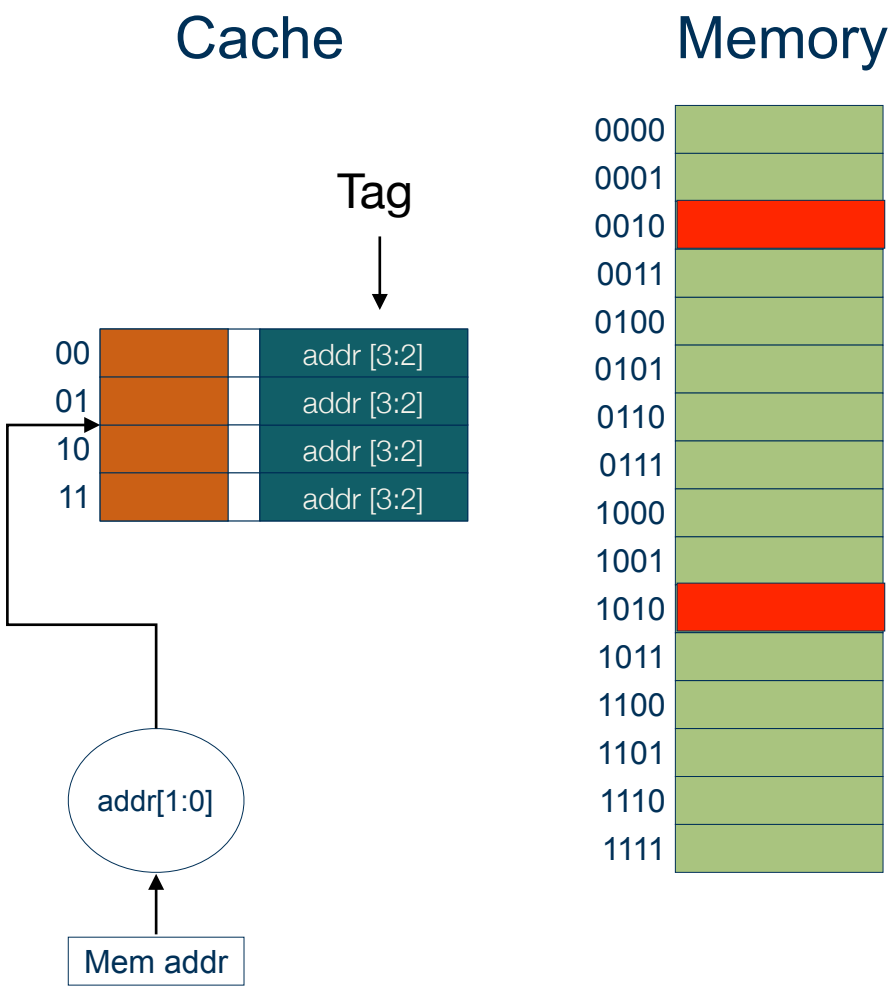

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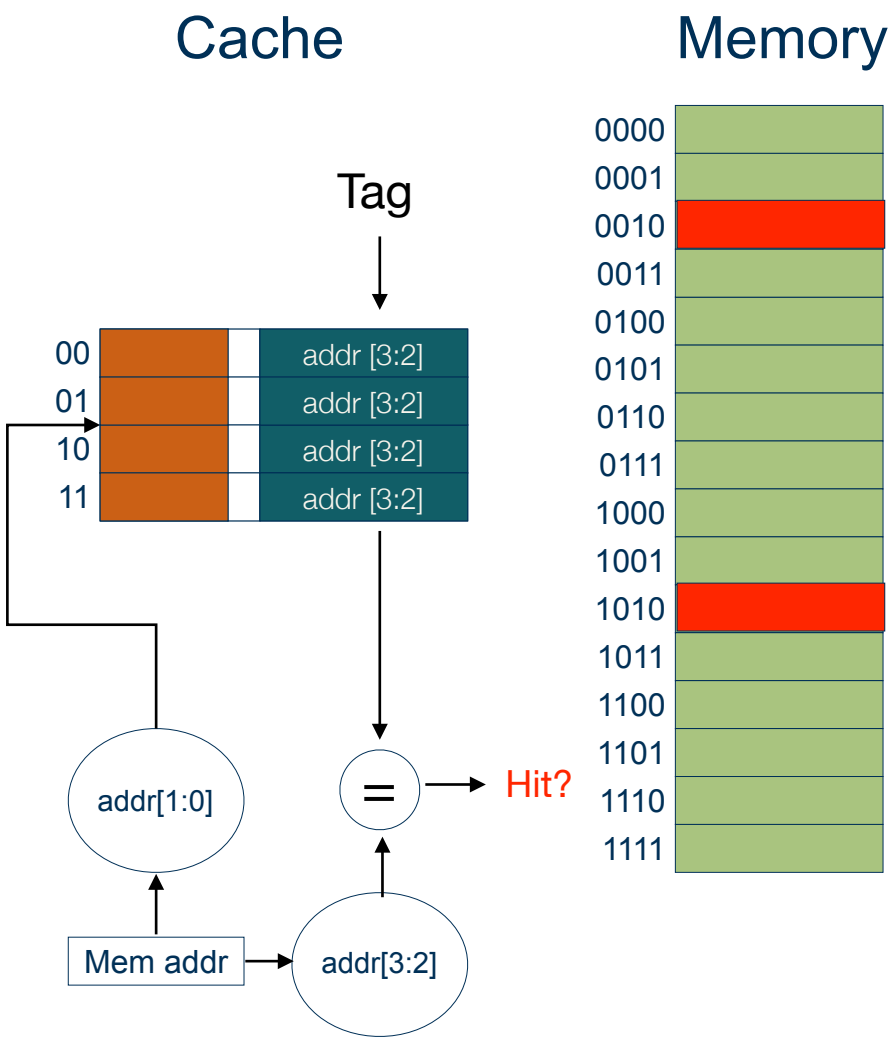

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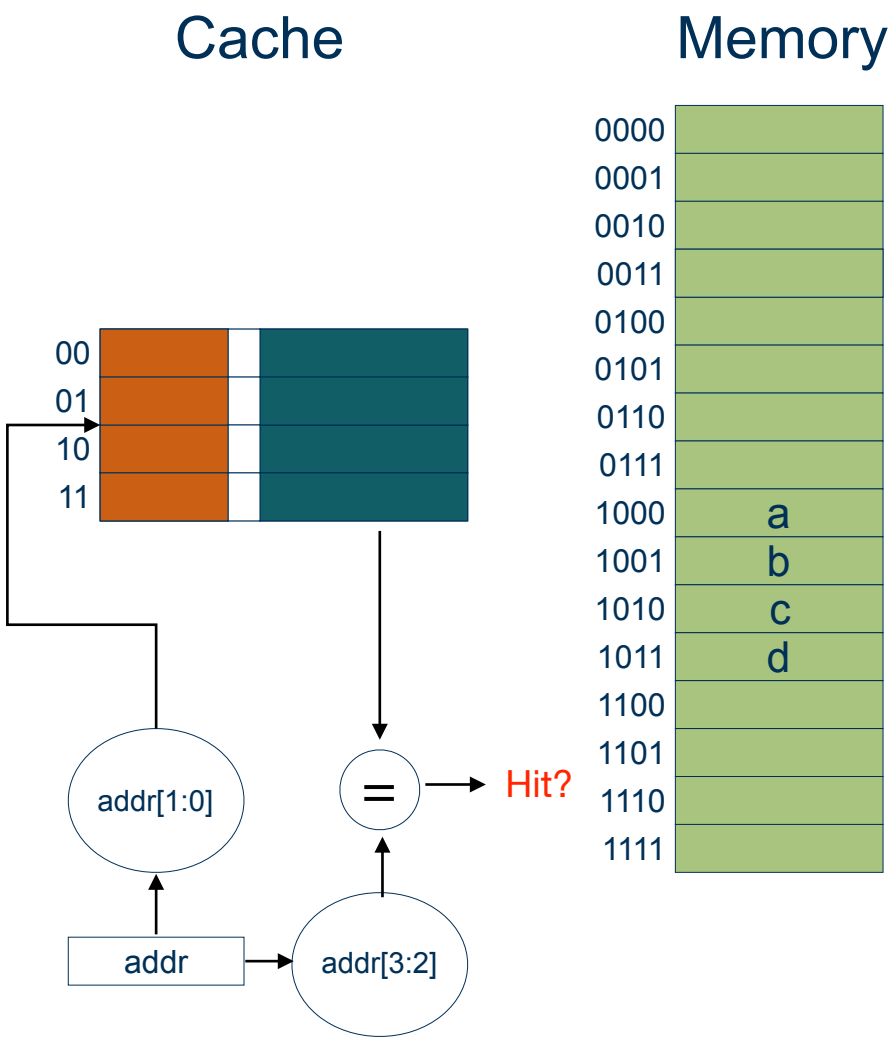
Example: Direct-Mapped Cache

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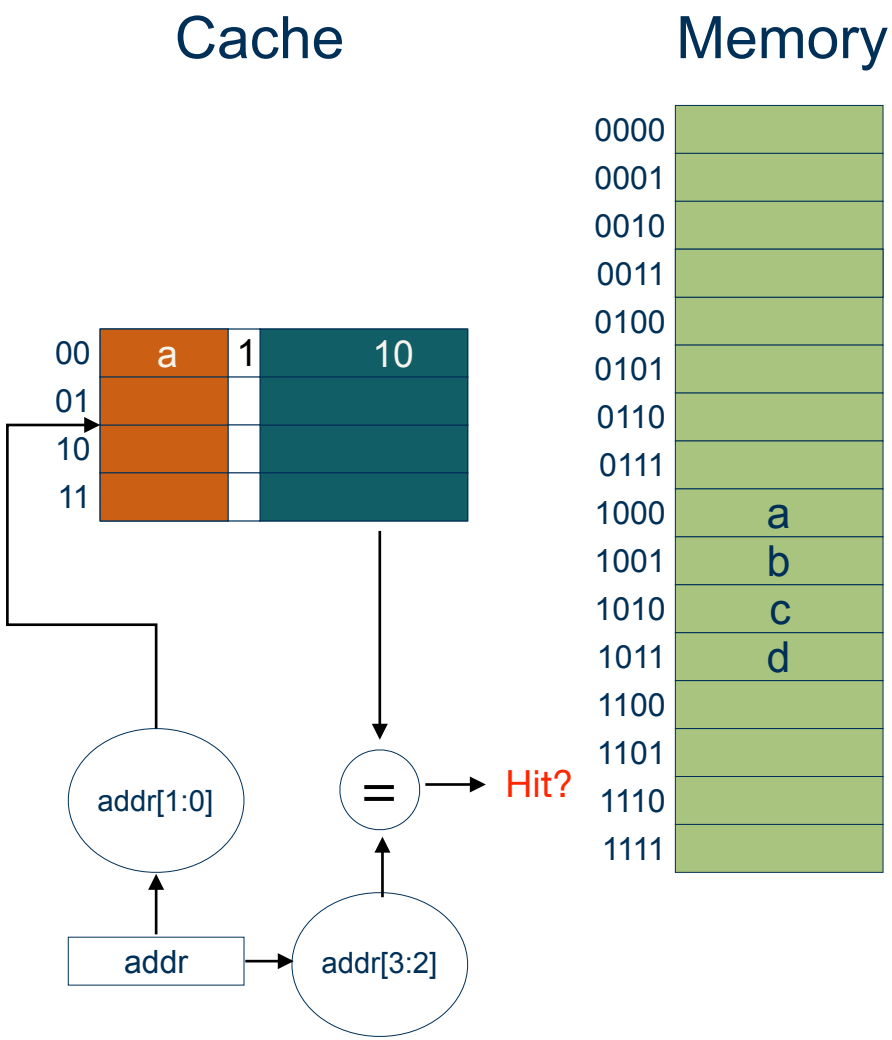


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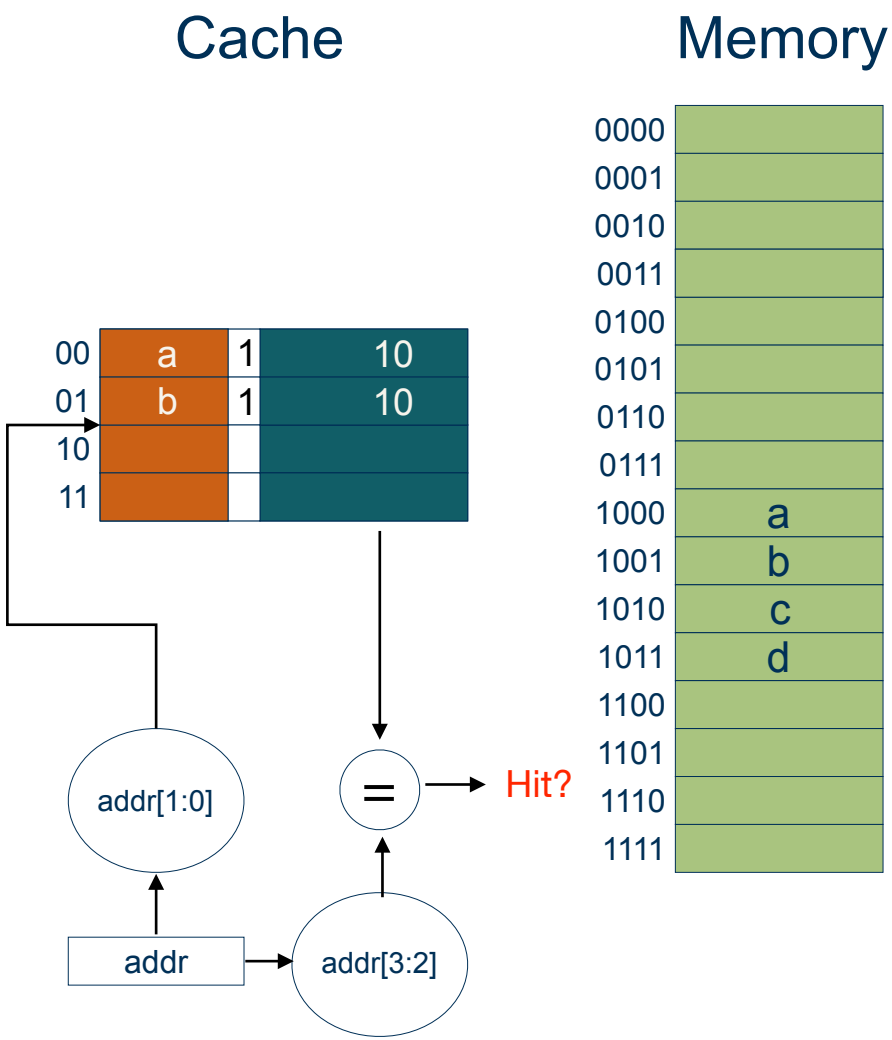


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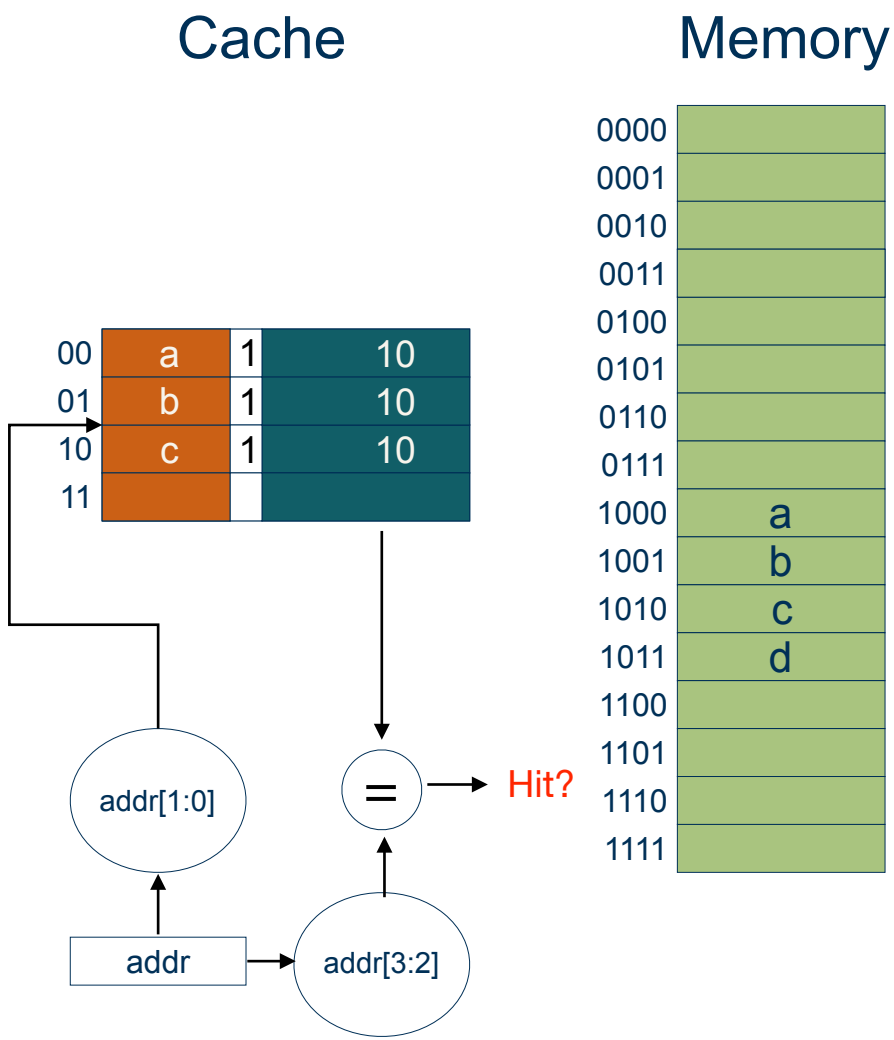


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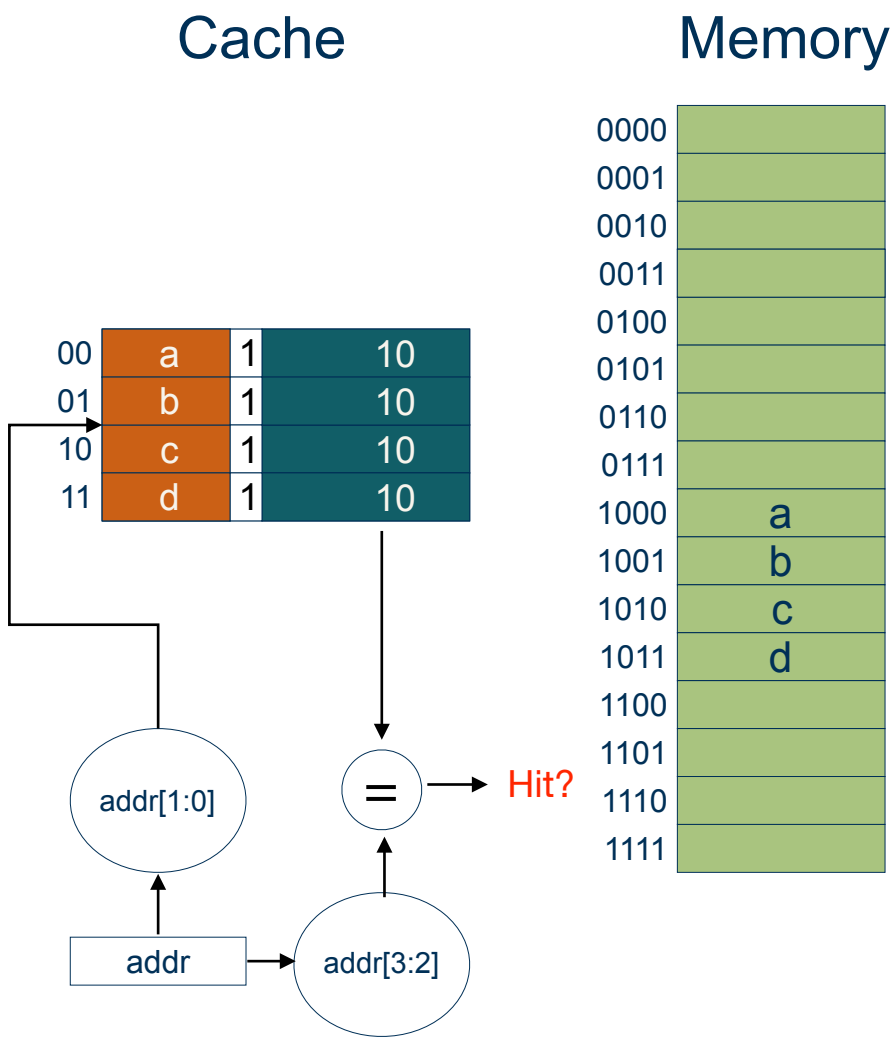


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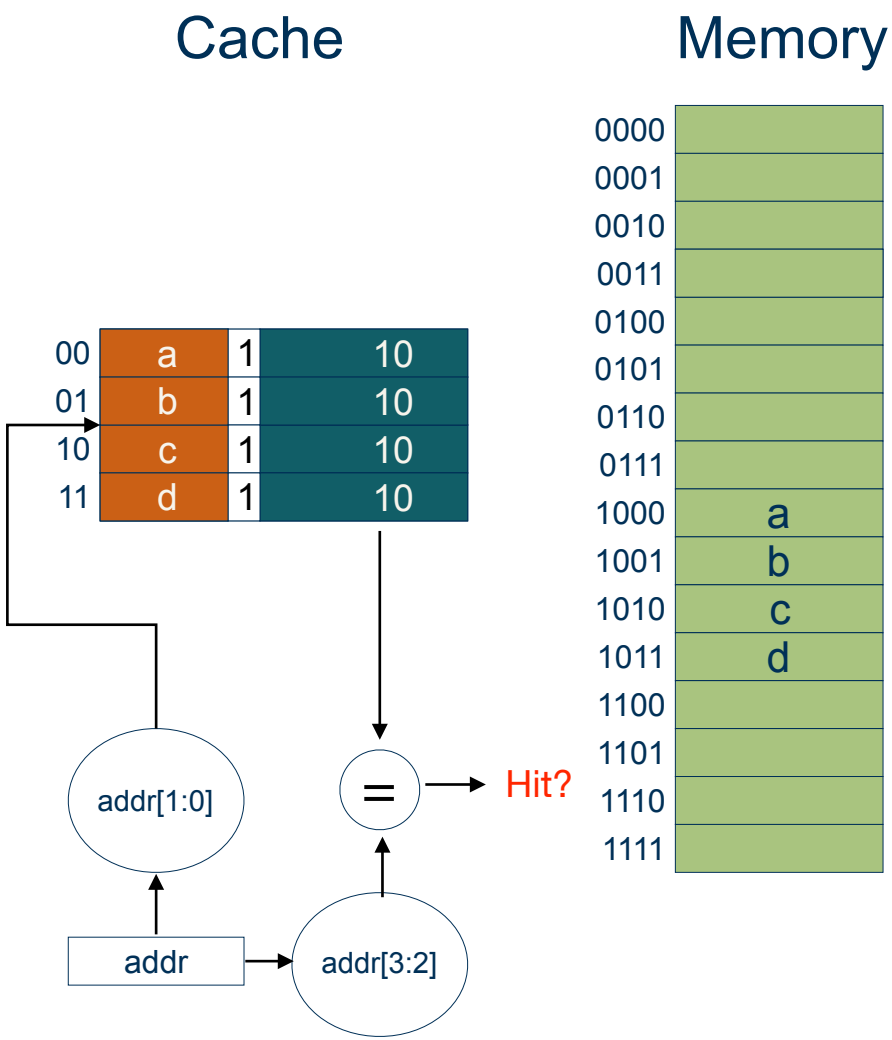


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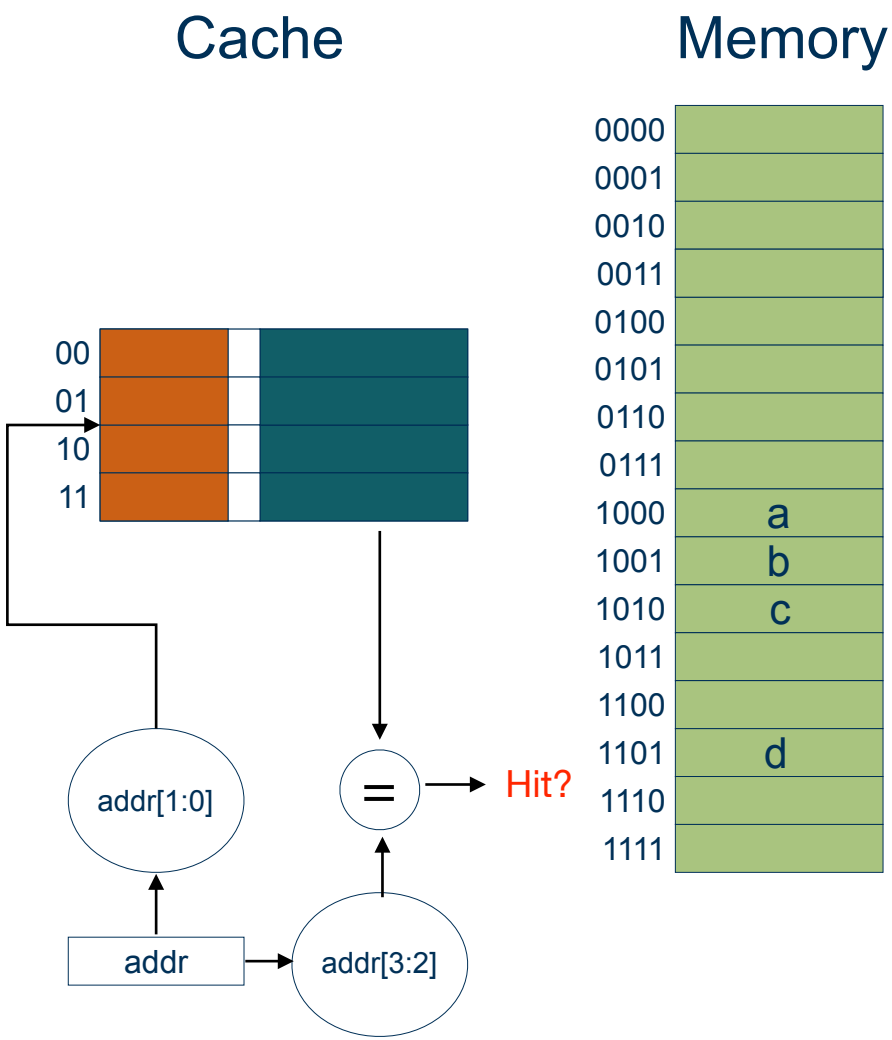

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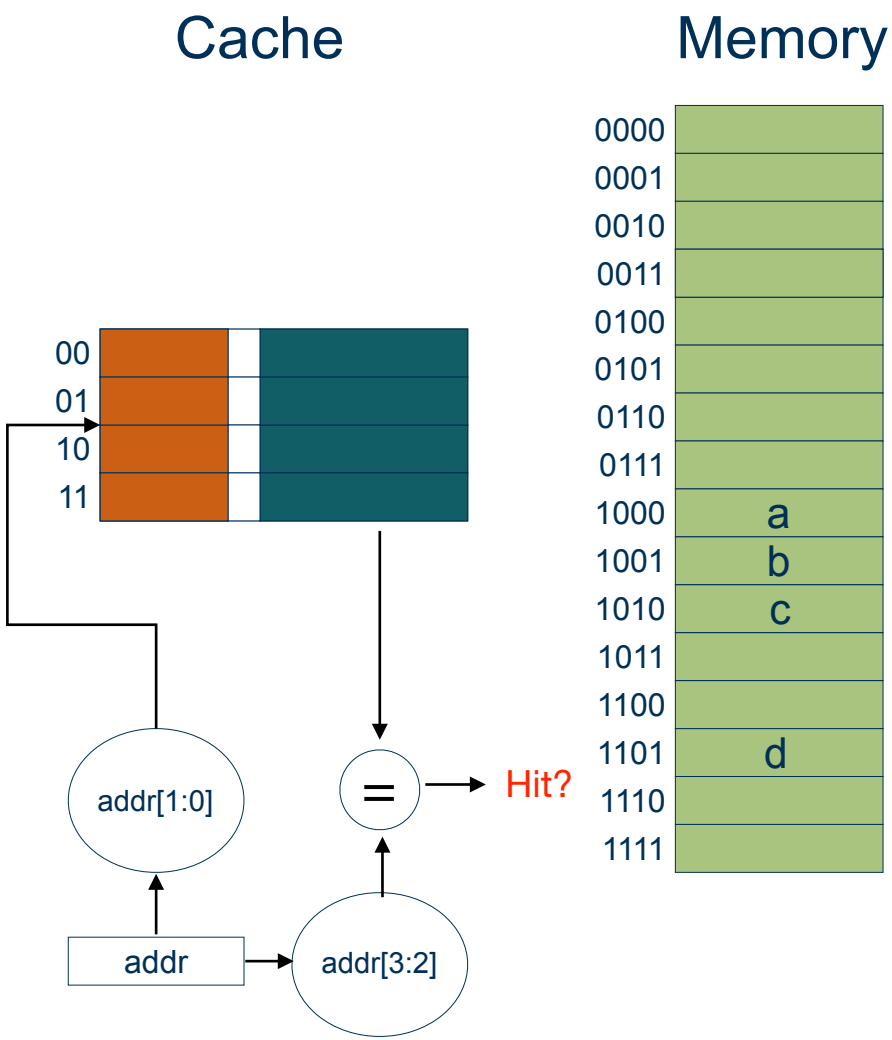

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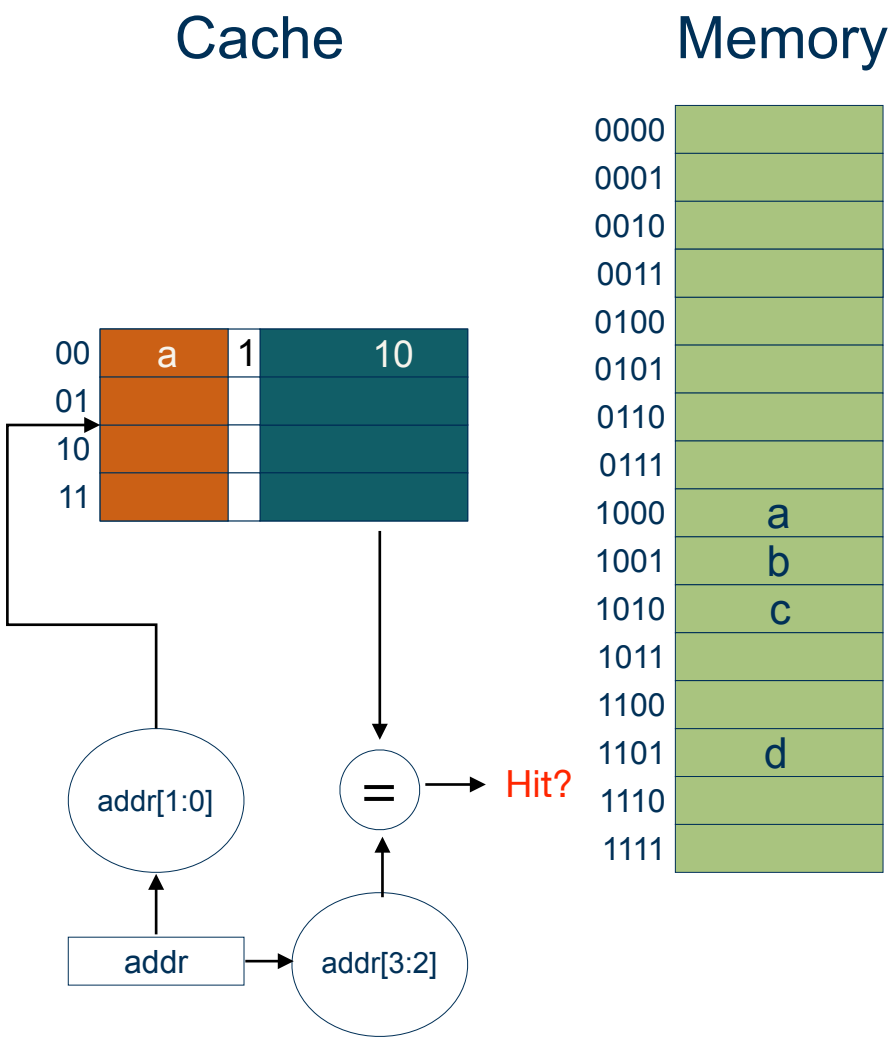

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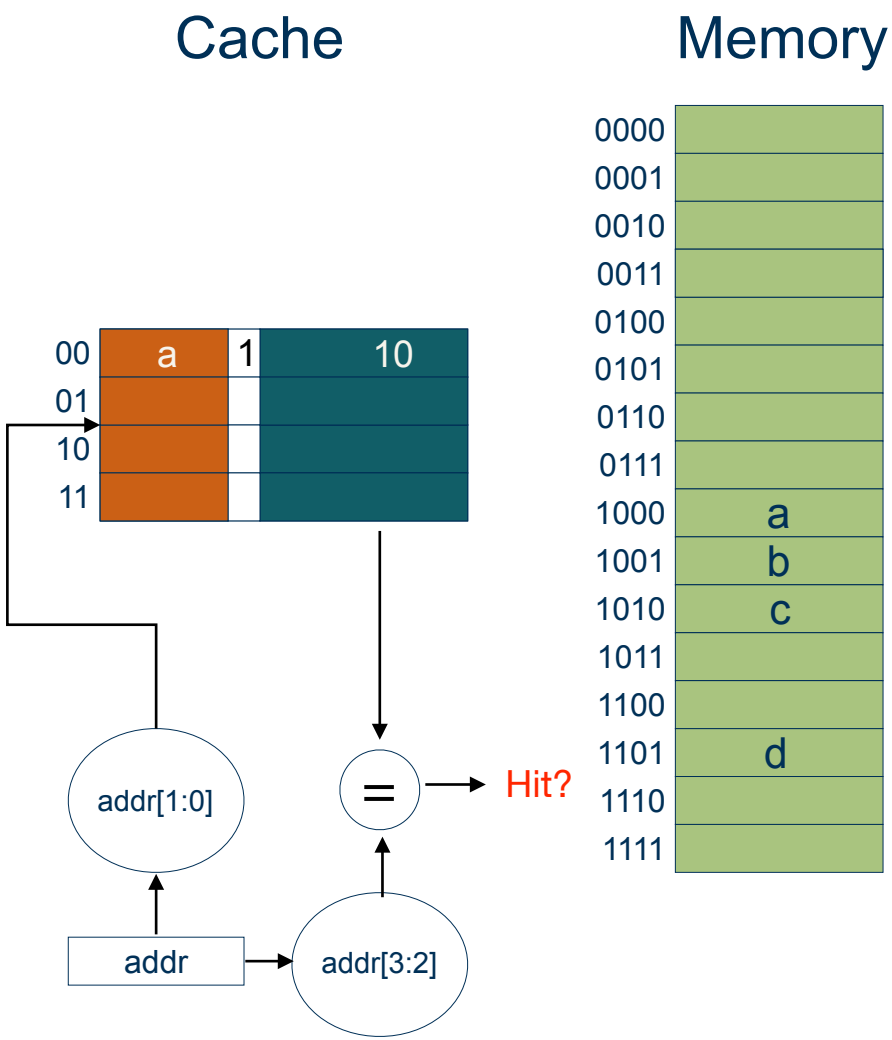

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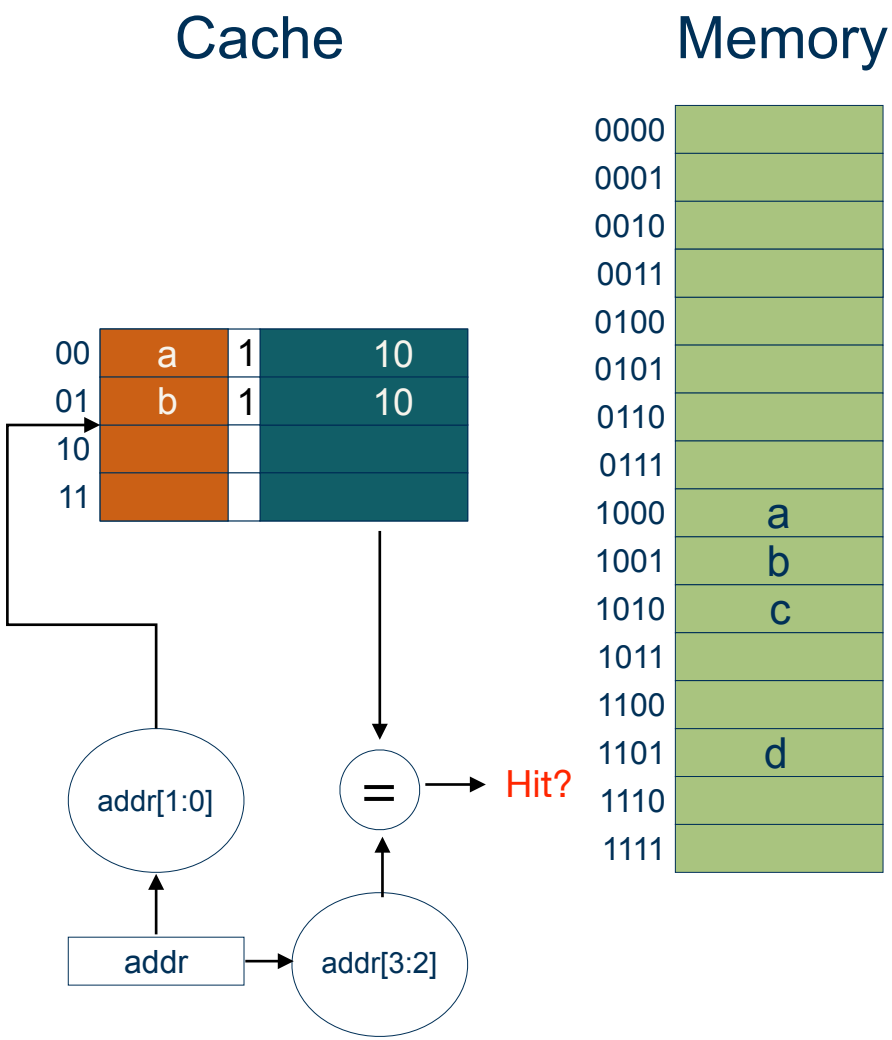

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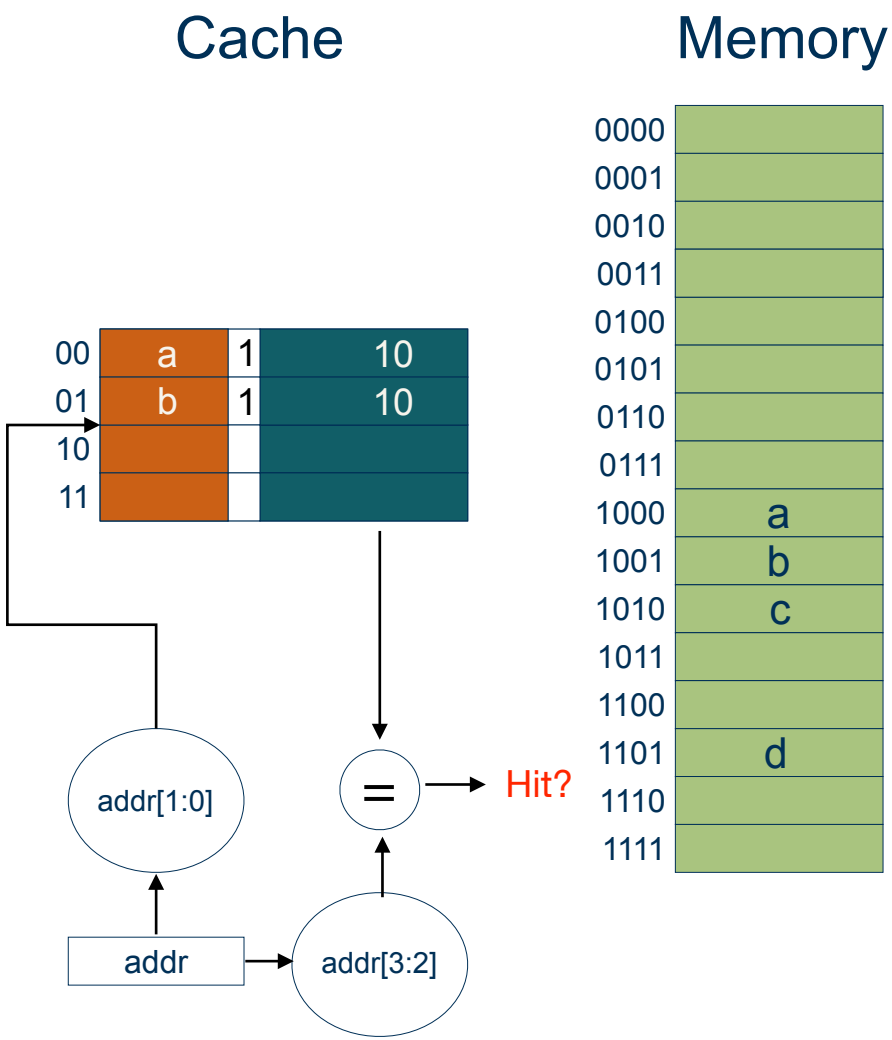

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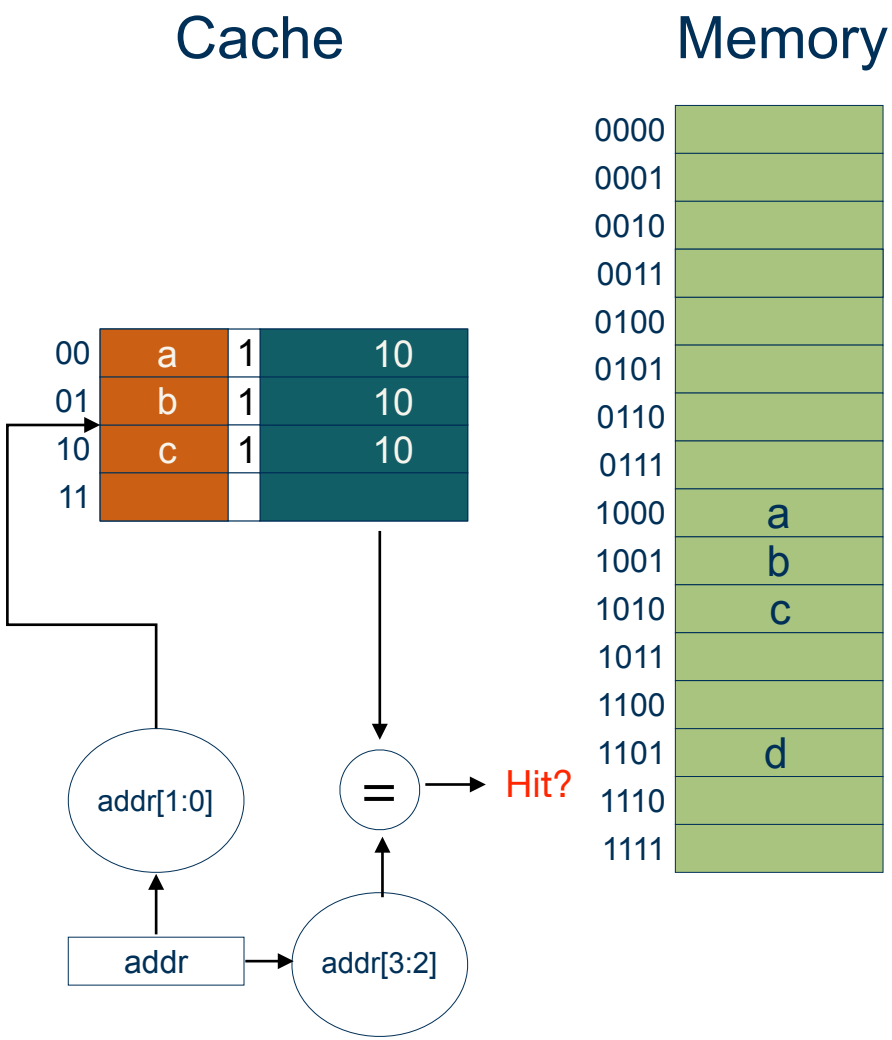

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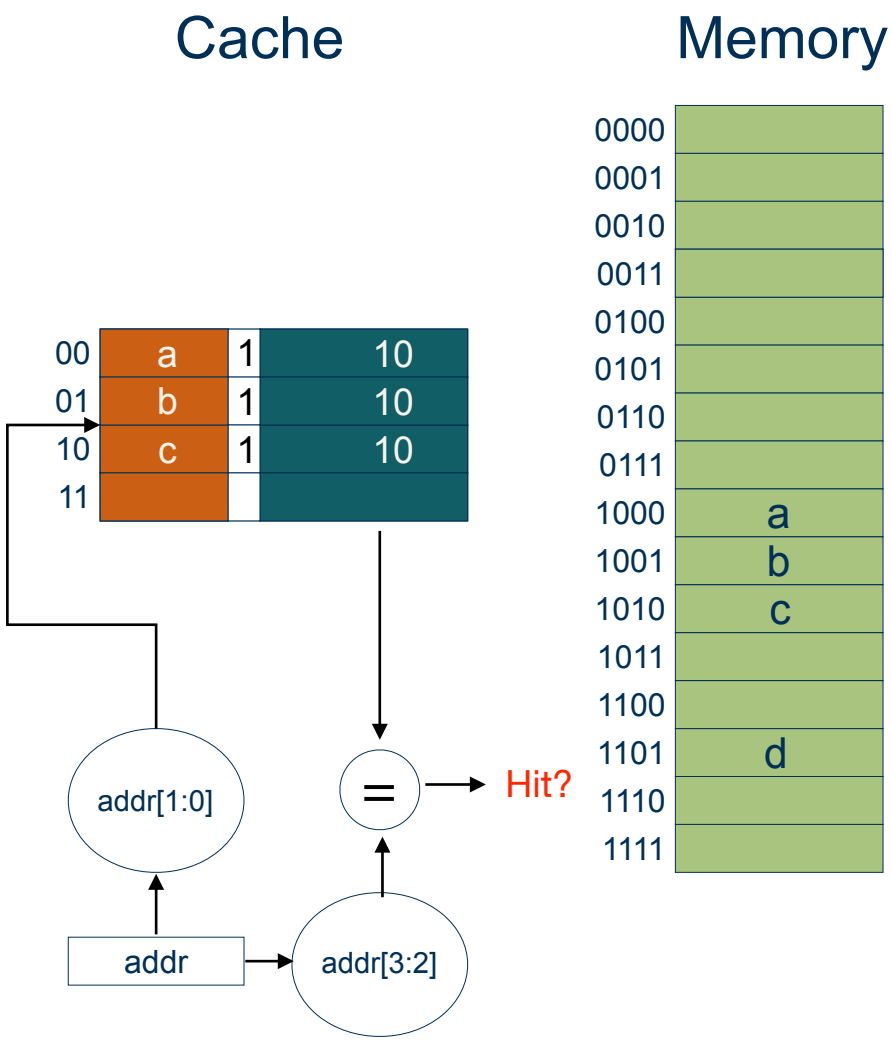

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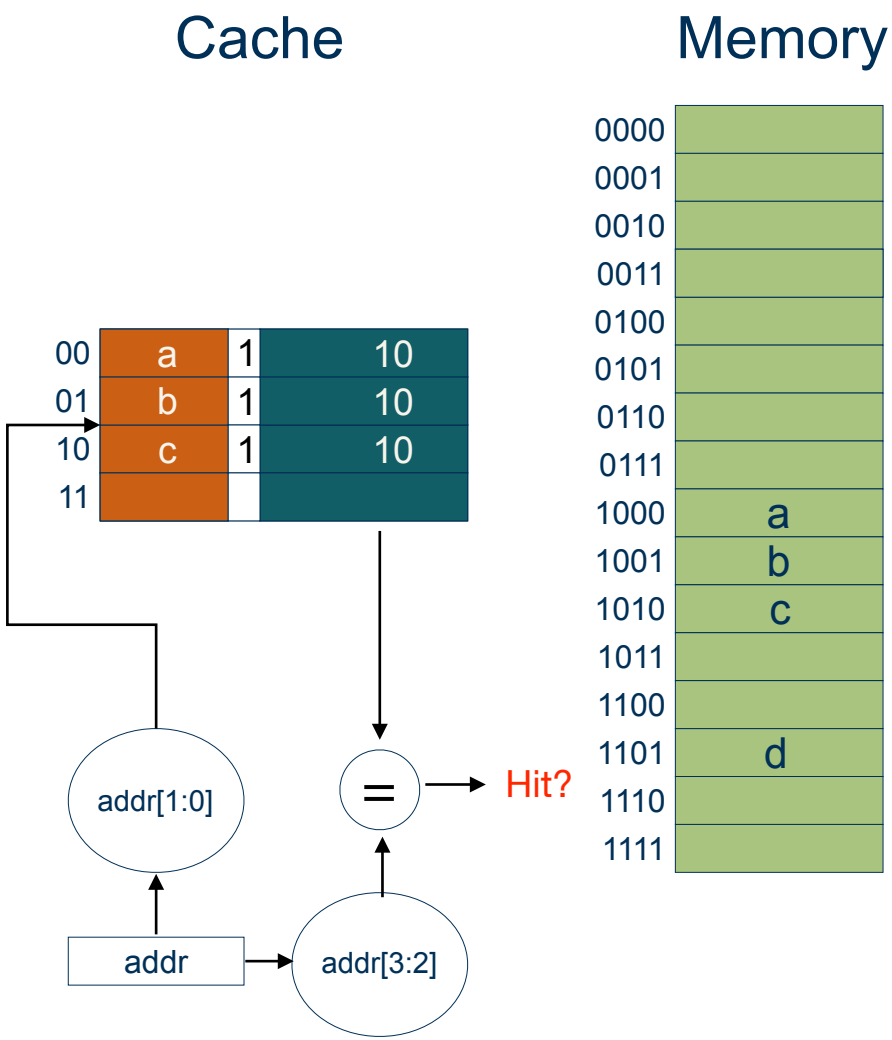

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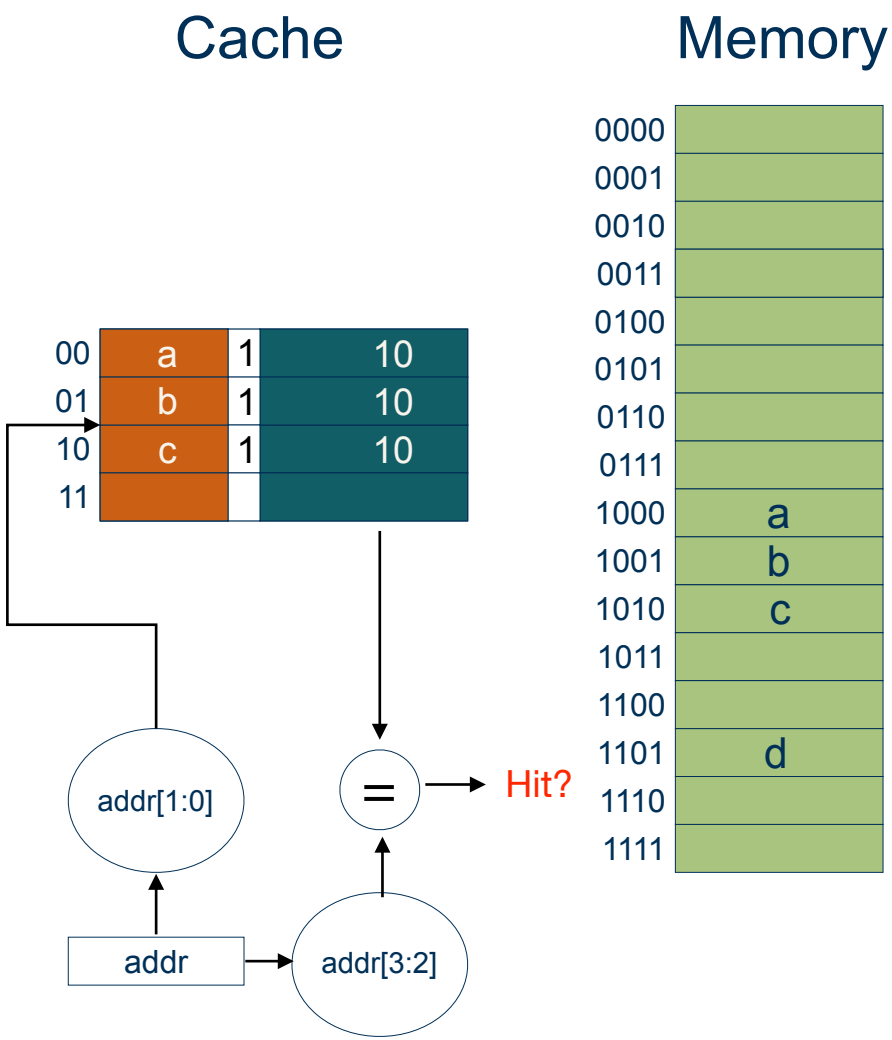

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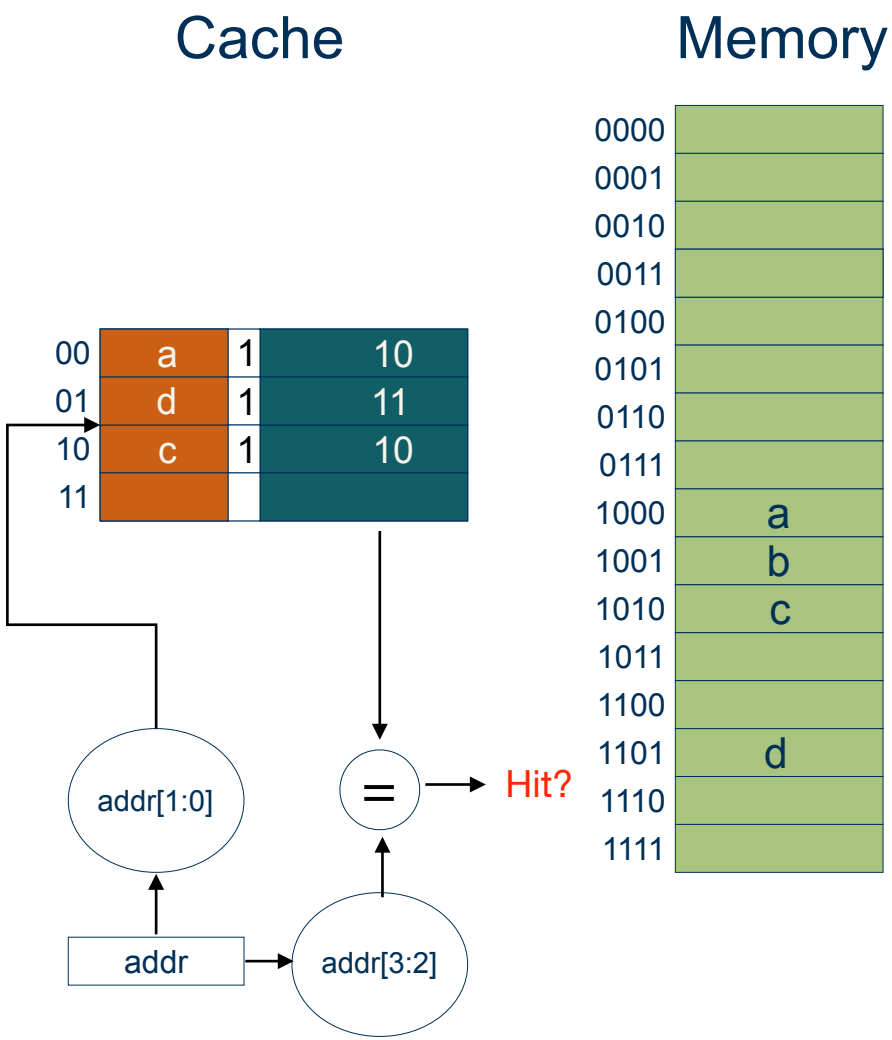

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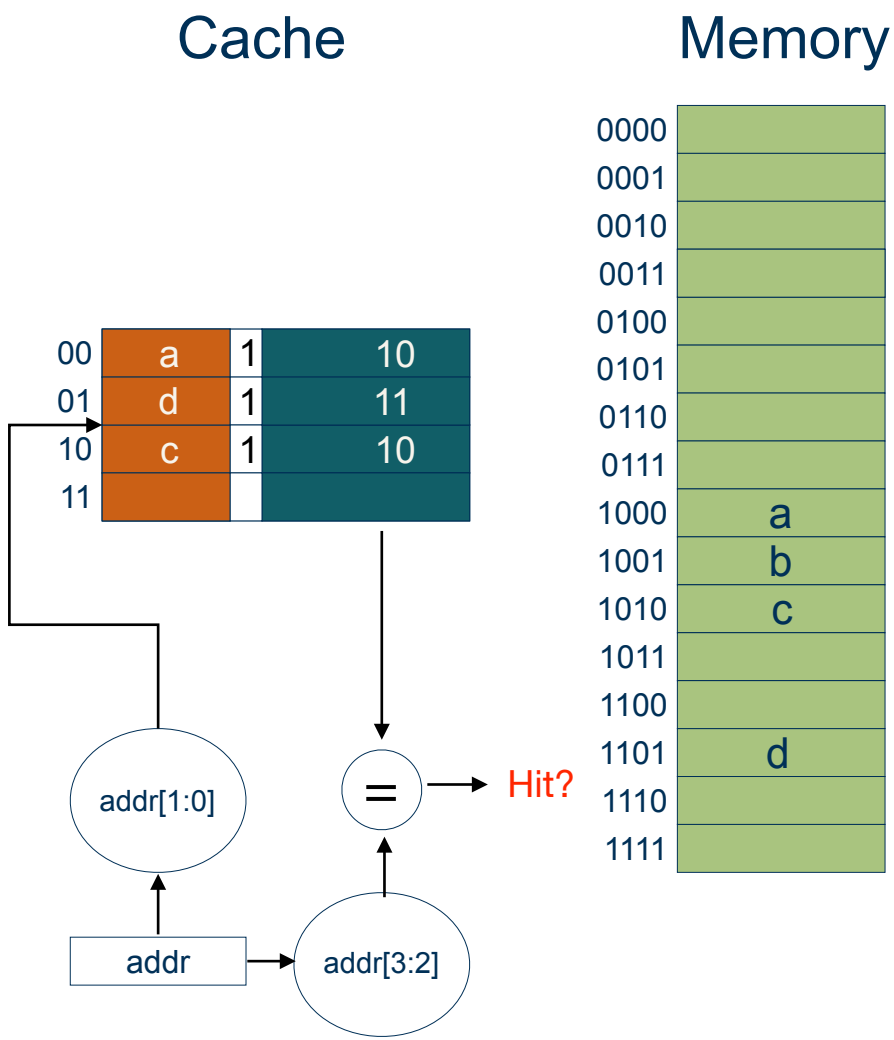

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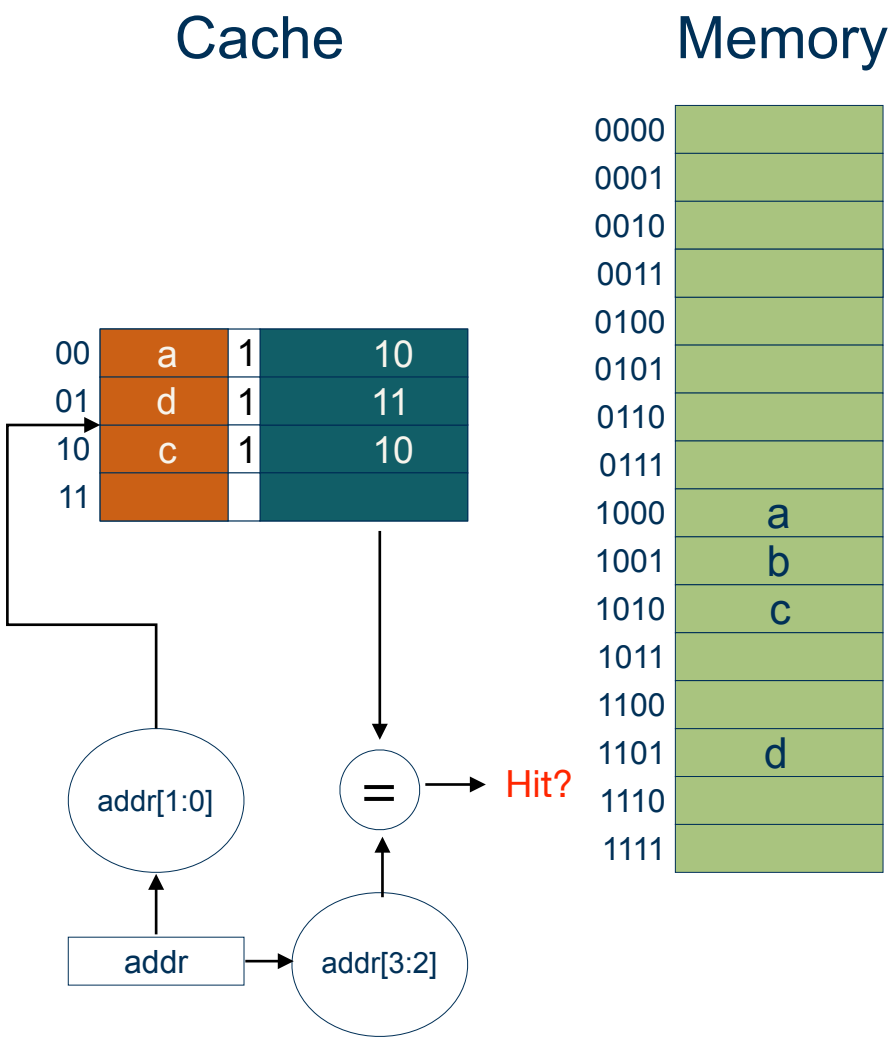

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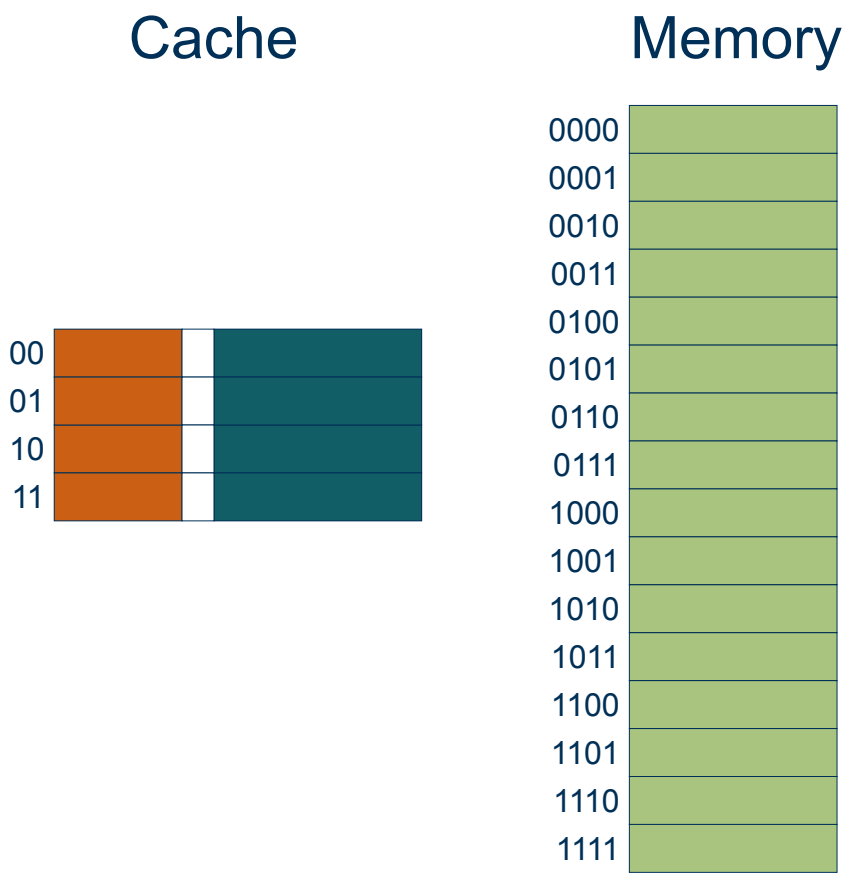
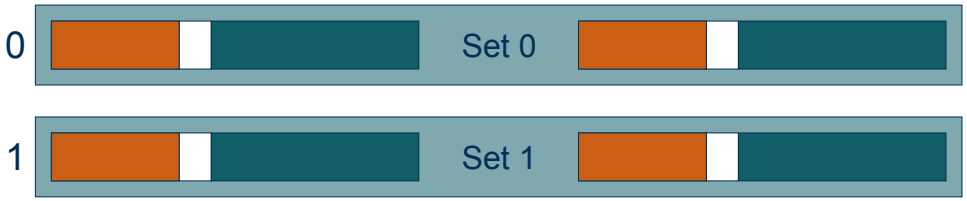
- Why? Each memory location is mapped to only one cache location

Sets



- Each cacheable memory location is mapped to **a set of cache locations**
- A set is one or more cache locations
- Set size is the number of locations in a set, also called **associativity**

2 Way Set Associative



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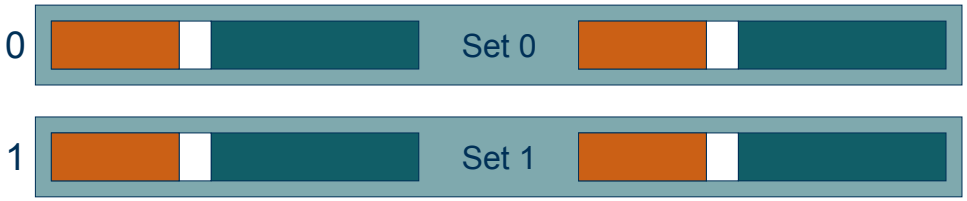

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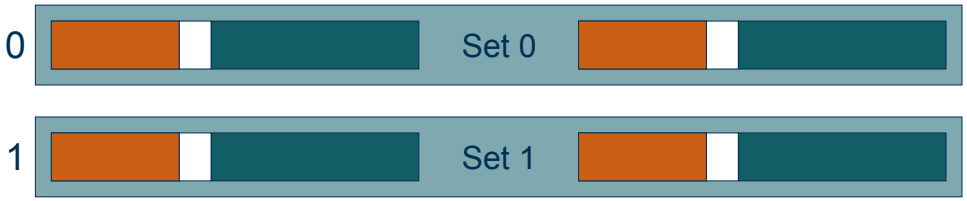

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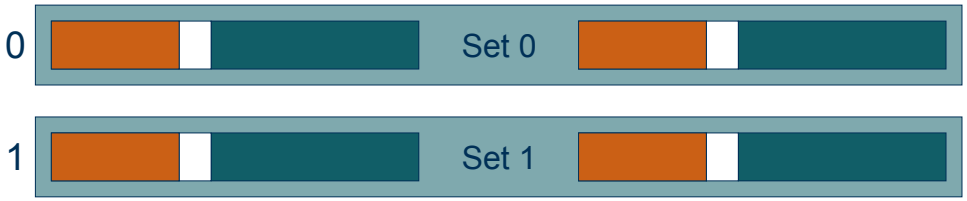

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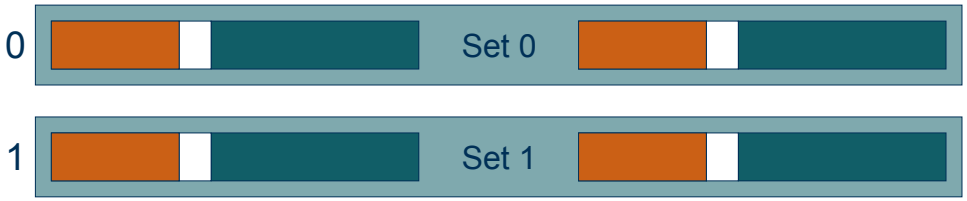

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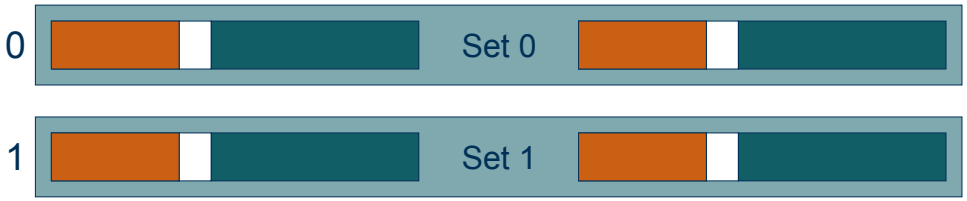

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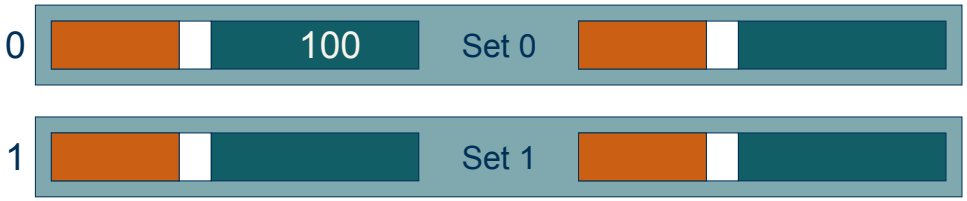

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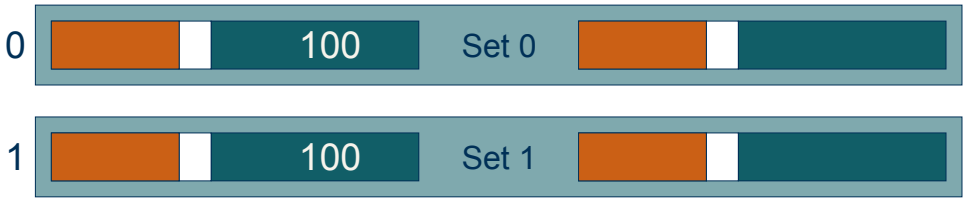

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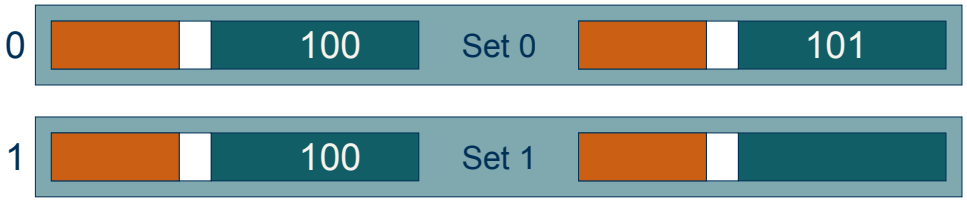

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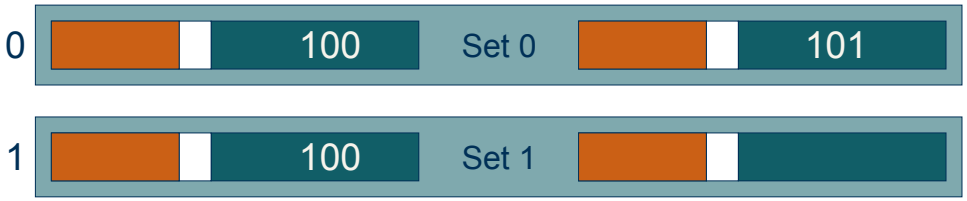

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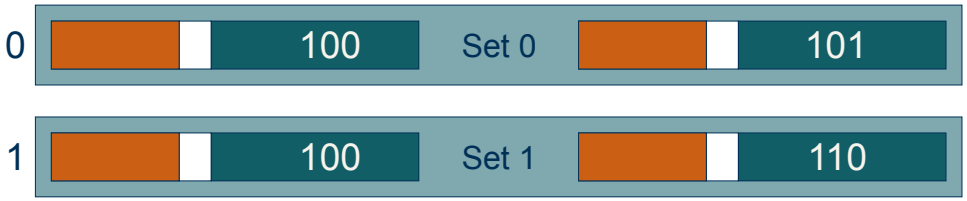

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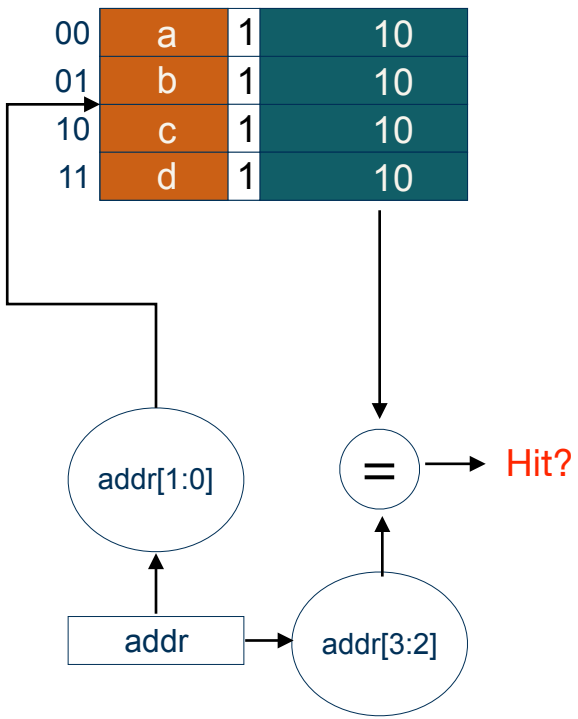

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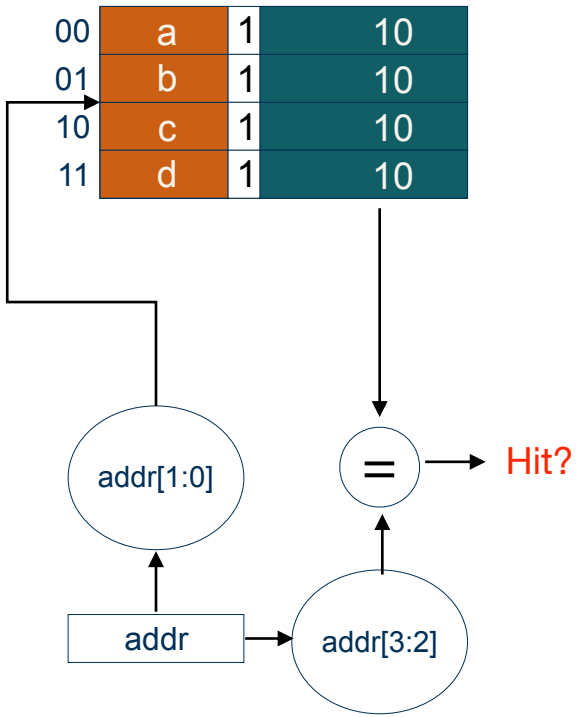

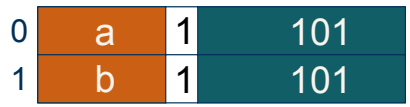

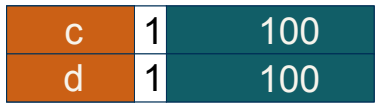

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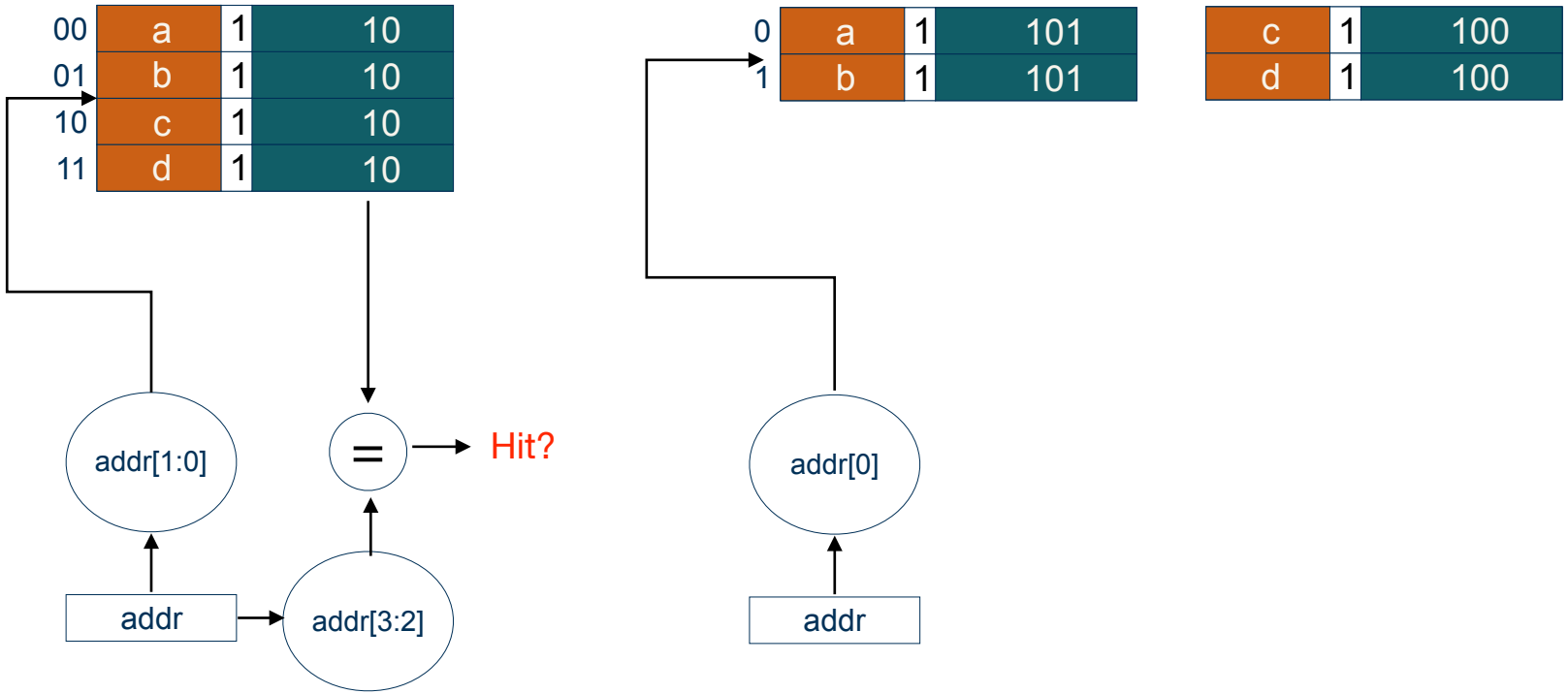

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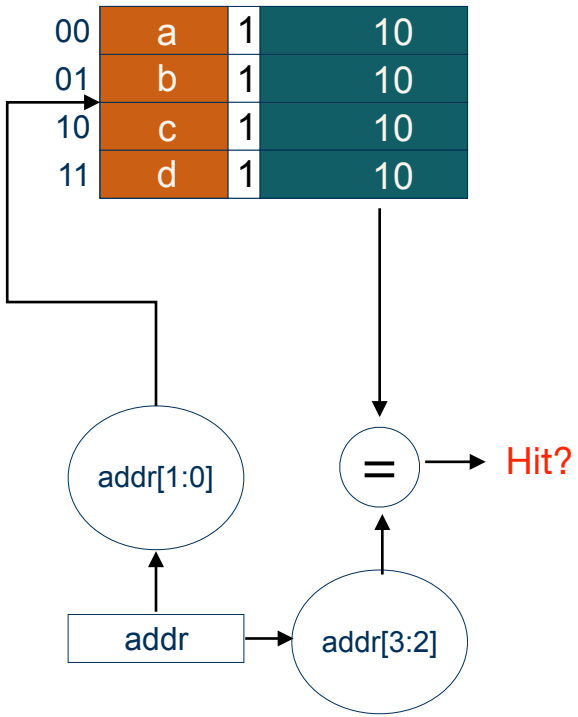

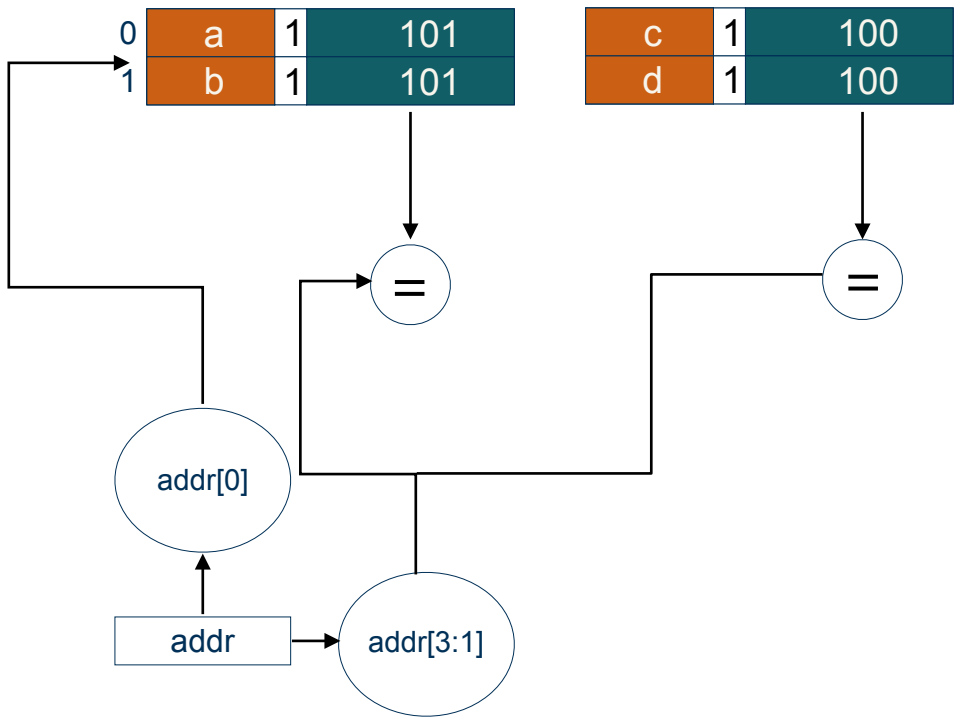

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