CSC 252: Computer Organization
Spring 2020: Lecture 18

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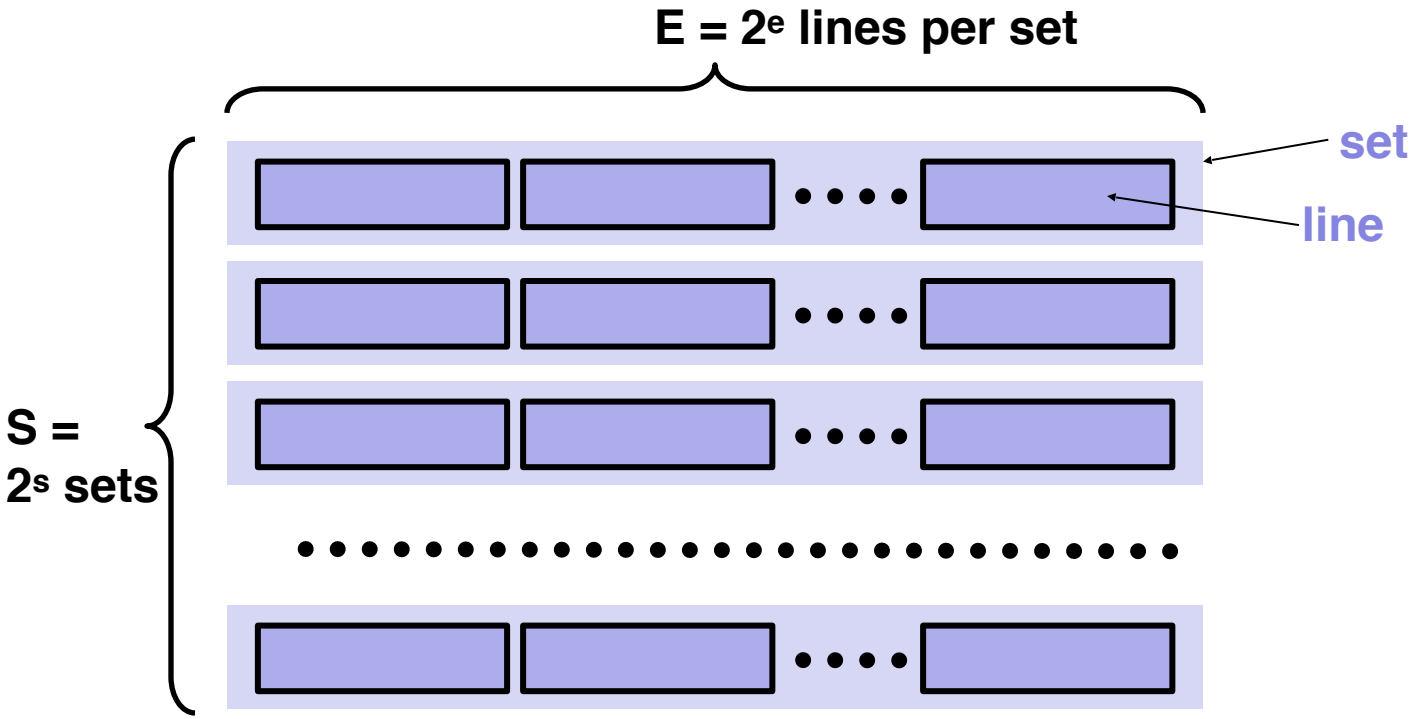
Announcements

- **Cache problem set: https://www.cs.rochester.edu/courses/252/spring2020/handouts.html**
- **Not to be turned in**
- **Assignment 4 soon to be released later today**

General Cache Organization (S, E, B)



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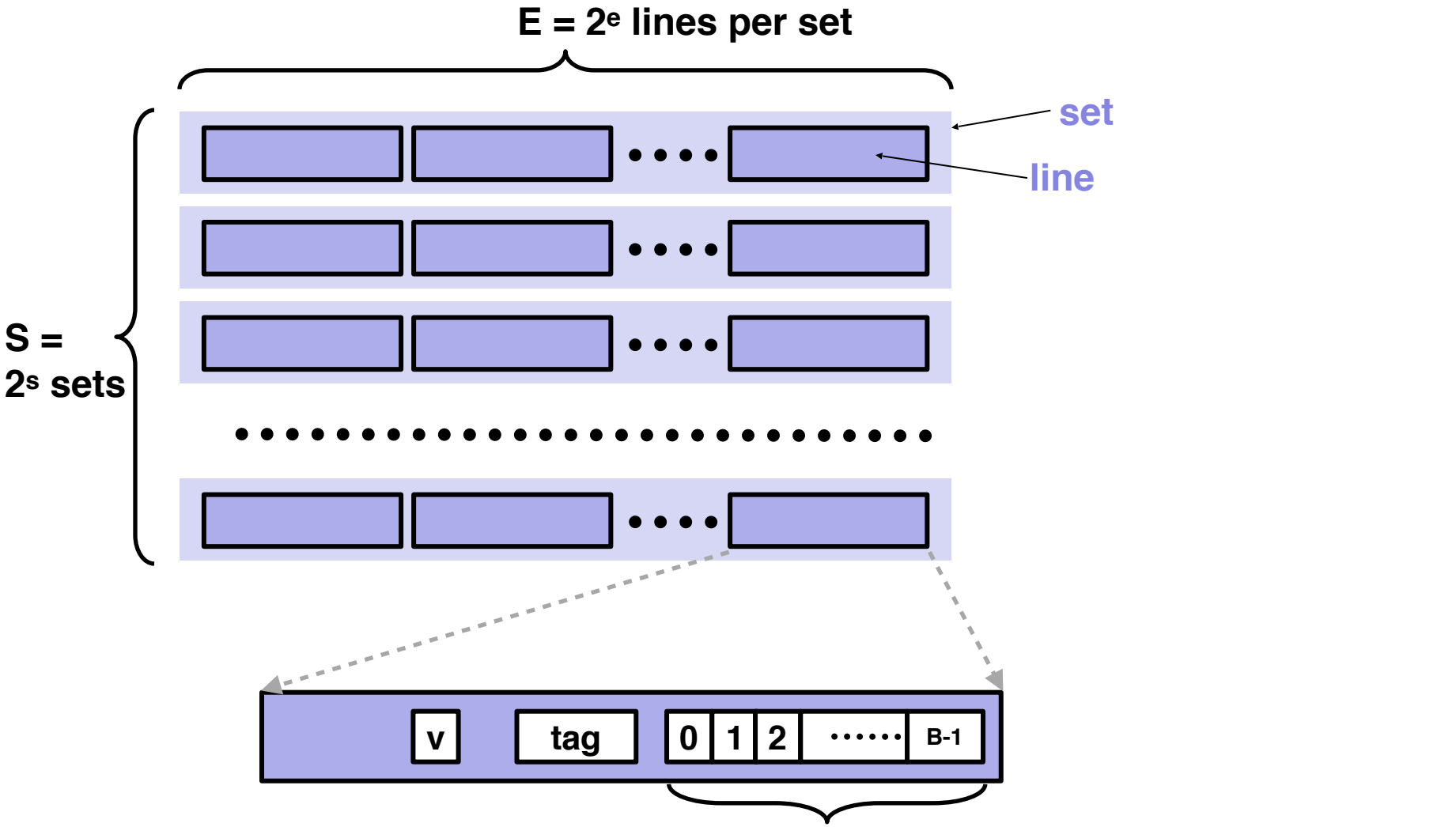

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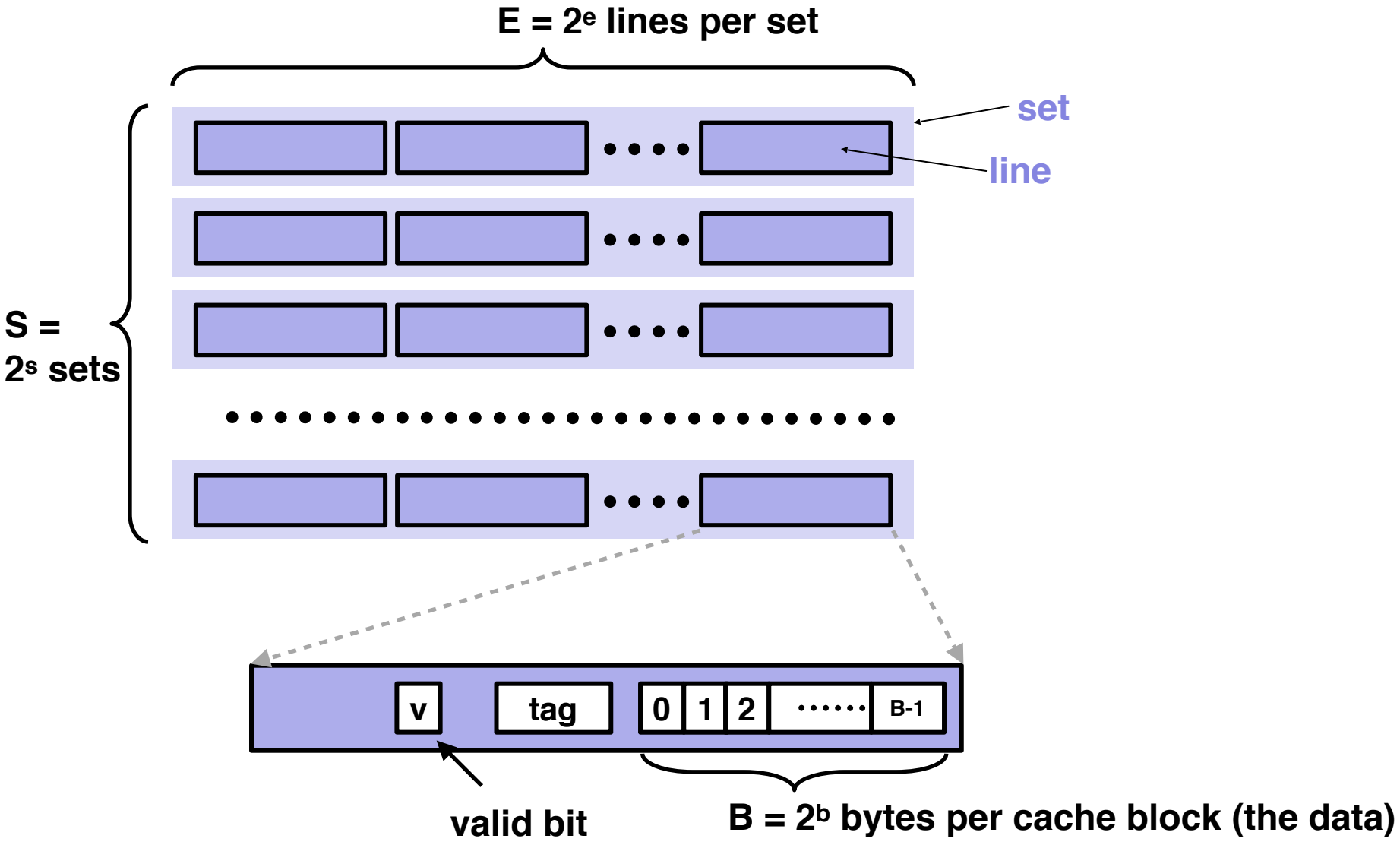

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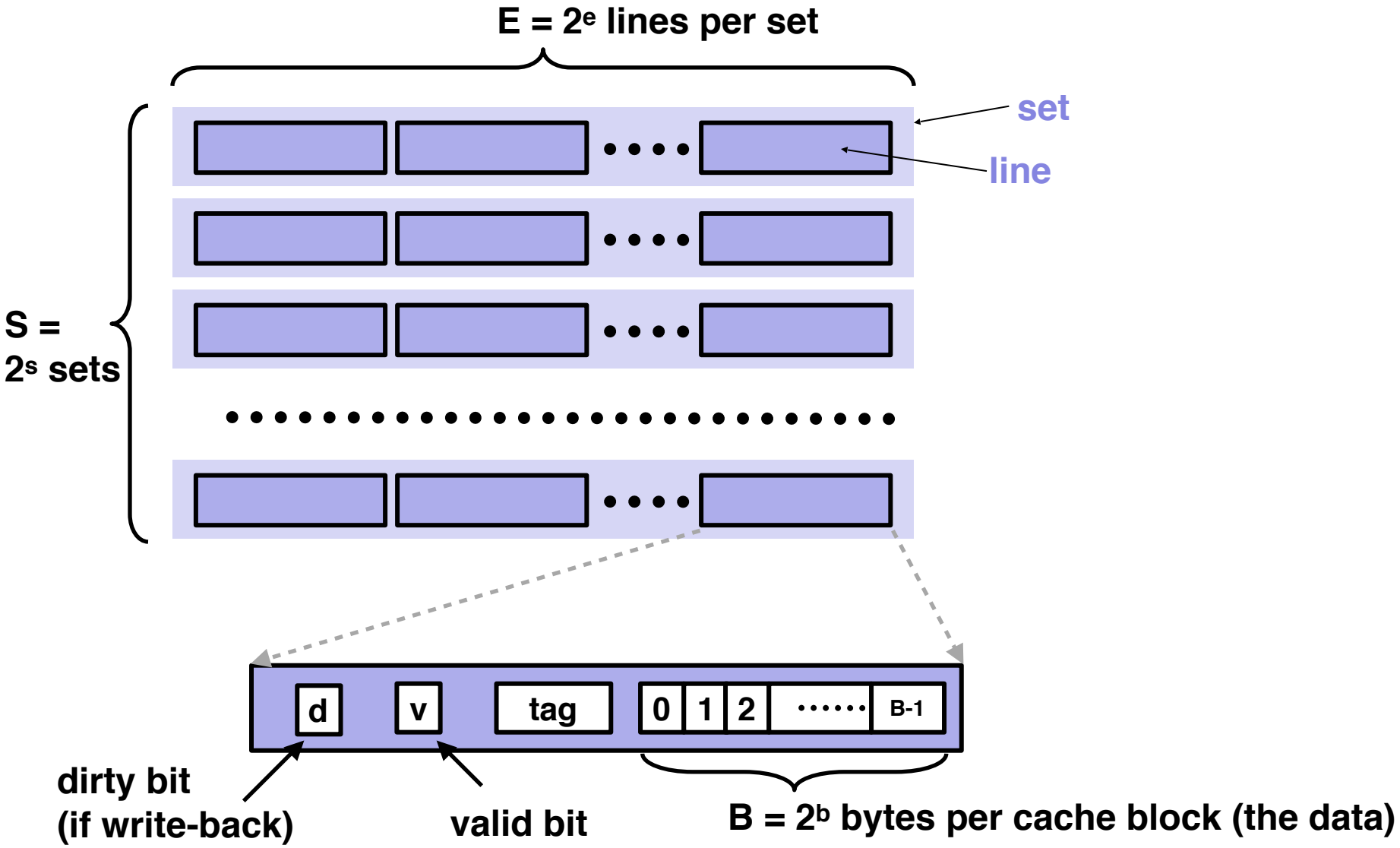

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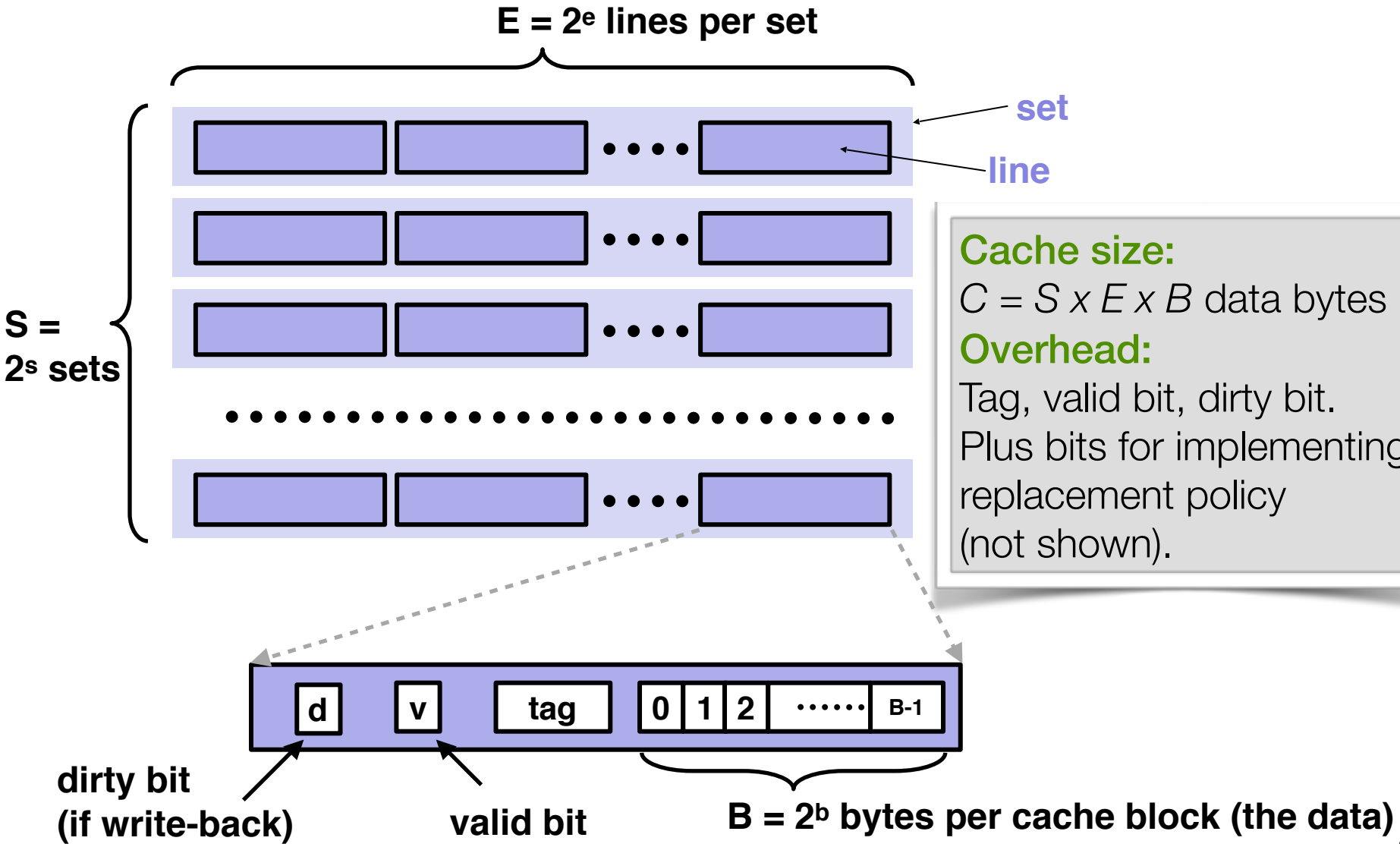
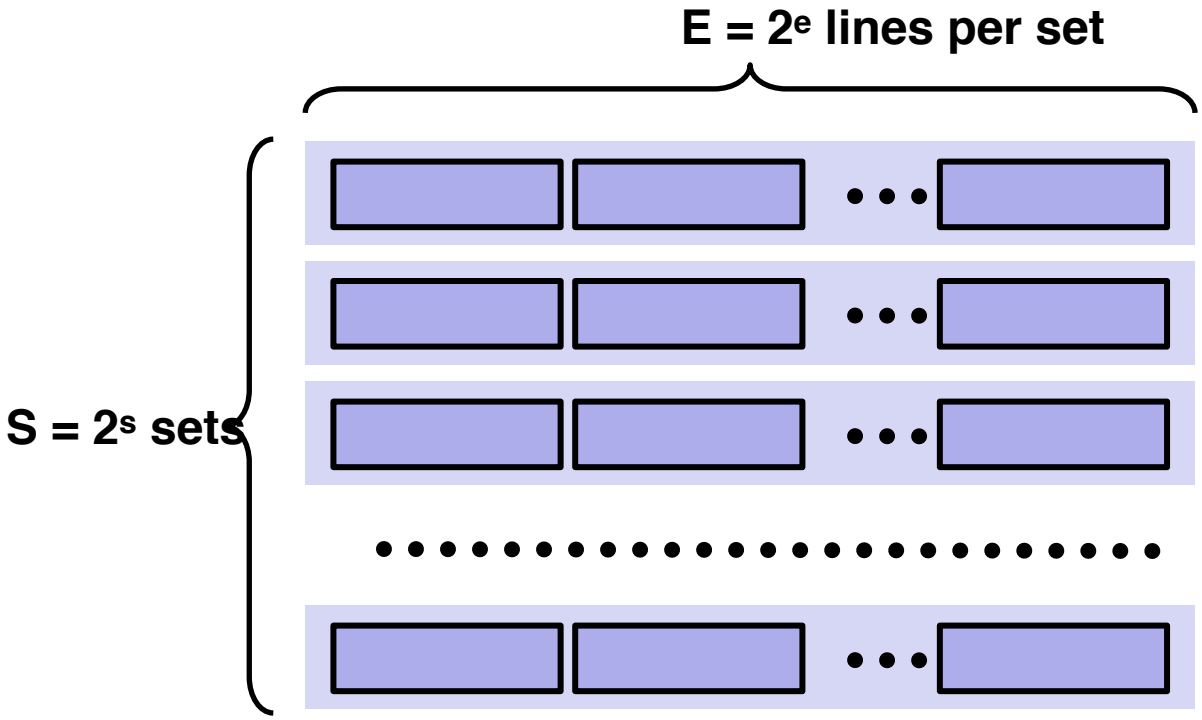
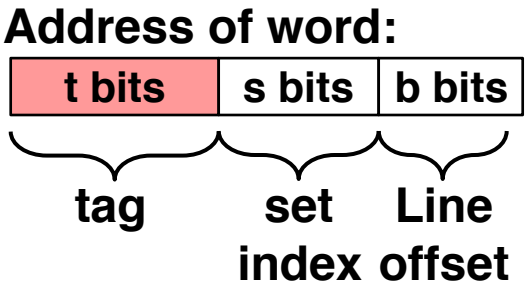


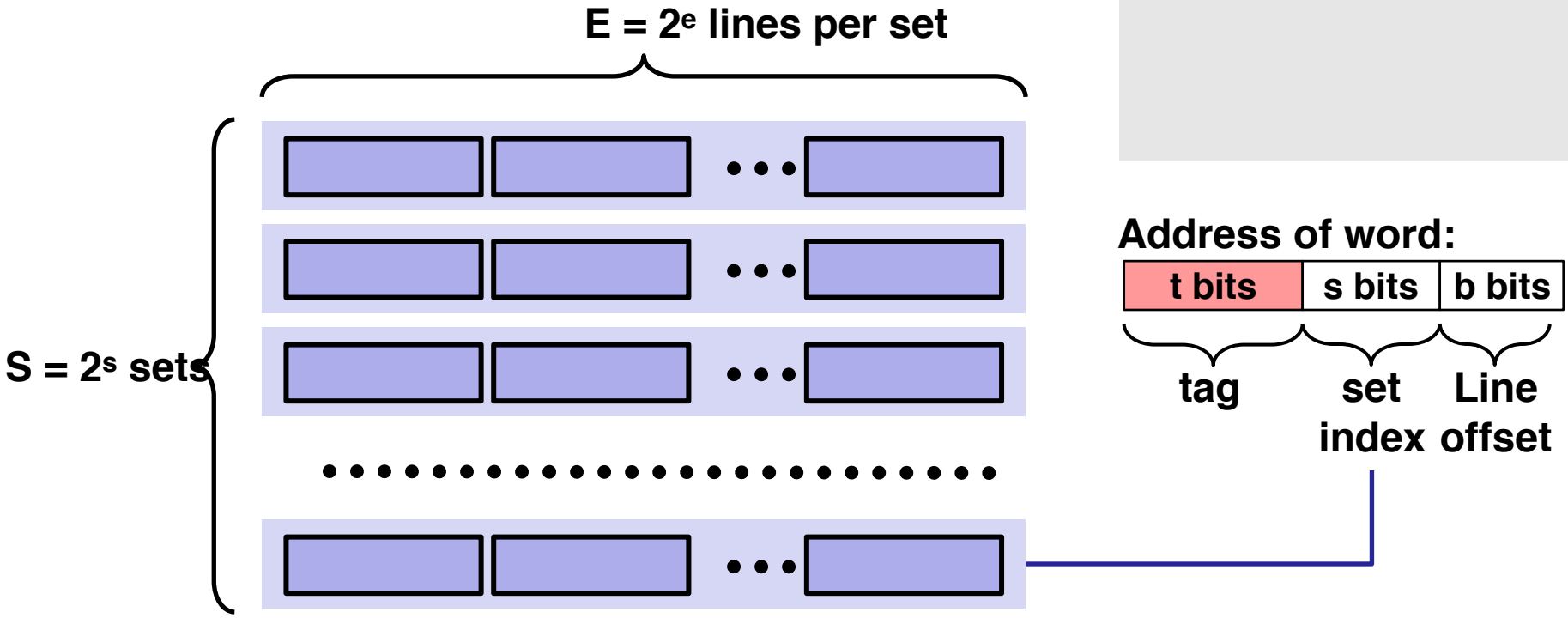
Cache Access





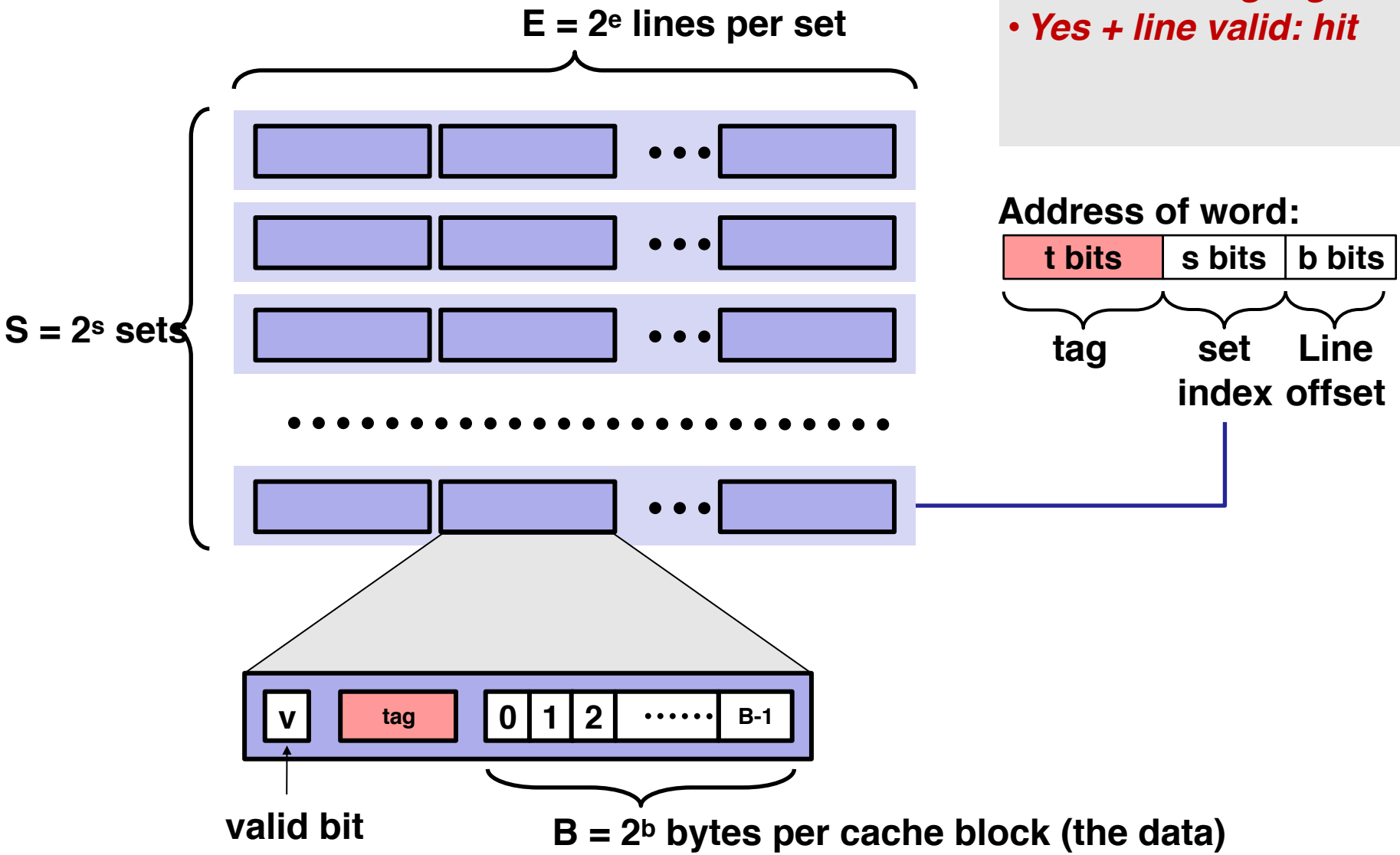
Cache Access

- *Locate set*



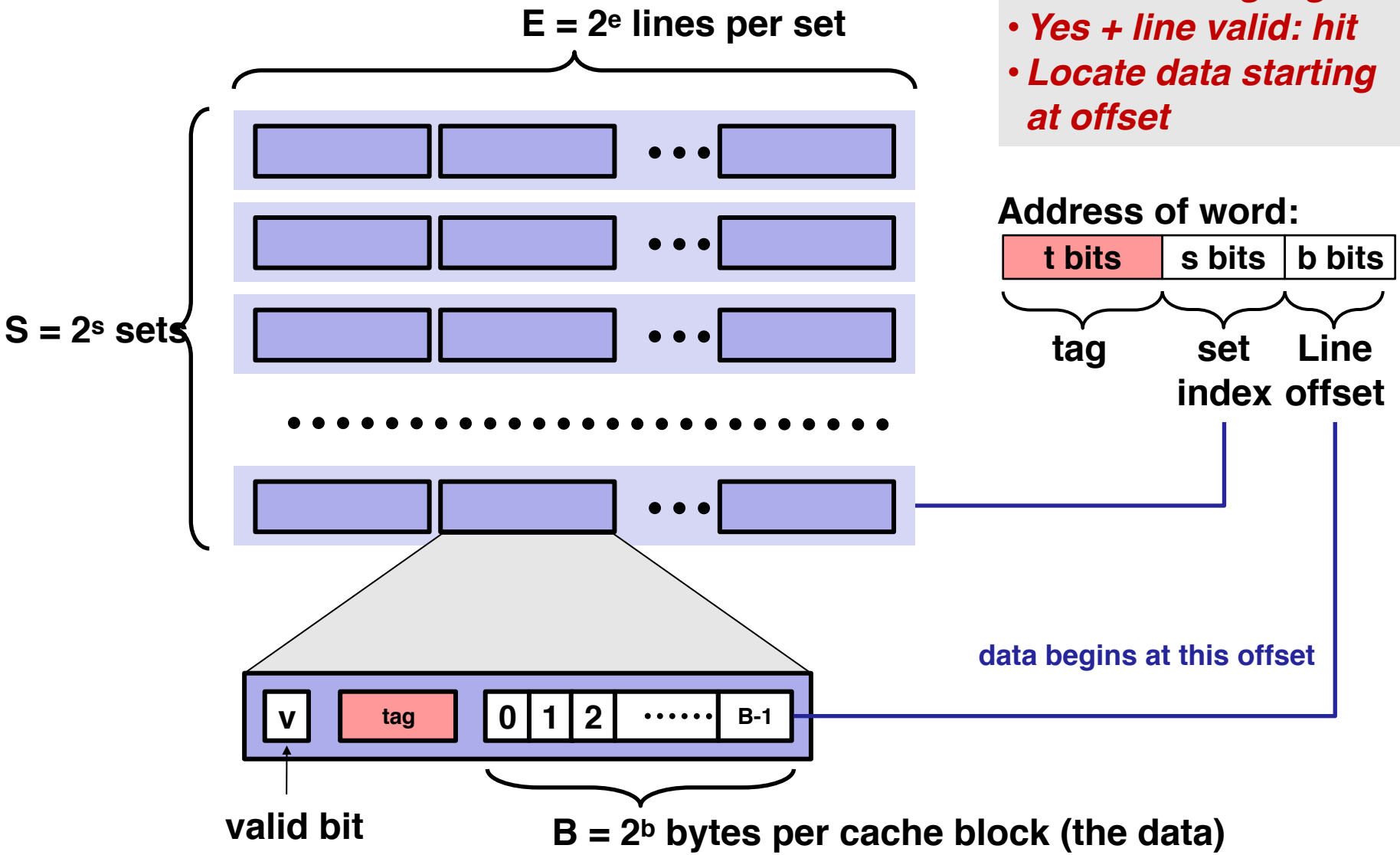
Cache Access

- *Locate set*
- *Check if any line in set has matching tag*
- *Yes + line valid: hit*



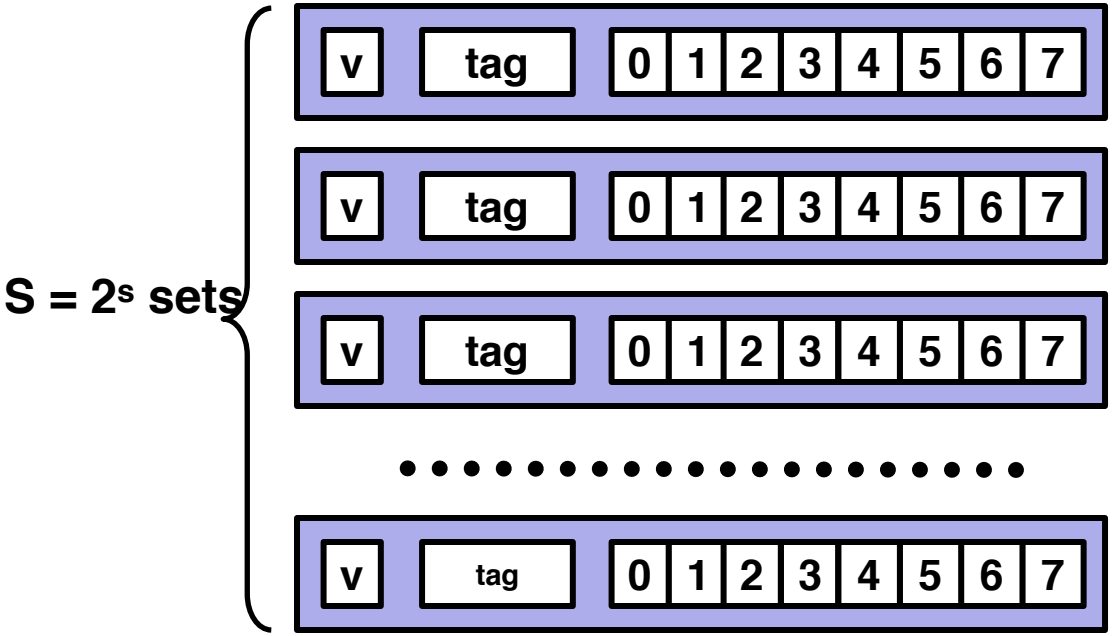
Cache Access

- *Locate set*
- *Check if any line in set has matching tag*
- *Yes + line valid: hit*
- *Locate data starting at offset*



Example: Direct Mapped Cache

Direct mapped: One line per set
Assume: cache block size 8 bytes



Address of `char`:

t bits	0…01	100

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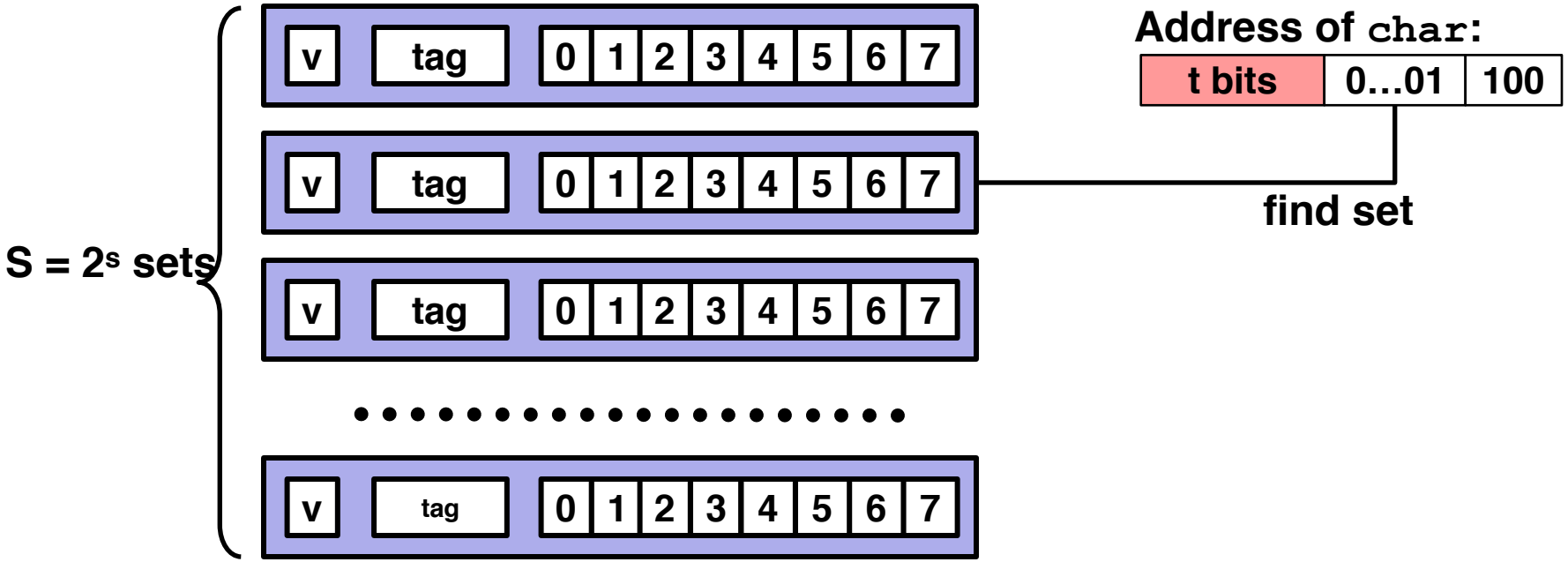

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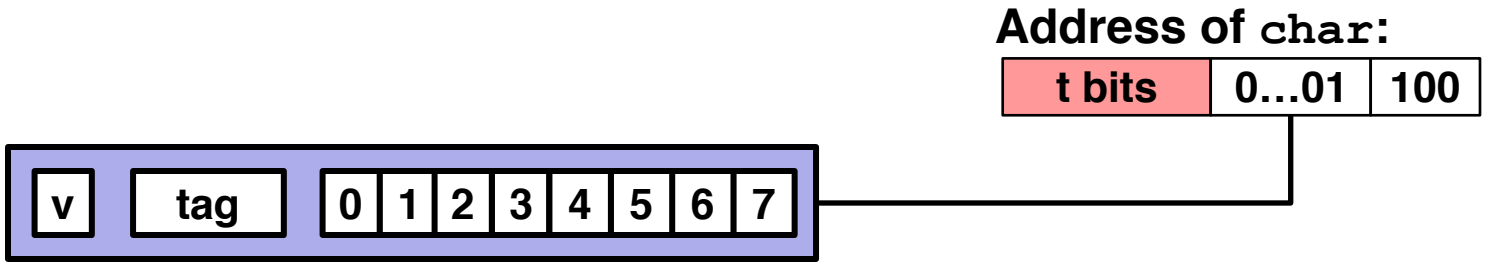

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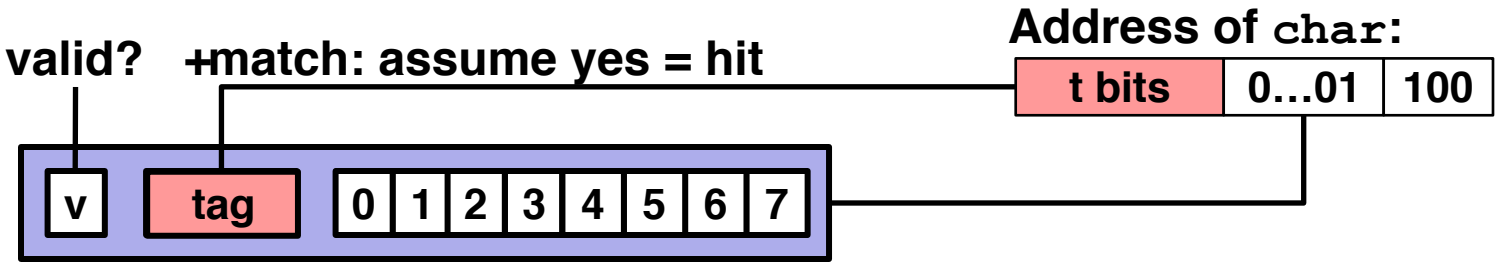

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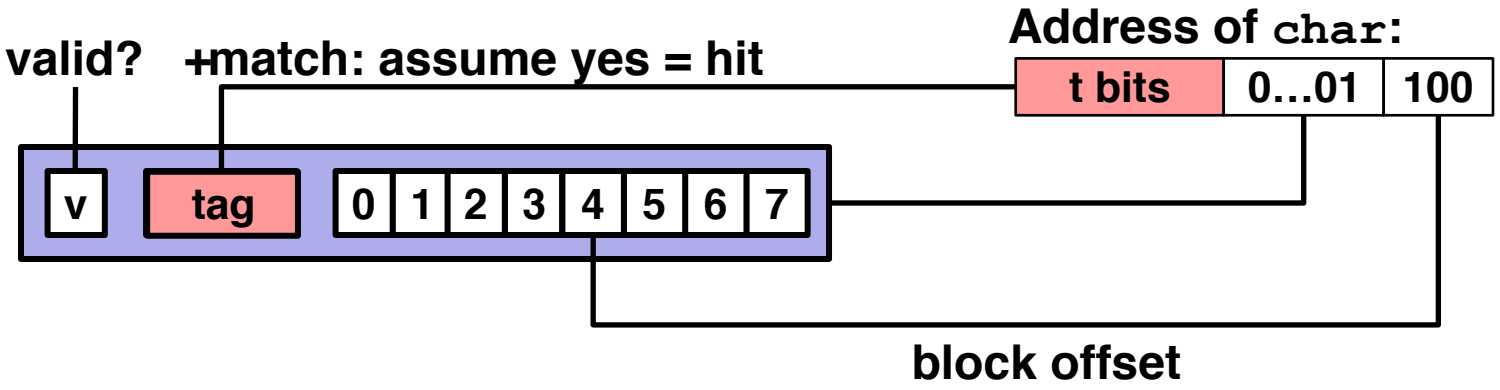

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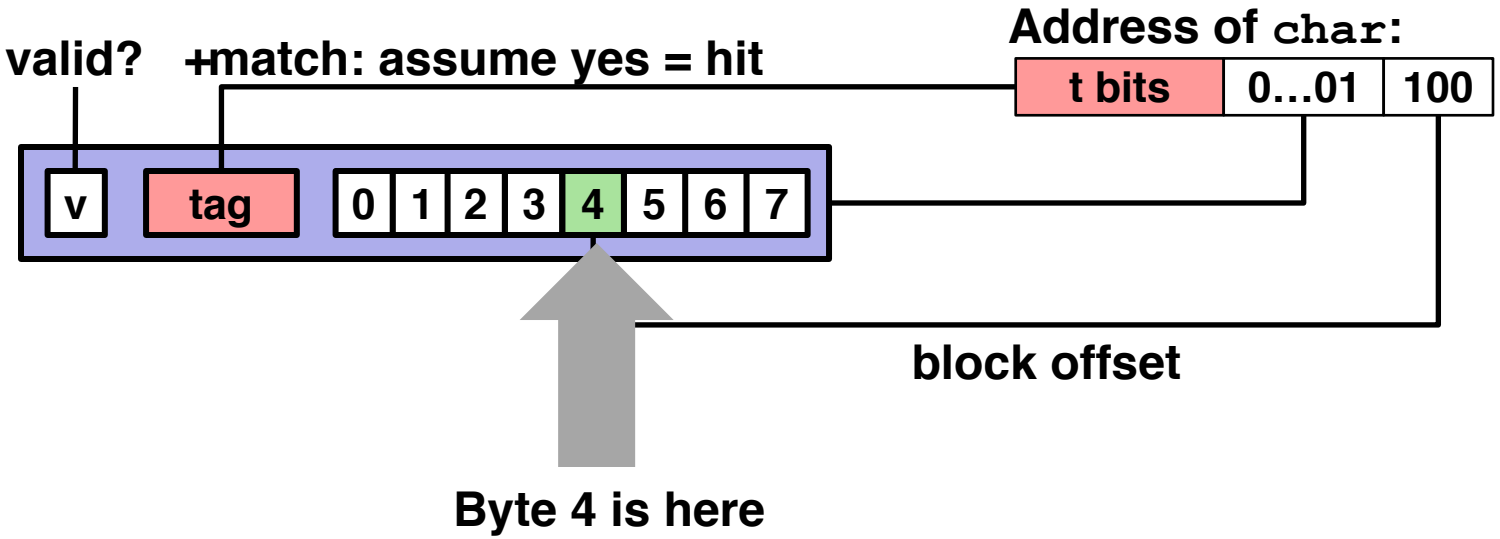

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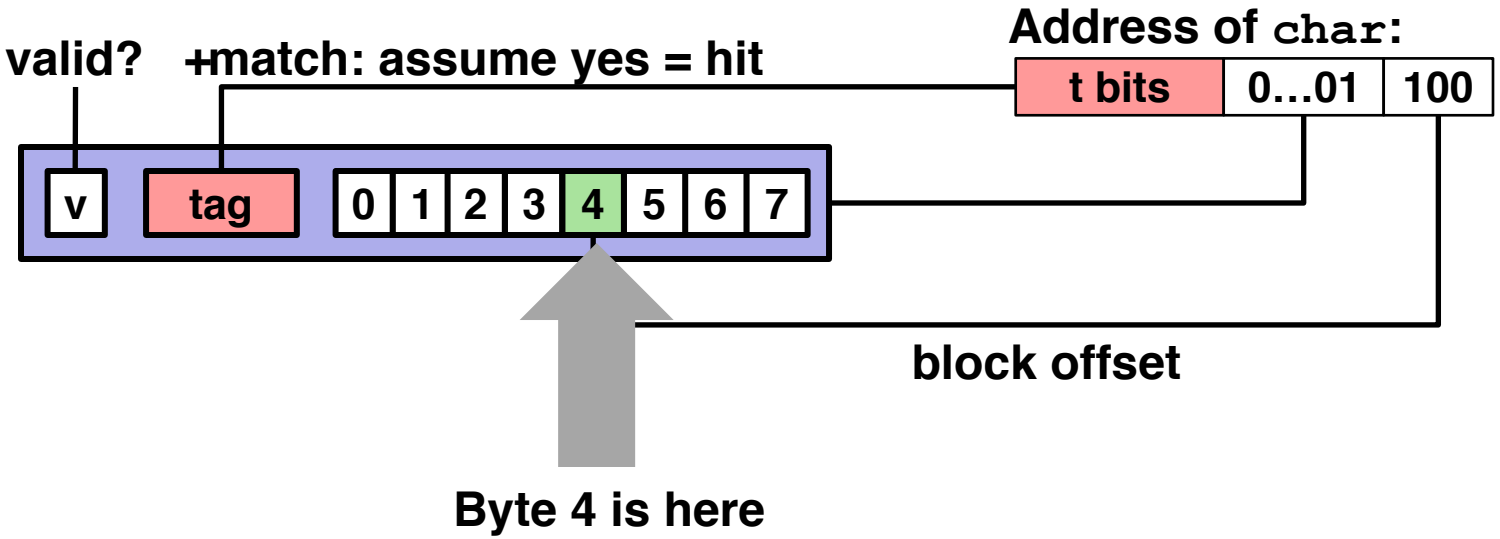

If tag doesn't match: old line is evicted and replaced

Direct-Mapped Cache Simulation

t=1	s=2	b=1
x	xx	x

4-bit address space, i.e., Memory = 16 bytes
B=2 bytes/line, S=4 sets, E=1 line/set

Address trace (reads, one byte per read):

0 **[0$\underline{00}$0$_2$],**
1 **[0$\underline{00}$1$_2$],**
7 **[0$\underline{11}$1$_2$],**
8 **[1$\underline{00}$0$_2$],**
0 **[0$\underline{00}$0$_2$]**

	v	Tag	Line
Set 0	0	?	?
Set 1			
Set 2			
Set 3			

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8	**[1$\underline{00}$0$_2$],**	
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8	**[1$\underline{00}$0$_2$],**	
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	v	Tag	Line
Set 0	1	0	M[0-1]
Set 1			
Set 2			
Set 3			

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	v	Tag	Line
Set 0	1	0	M[0-1]
Set 1			
Set 2			
Set 3			

← The two bytes at memory address 0 and 1

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B=2 bytes/line, S=4 sets, E=1 line/set

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0	**[0$\underline{00}$0$_2$],**	miss
1	**[0$\underline{00}$1$_2$],**	hit
7	**[0$\underline{11}$1$_2$],**	
8	**[1$\underline{00}$0$_2$],**	
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	v	Tag	Line	
Set 0	1	0	M[0-1]	← The two bytes at memory address 0 and 1
Set 1				
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Set 3				

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Set 1			
Set 2			
Set 3			

← The two bytes at memory address 0 and 1

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8	**[1$\underline{00}$0$_2$],**	
0	**[0$\underline{00}$0$_2$]**	

	v	Tag	Line	
Set 0	1	0	M[0-1]	← The two bytes at memory address 0 and 1
Set 1				
Set 2				
Set 3	1	0	M[6-7]	

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x	xx	x

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1	**[0$\underline{00}$1$_2$],**	hit
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8	**[1$\underline{00}$0$_2$],**	
0	**[0$\underline{00}$0$_2$]**	

	v	Tag	Line	
Set 0	1	0	M[0-1]	← The two bytes at memory address 0 and 1
Set 1				
Set 2				
Set 3	1	0	M[6-7]	← The two bytes at memory address 6 and 7

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	v	Tag	Line	
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Set 2				
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x	xx	x

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Address trace (reads, one byte per read):

0	**[0$\underline{000}$0$_2$],**	miss
1	**[0$\underline{000}$1$_2$],**	hit
7	**[0$\underline{111}$1$_2$],**	miss
8	**[1$\underline{000}$0$_2$],**	miss
0	**[0$\underline{000}$0$_2$]**	

	v	Tag	Line	
Set 0	1	1	M[8-9]	← The two bytes at memory address 8 and 9
Set 1				
Set 2				
Set 3	1	0	M[6-7]	← The two bytes at memory address 6 and 7

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0	**[0$\underline{00}$0$_2$],**	miss
1	**[0$\underline{00}$1$_2$],**	hit
7	**[0$\underline{11}$1$_2$],**	miss
8	**[1$\underline{00}$0$_2$],**	miss
0	**[0$\underline{00}$0$_2$]**	miss

	v	Tag	Line	
Set 0	1	1	M[8-9]	← The two bytes at memory address 8 and 9
Set 1				
Set 2				
Set 3	1	0	M[6-7]	← The two bytes at memory address 6 and 7

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7	**[0$\underline{11}$1$_2$],**	miss
8	**[1$\underline{00}$0$_2$],**	miss
0	**[0$\underline{00}$0$_2$]**	miss

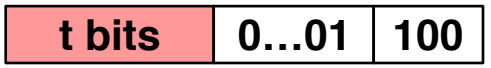
	v	Tag	Line	
Set 0	1	0	M[0-1]	← The two bytes at memory address 0 and 1
Set 1				
Set 2				
Set 3	1	0	M[6-7]	← The two bytes at memory address 6 and 7

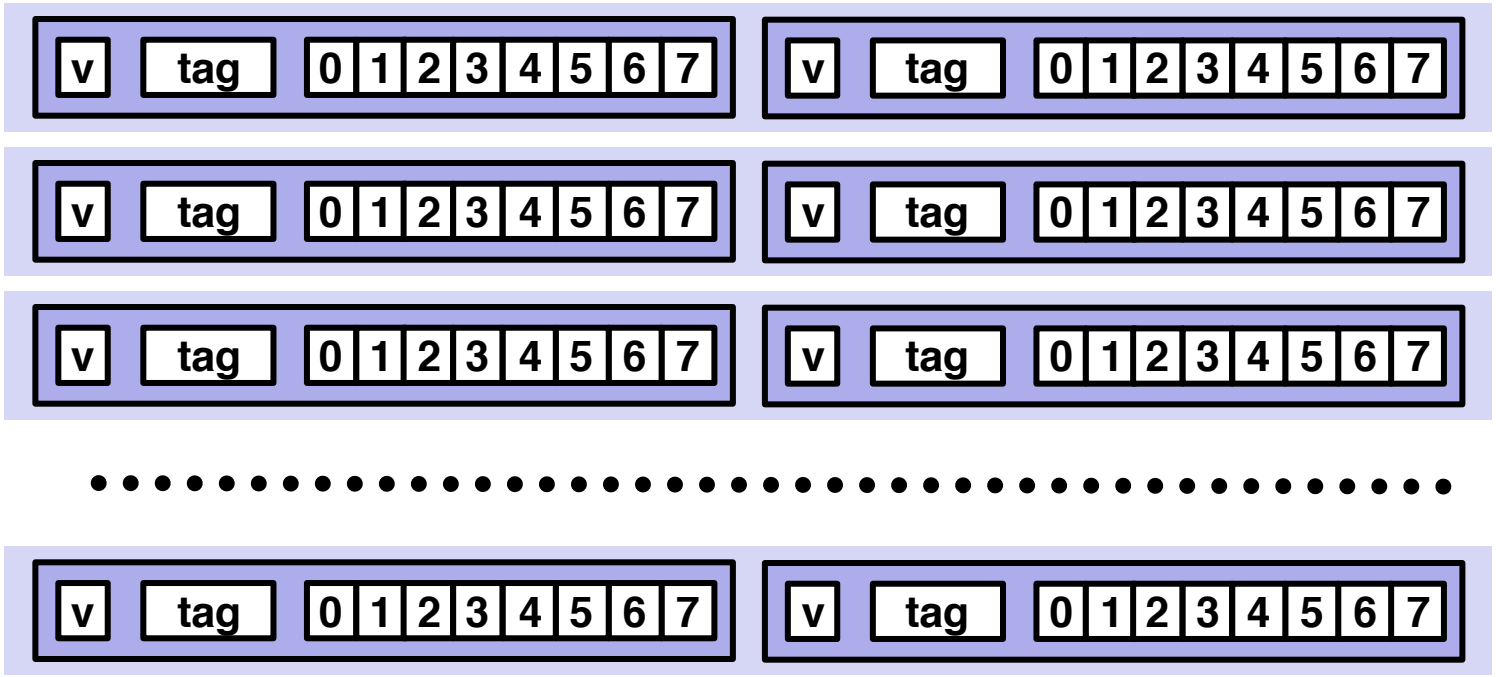
E-way Set Associative Cache (Here: E = 2)

E = 2: Two lines per set

Assume: cache block size 8 bytes

Address of `short int`:





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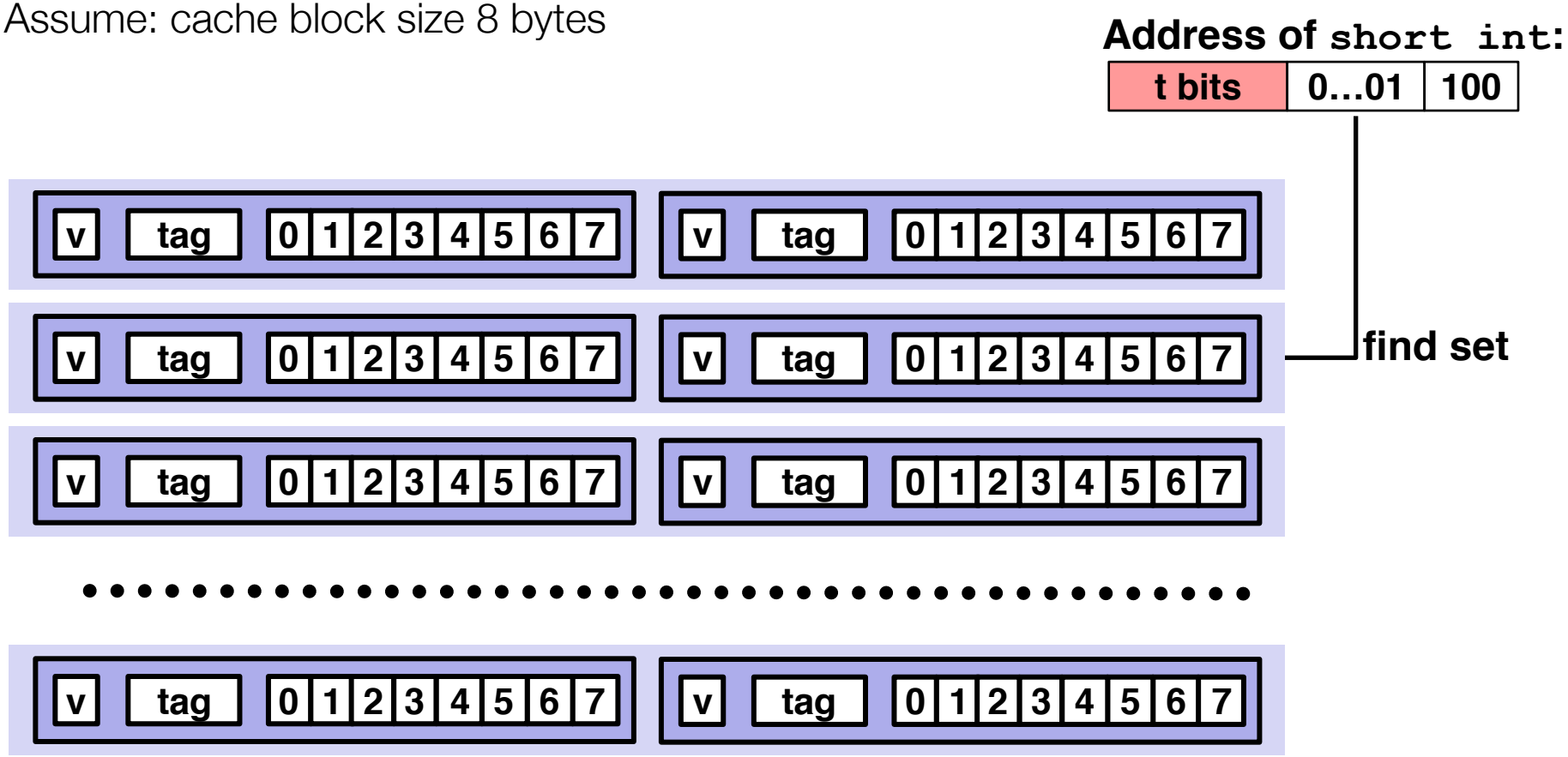

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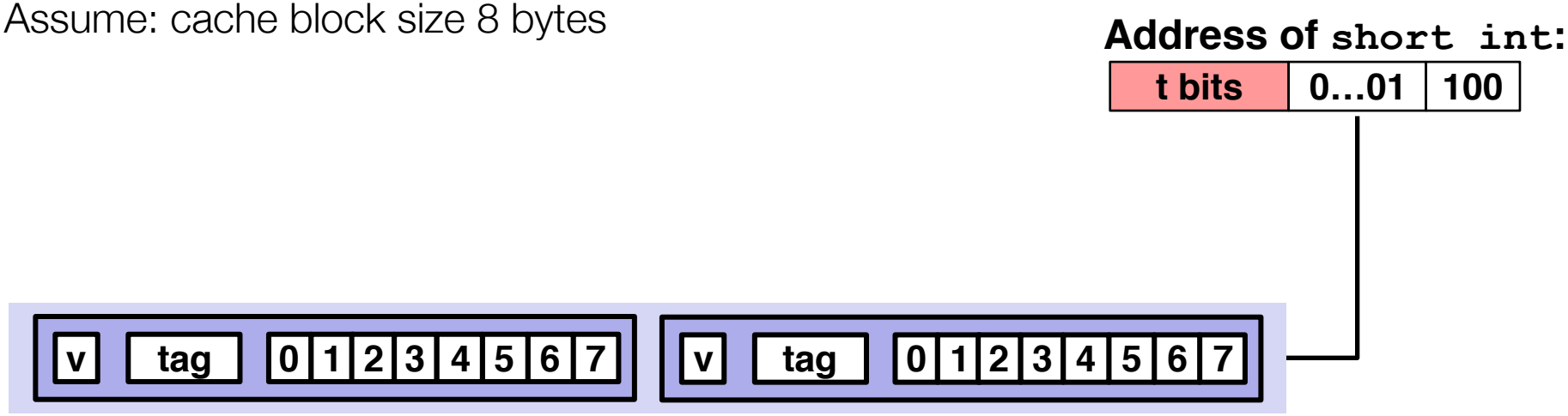

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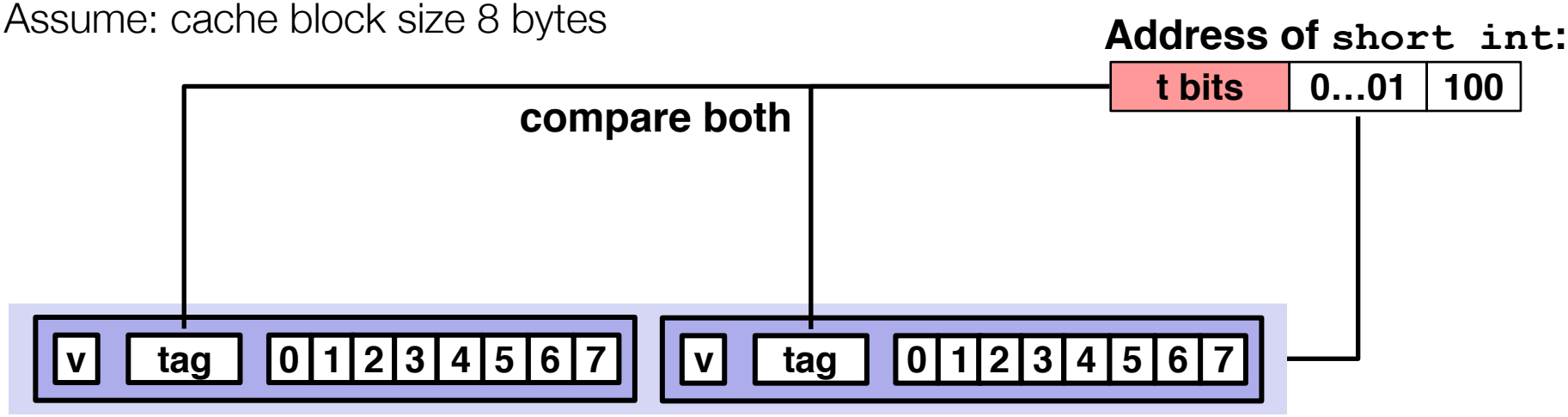

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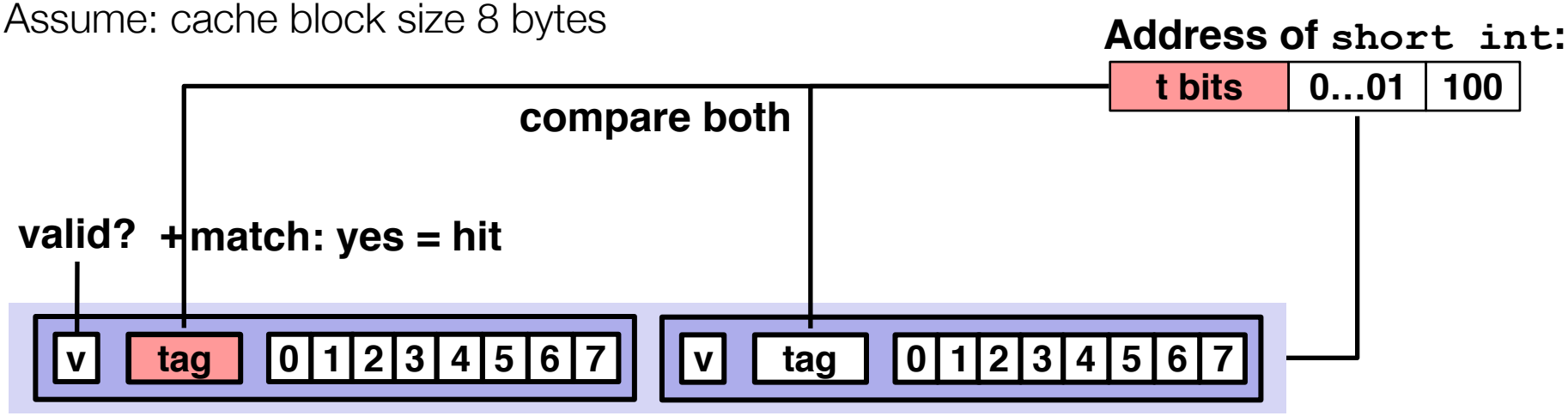

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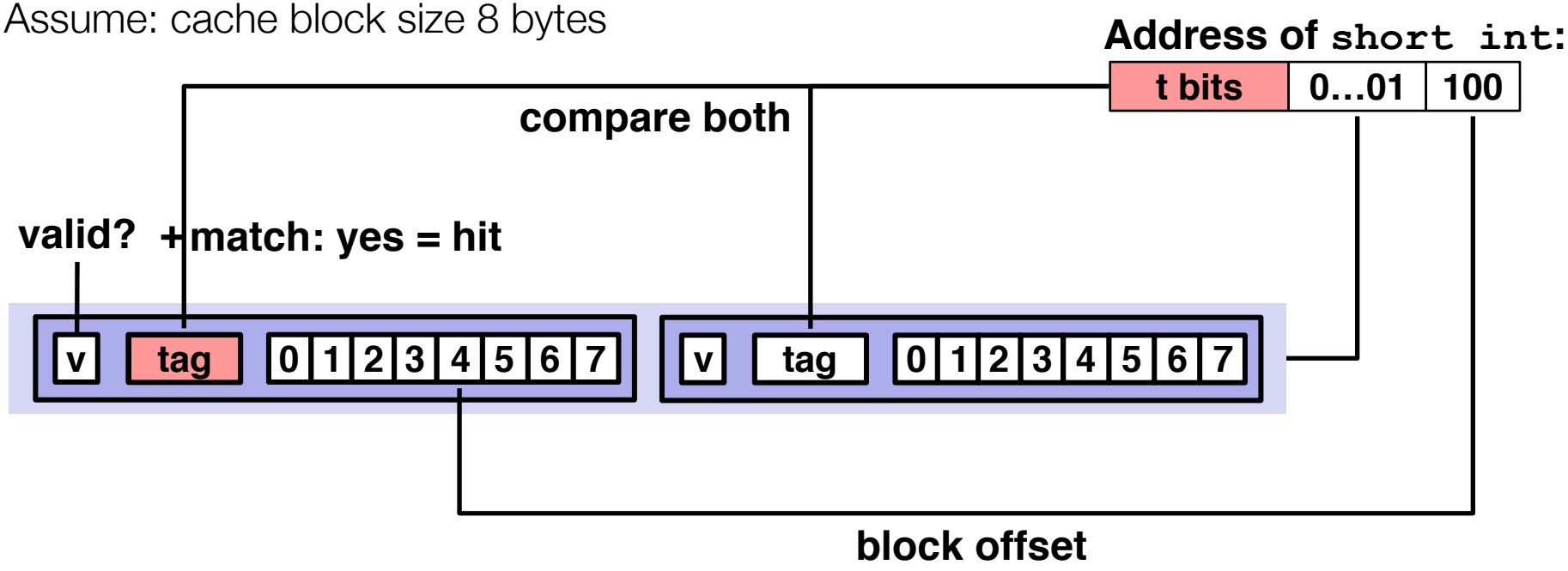

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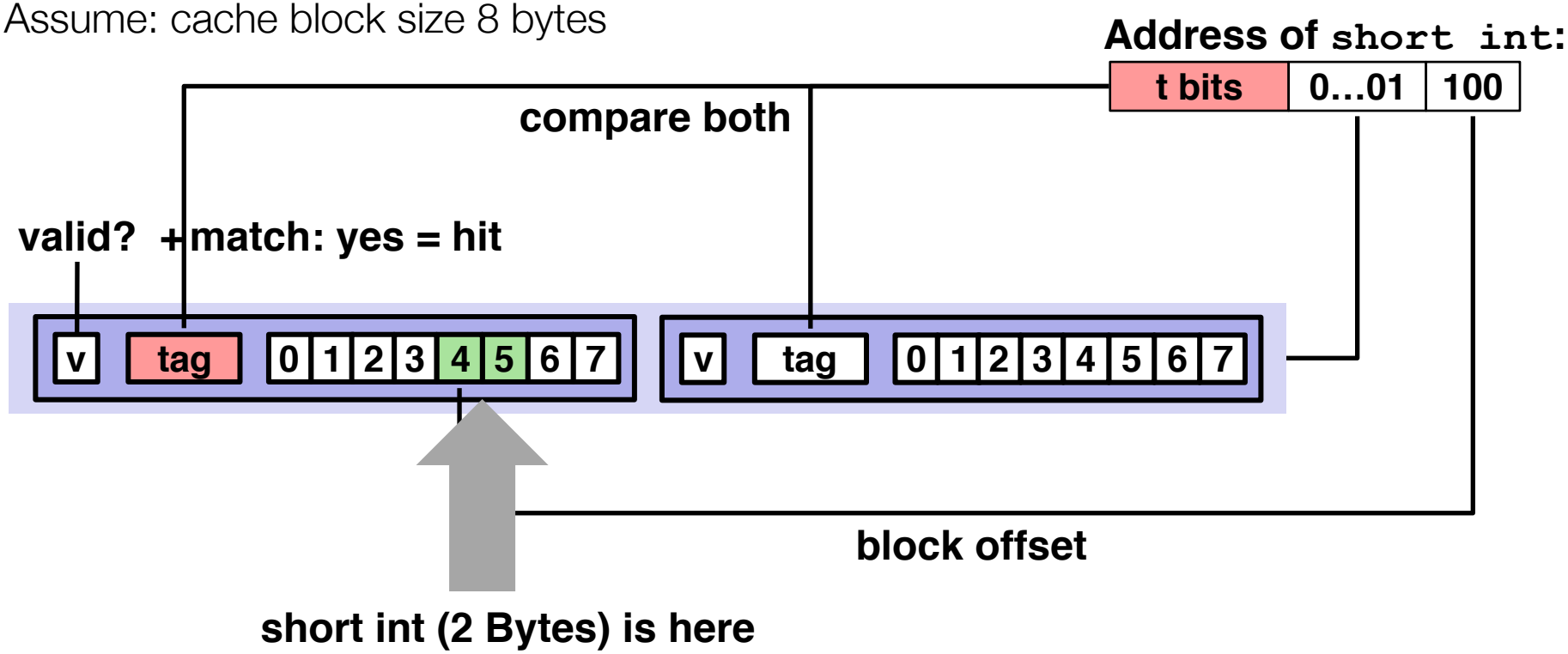

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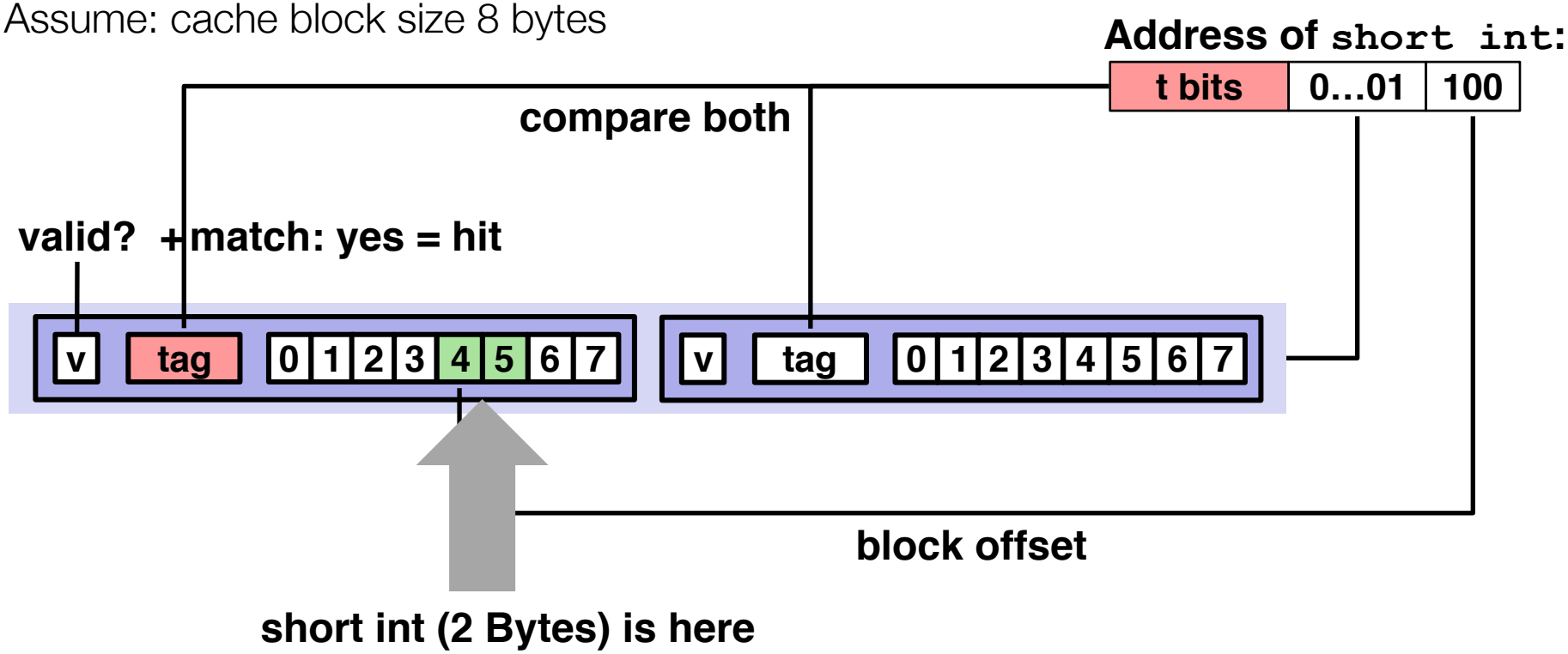

No match:

- **One line in set is selected for eviction and replacement**
- **Replacement policies: random, least recently used (LRU),**

2-Way Set Associative Cache Simulation

t=2	s=1	b=1
xx	x	x

4-bit address space, i.e., Memory = 16 bytes
S=2 sets, E=2 blocks/set

Address trace (reads, one byte per read):

0 **[0000$_2$],**
1 **[0001$_2$],**
7 **[0111$_2$],**
8 **[1000$_2$],**
0 **[0000$_2$]**

	v	Tag	Block
Set 0	0	?	?
	0		
Set 1	0		
	0		

2-Way Set Associative Cache Simulation

t=2	s=1	b=1
xx	x	x

4-bit address space, i.e., Memory = 16 bytes
S=2 sets, E=2 blocks/set

Address trace (reads, one byte per read):

0	**[00$\underline{0}$0$_2$],**	miss
1	**[00$\underline{0}$1$_2$],**	
7	**[01$\underline{1}$1$_2$],**	
8	**[10$\underline{0}$0$_2$],**	
0	**[00$\underline{0}$0$_2$]**	

	v	Tag	Block
Set 0	0	?	?
	0		
Set 1	0		
	0		

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1	**[00$\underline{0}$1$_2$],**	
7	**[01$\underline{1}$1$_2$],**	
8	**[10$\underline{0}$0$_2$],**	
0	**[00$\underline{0}$0$_2$]**	

	v	Tag	Block
Set 0	1	00	M[0-1]
	0		
Set 1	0		
	0		

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t=2	s=1	b=1
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4-bit address space, i.e., Memory = 16 bytes
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1	**[00$\underline{0}$1$_2$],**	hit
7	**[01$\underline{1}$1$_2$],**	
8	**[10$\underline{0}$0$_2$],**	
0	**[00$\underline{0}$0$_2$]**	

	v	Tag	Block
Set 0	1	00	M[0-1]
	0		
Set 1	0		
	0		

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7	**[01$\underline{1}$1$_2$],**	miss
8	**[10$\underline{0}$0$_2$],**	
0	**[00$\underline{0}$0$_2$]**	

	v	Tag	Block
Set 0	1	00	M[0-1]
	0		
Set 1	0		
	0		

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8	**[10$\underline{0}$0$_2$],**	
0	**[00$\underline{0}$0$_2$]**	

	v	Tag	Block
Set 0	1	00	M[0-1]
	0		
Set 1	1	01	M[6-7]
	0		

2-Way Set Associative Cache Simulation

t=2	s=1	b=1
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	v	Tag	Block
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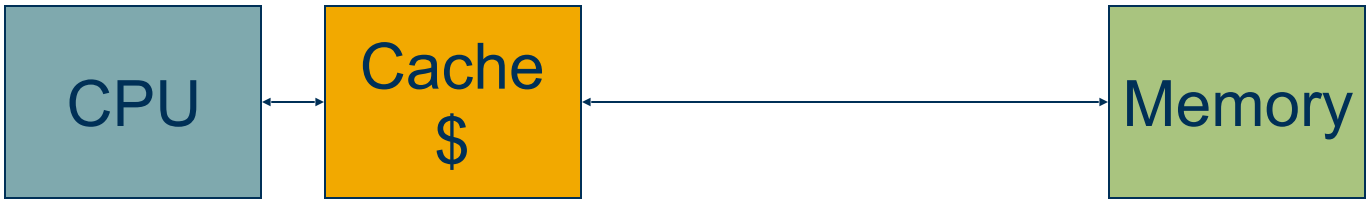

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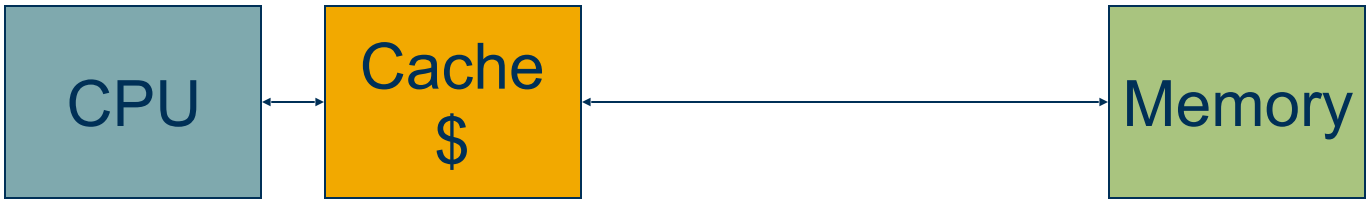

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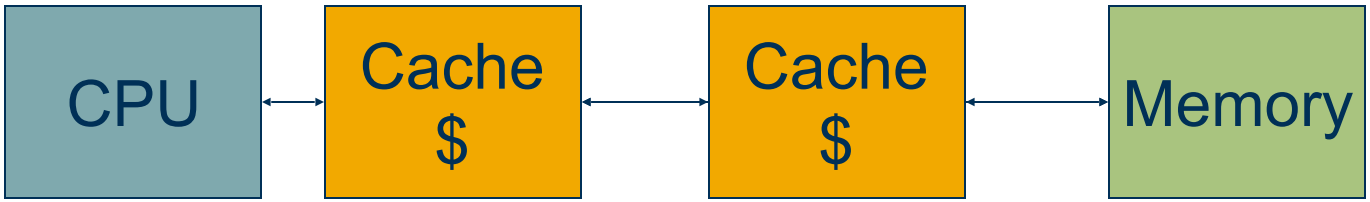

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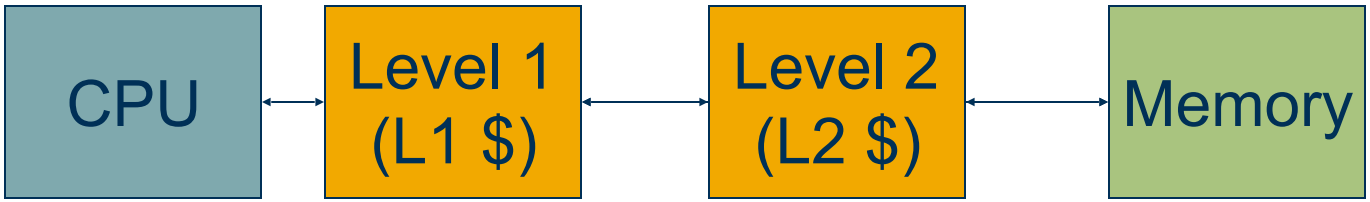

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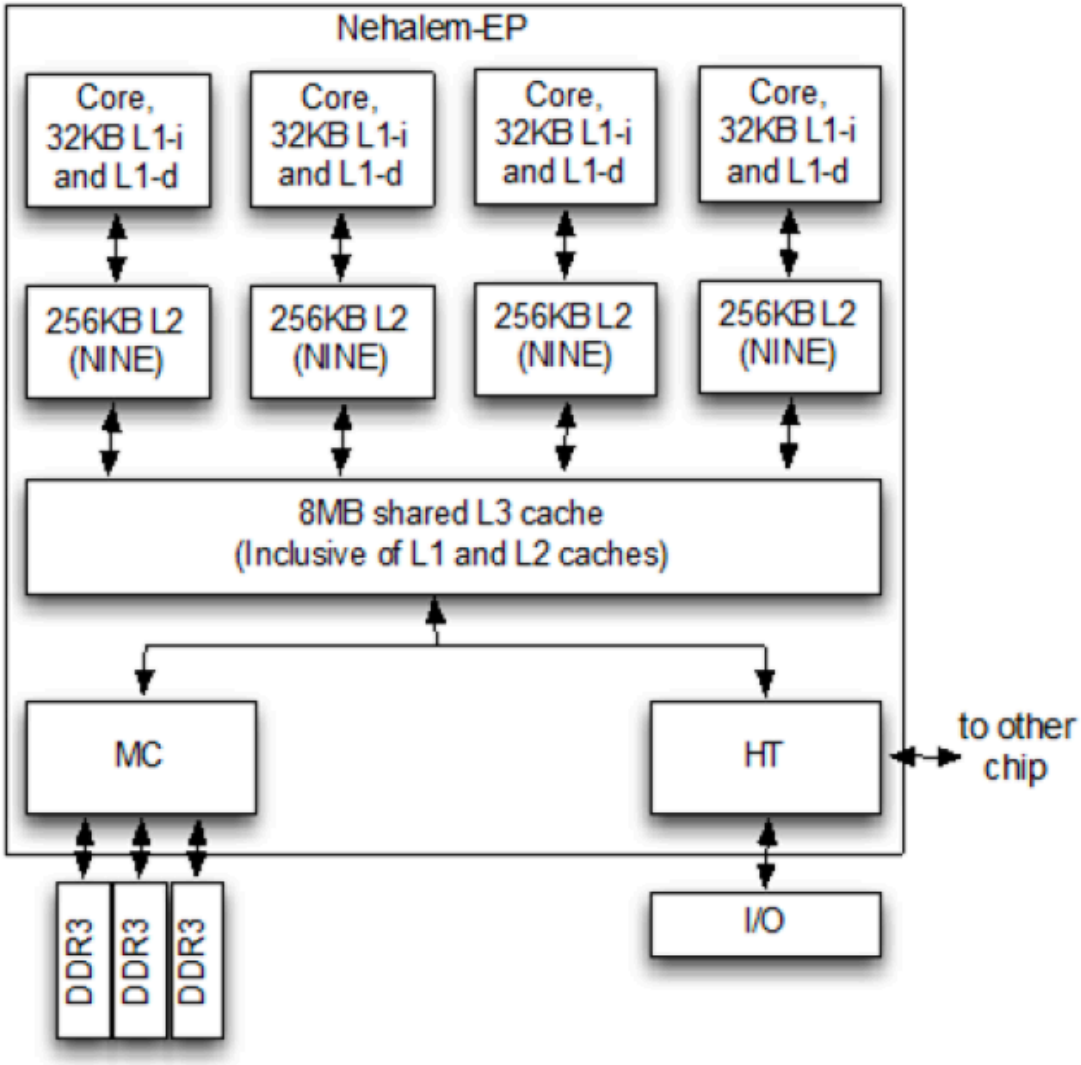
Nehalem-EP
Core, 32KB L1-i and L1-d
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8MB shared L3 cache (Inclusive of L1 and L2 caches)
MC
HT
to other chip
DDR3
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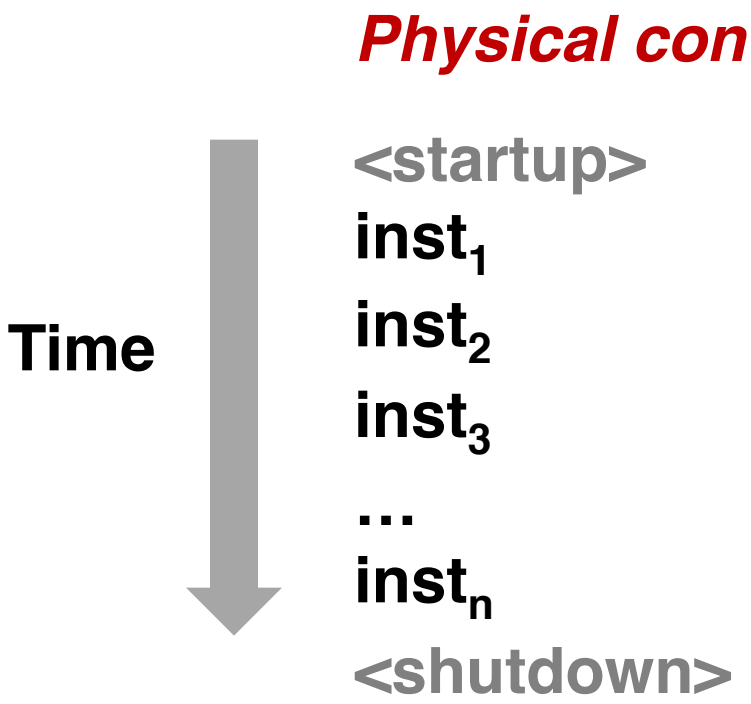
I/O

So Far in CSC252…

- Processors do only one thing:
  - From startup to shutdown, a CPU simply reads and executes (interprets) a sequence of instructions, one at a time
  - This sequence is the CPU's *control flow* (or flow of control)



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- Higher level mechanisms
  - 2. **Process context switch**
    - Implemented by OS software and hardware timer
  - 3. **Signals**
    - Implemented by OS software
  - 4. **Nonlocal jumps**: `setjmp()` and `longjmp()`
    - Implemented by C runtime library

Today

- Exceptions/Interrupts
- Processes and Signals: Special kinds of exception

Exceptions

- An *exception* is a transfer of control to the OS *kernel* in response to some *event* (i.e., change in processor state)
  - Kernel is the memory-resident part of the OS
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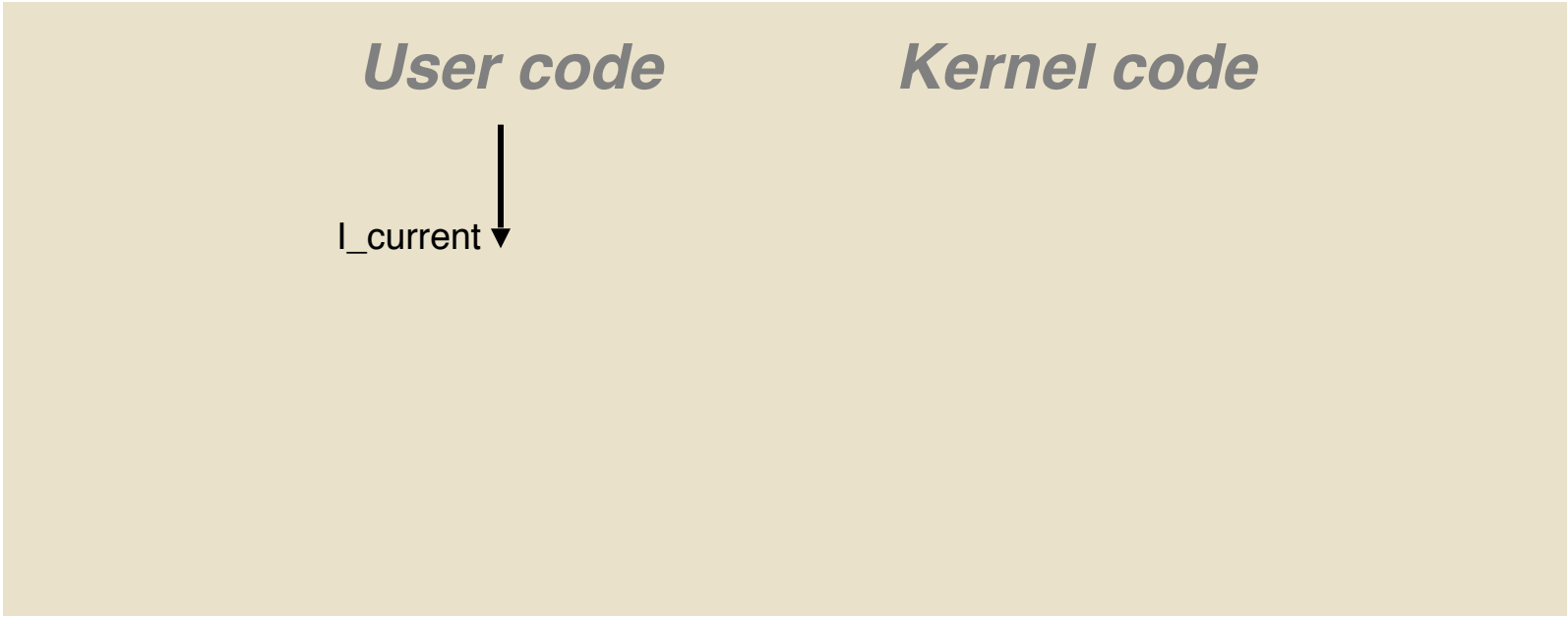

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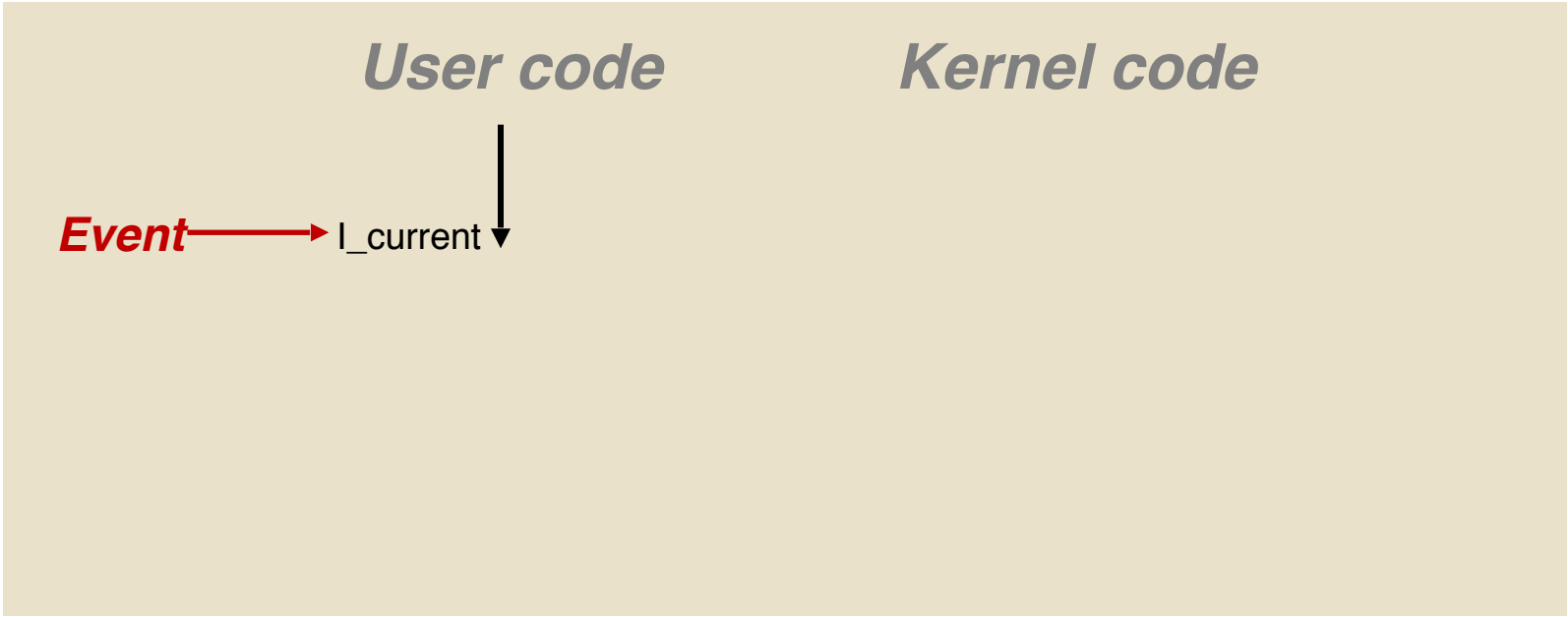

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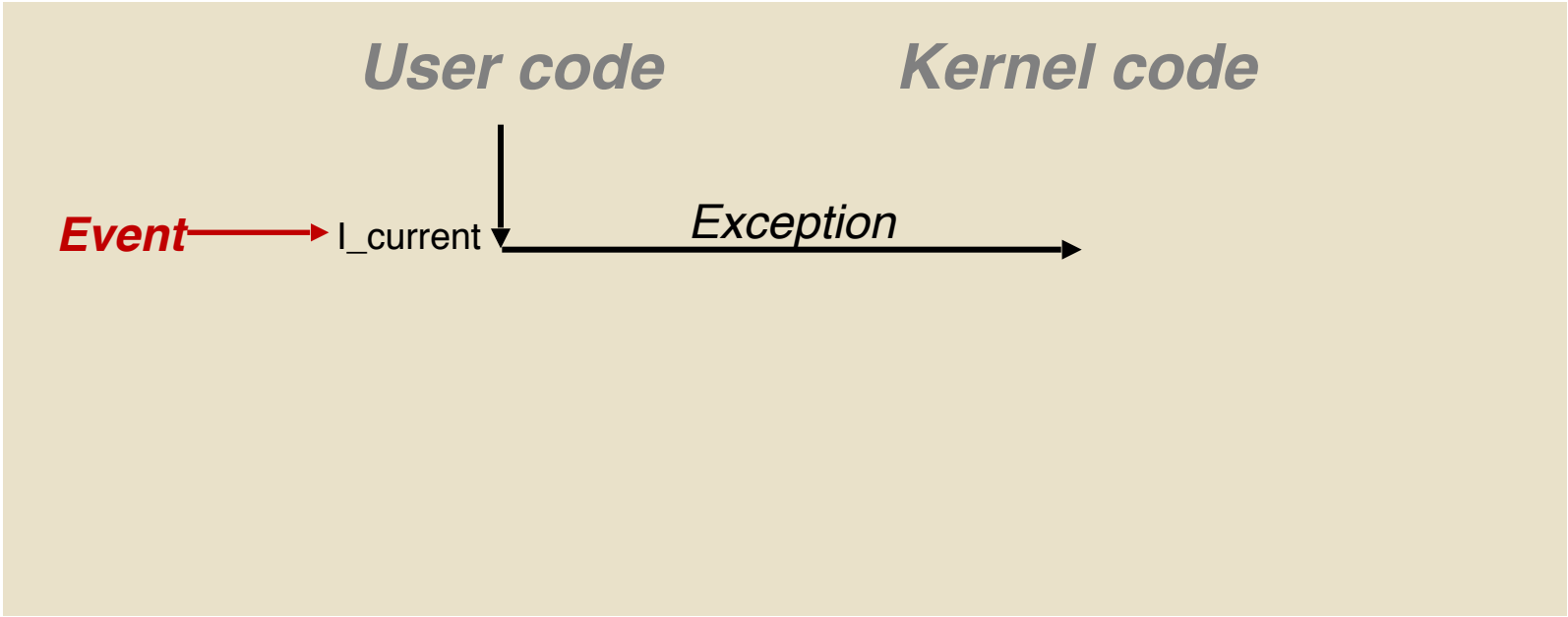

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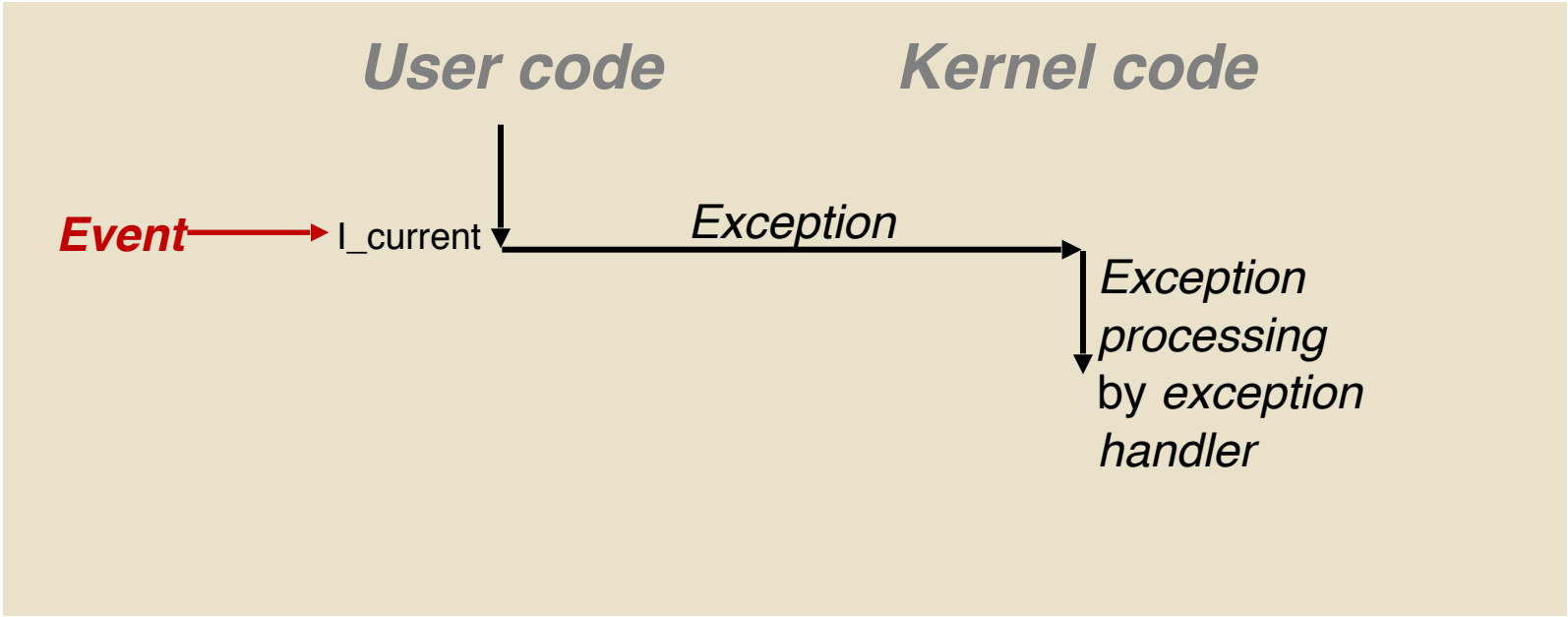

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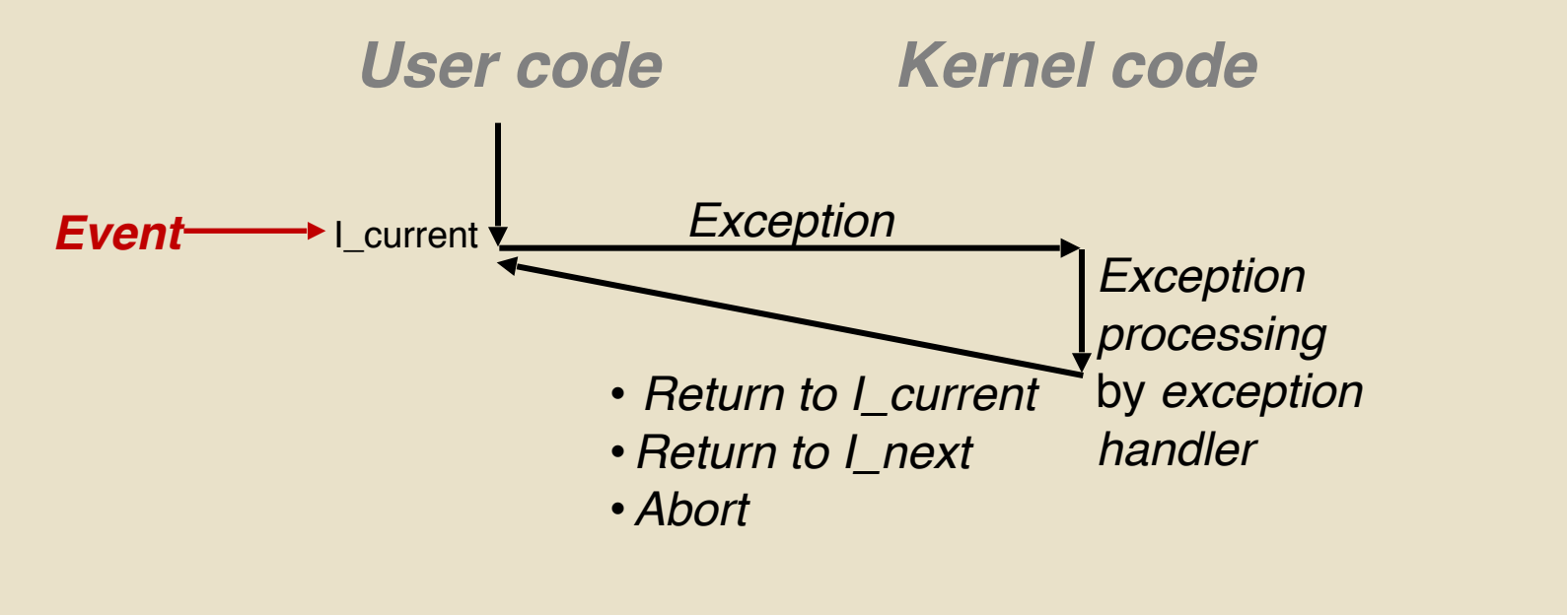

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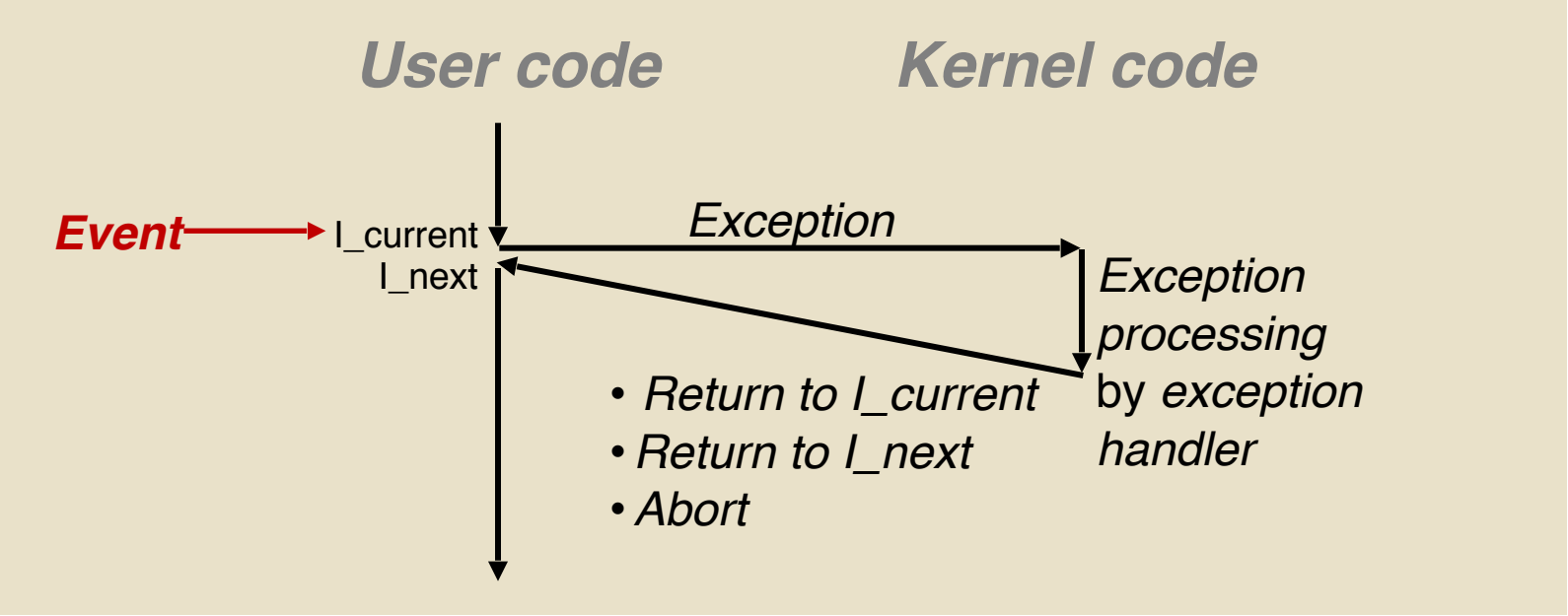

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  - I/O interrupt from external device
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  - *Aborts*
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    - Examples: illegal instruction, parity error, machine check
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- User writes to memory location
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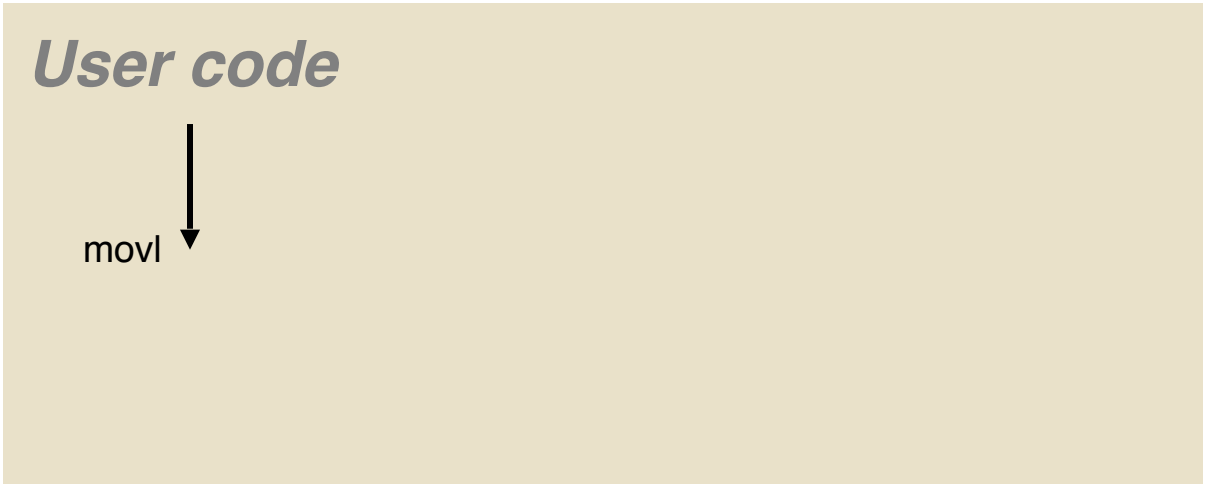

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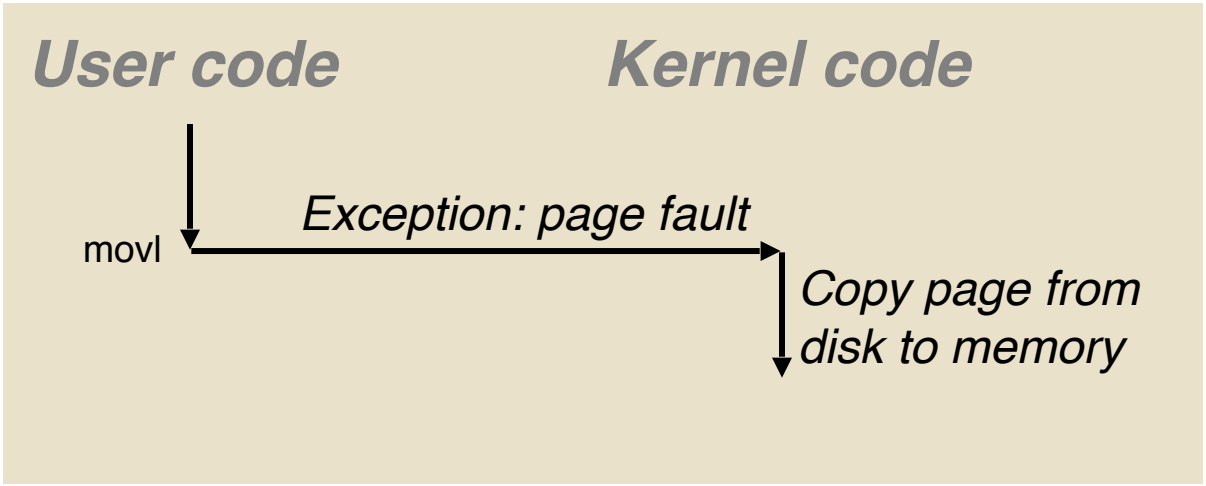

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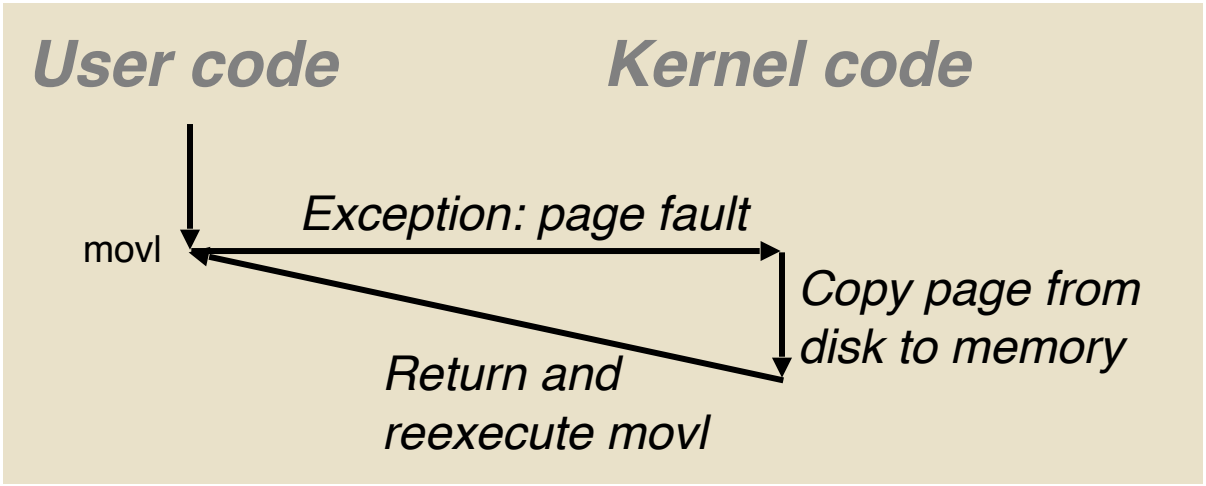

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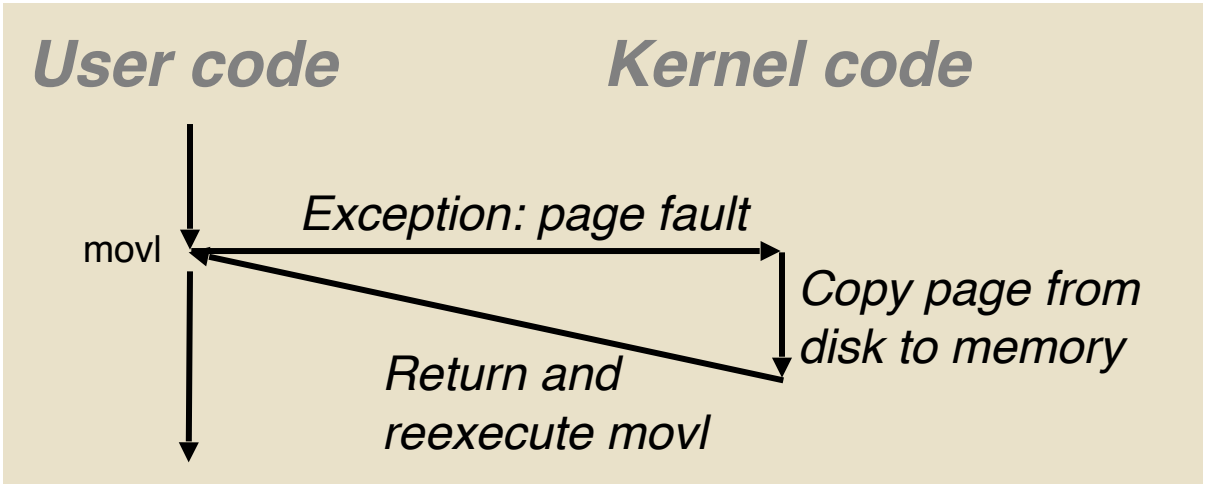

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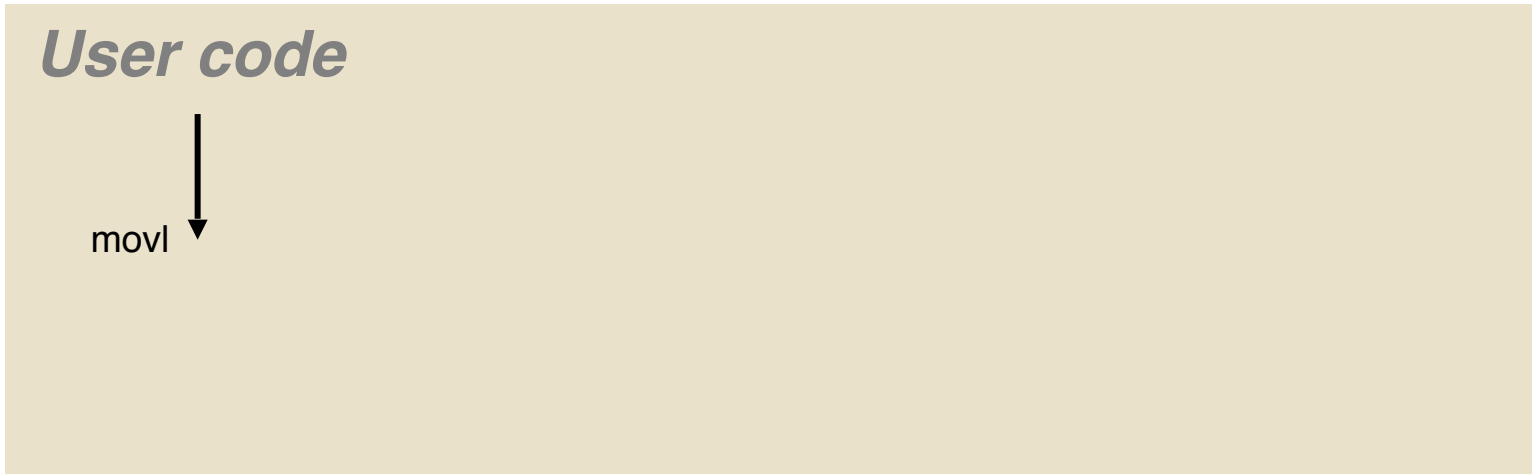

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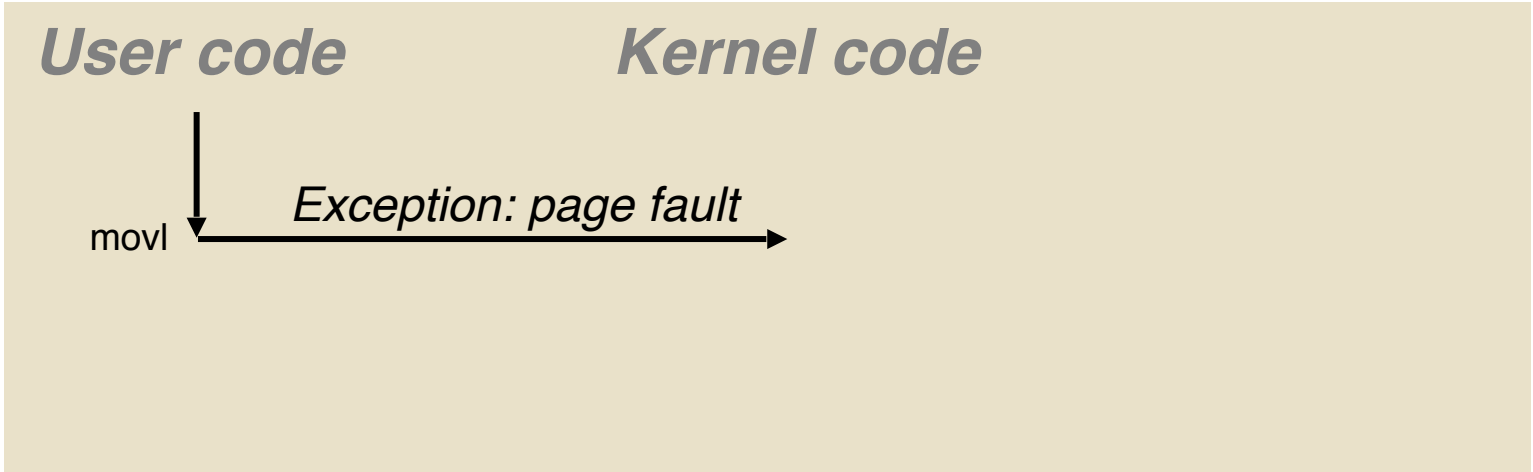

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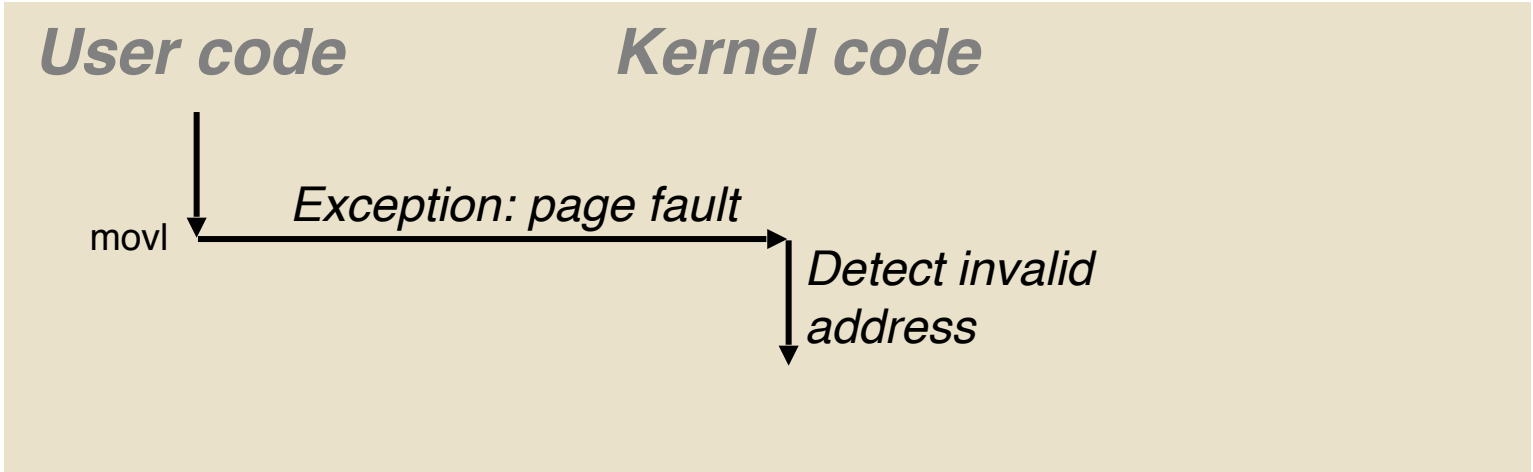

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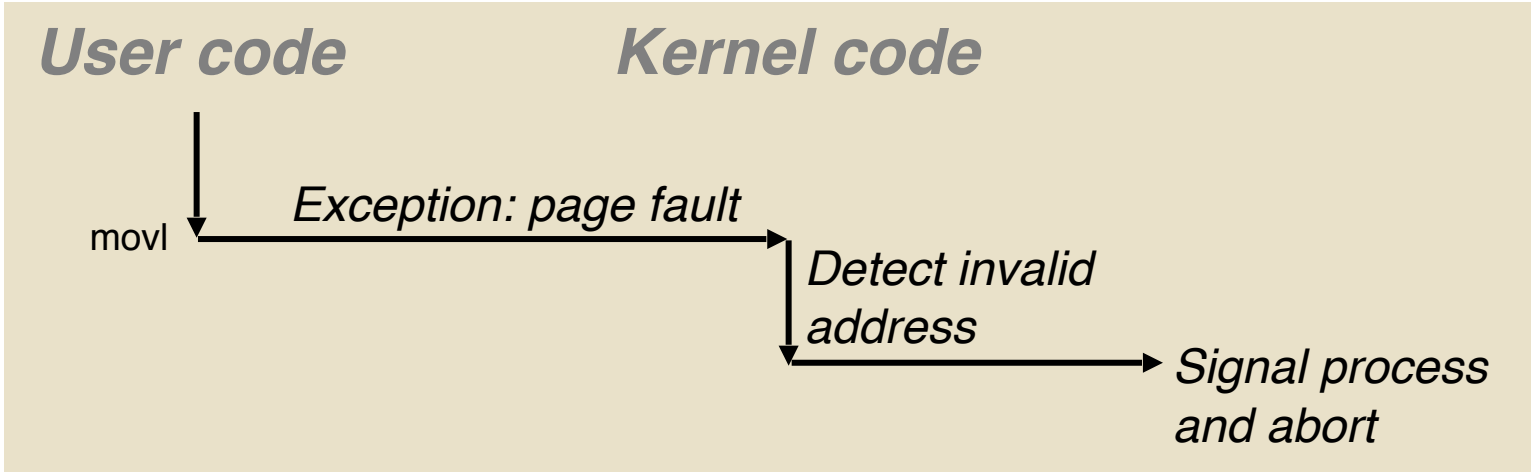

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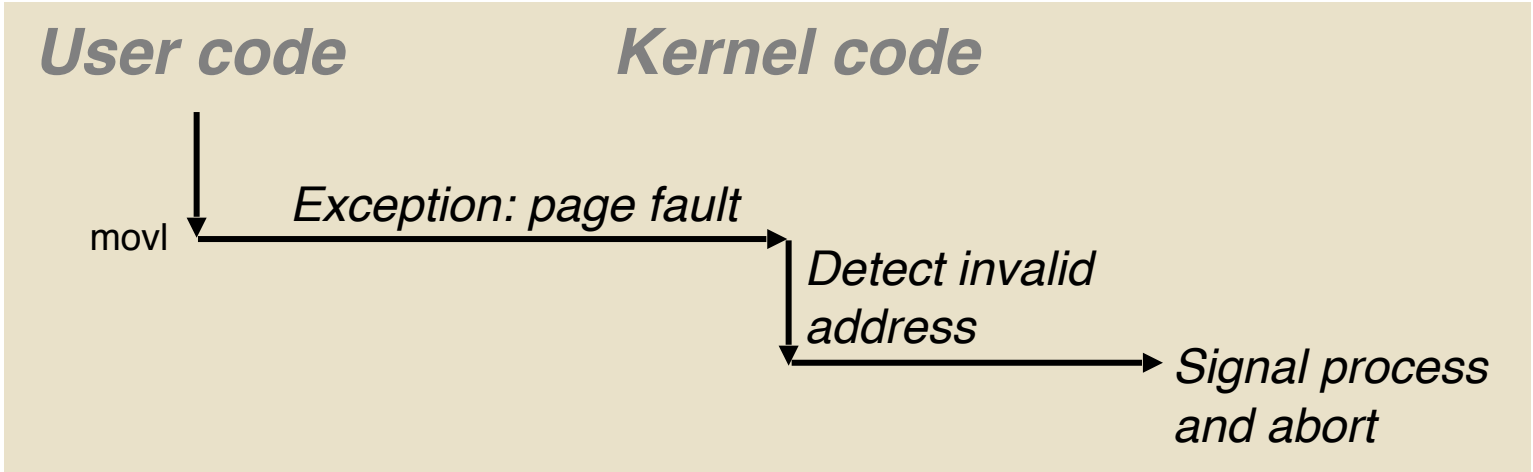

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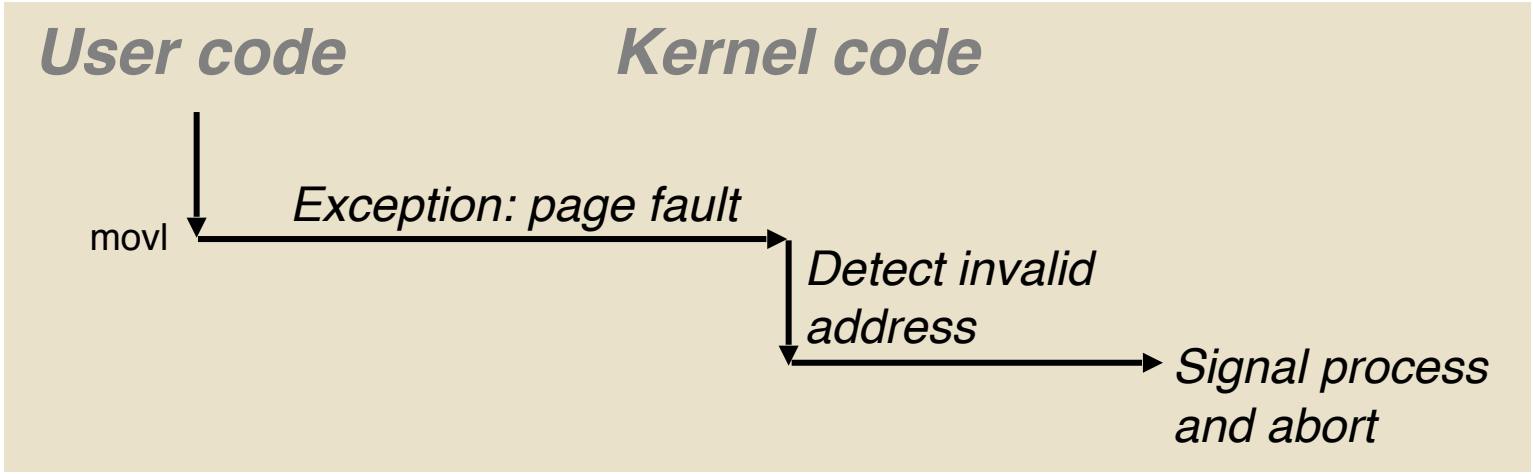

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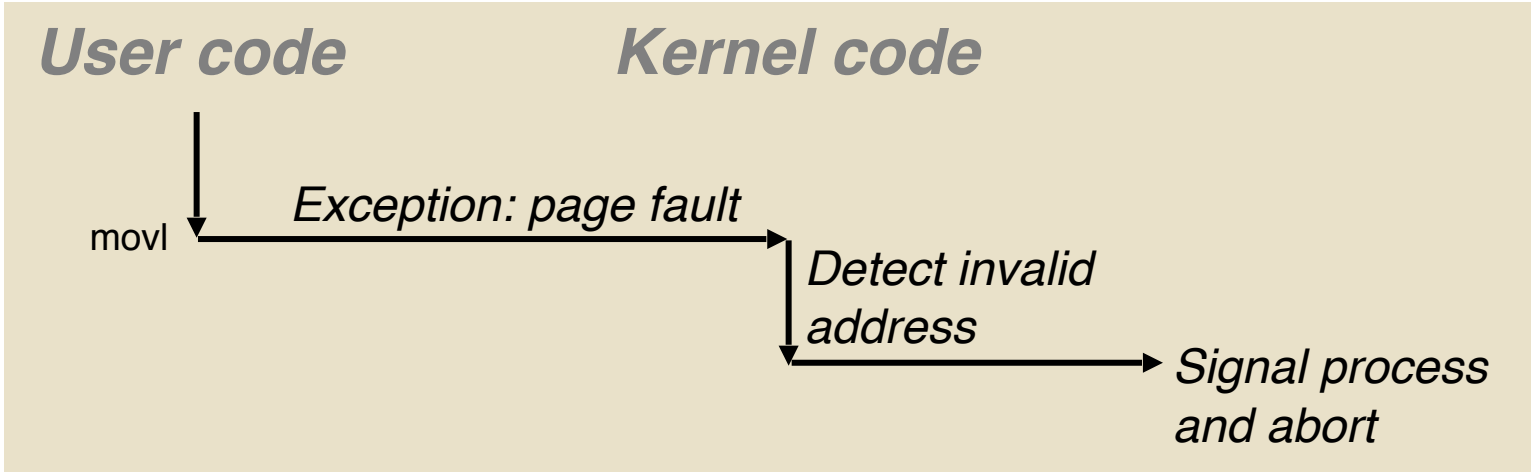

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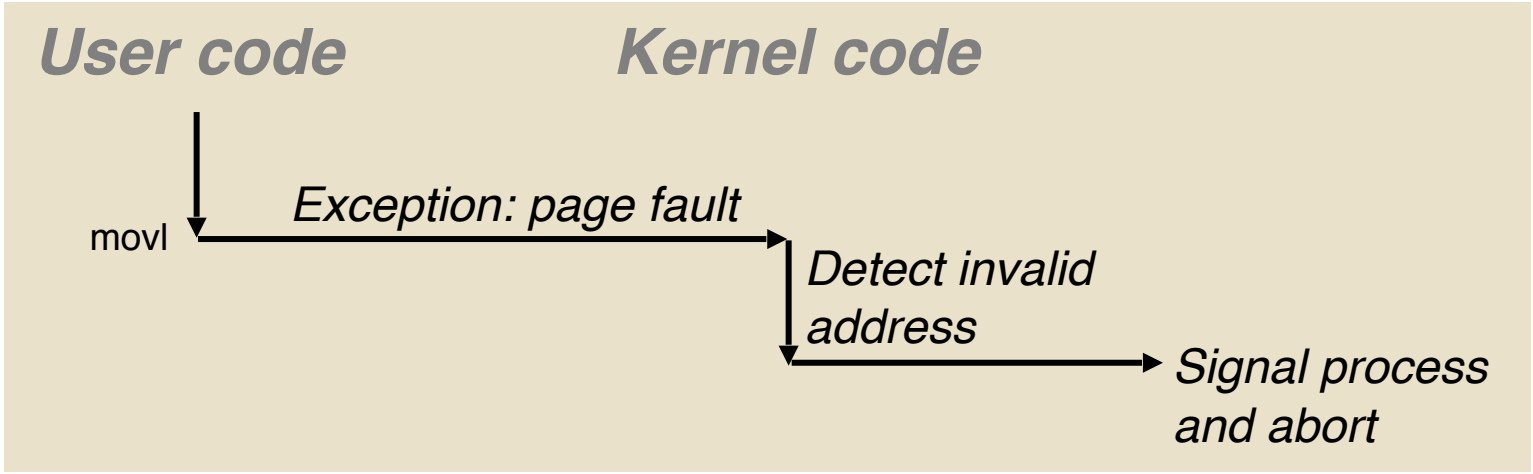

Others' Definitions

- The textbook's definitions are not universally accepted
- Intel (http://www.intel.com/cd/ids/developer/asmo-na/eng/microprocessors/ia32/xeon/19250.htm?page=2)
  - **Interrupt**: An exception that comes from outside of the processor. There are two kinds of exceptions: local and external. A local exception is generated from a program. External exceptions are usually generated by external I/O devices and received at exception pins.
- PowerPC Architecture
  - Interrupts "allow the processor to change state as a result of external signals, errors, or unusual conditions arising in the execution of instructions"
- PowerPC 604
  - Everything is an exception
- Motorola 68K
  - Everything is an exception
- VAX
  - Interrupts: device, software, urgent
  - Exceptions: faults, traps, aborts

When Do You Call the Handler?

- Interrupts: when convenient. Typically wait until the current instructions in the pipeline are finished
- Exceptions: typically immediately as programs can't continue without resolving the exception (think of page fault)
- Maskable verses Unmaskable
  - Interrupts can be individually masked (i.e., ignored by CPU)
  - Synchronous exceptions are usually unmaskable
- Some interrupts are intentionally unmaskable
  - Called non-maskable interrupts (NMI)
  - Indicating a critical error has occurred, and that the system is probably about to crash

Where Do You Restart?

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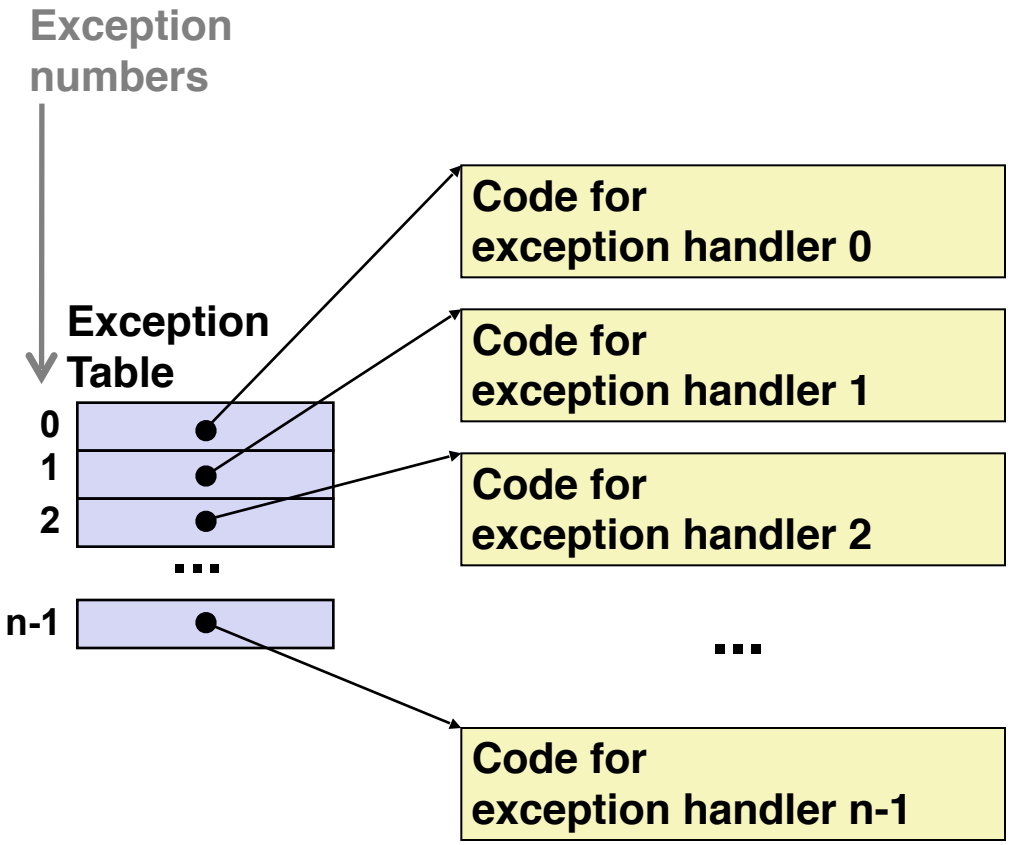
Where to Find Exception Handlers?



- Each type of event has a unique exception number k
- k = index into exception table
- Exception table lives in memory. Its start address is stored in a special register
- Handler k is called each time exception k occurs

Nested Exceptions

- One interrupt/exception occurs when another is already active
- Can fundamentally do it
  - Subroutine calls within subroutine calls
  - Handlers need to save appropriate state

Concurrent Interrupts

- More than one interrupts happen at the same time
- Pre-defined priority
- The chipset arbitrates which one to respond to first

Today

- Exceptions/Interrupts
- Processes and Signals: Special kinds of exception
  - Processes
  - Process Control
  - Signals

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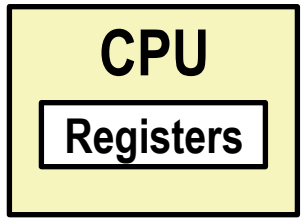
  - *“Owns” the CPU*



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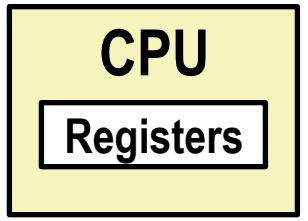

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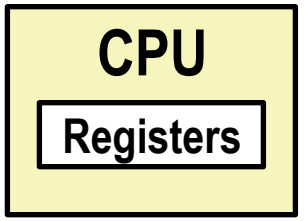

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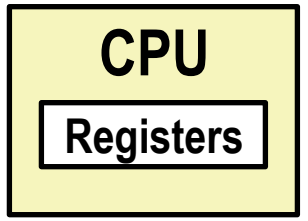

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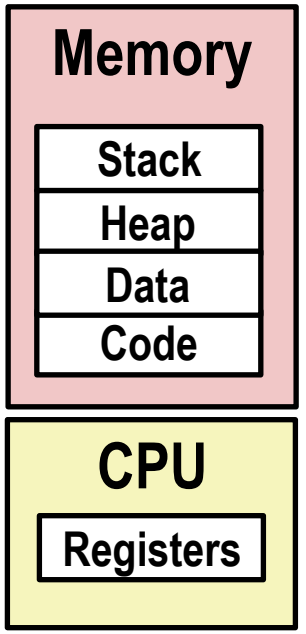

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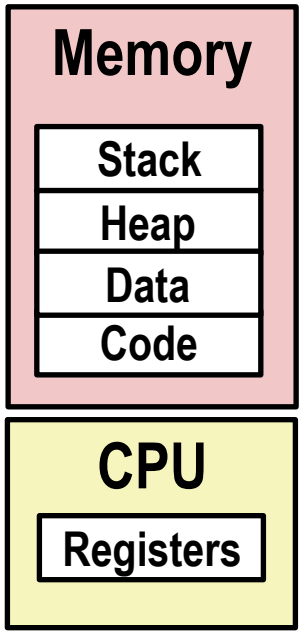

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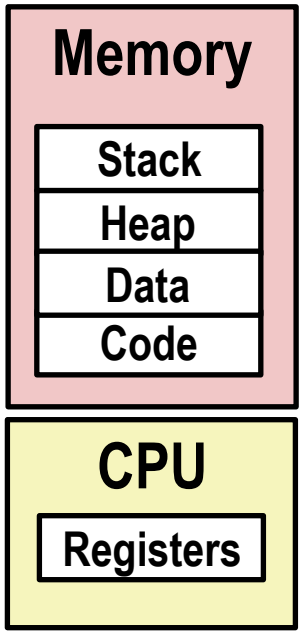
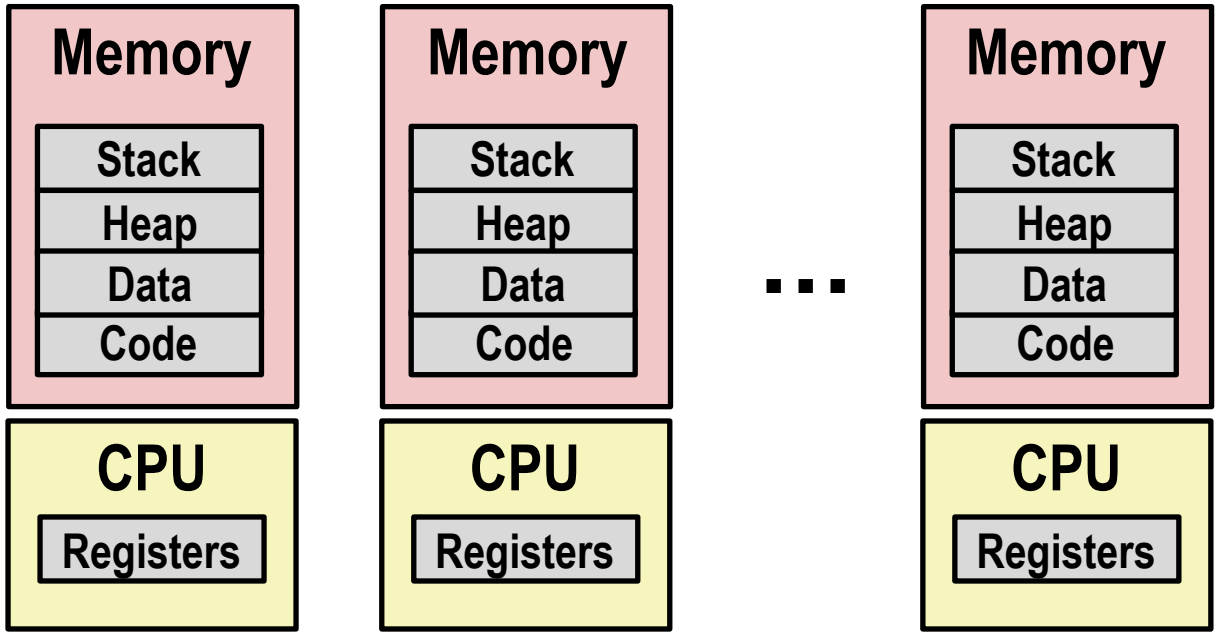
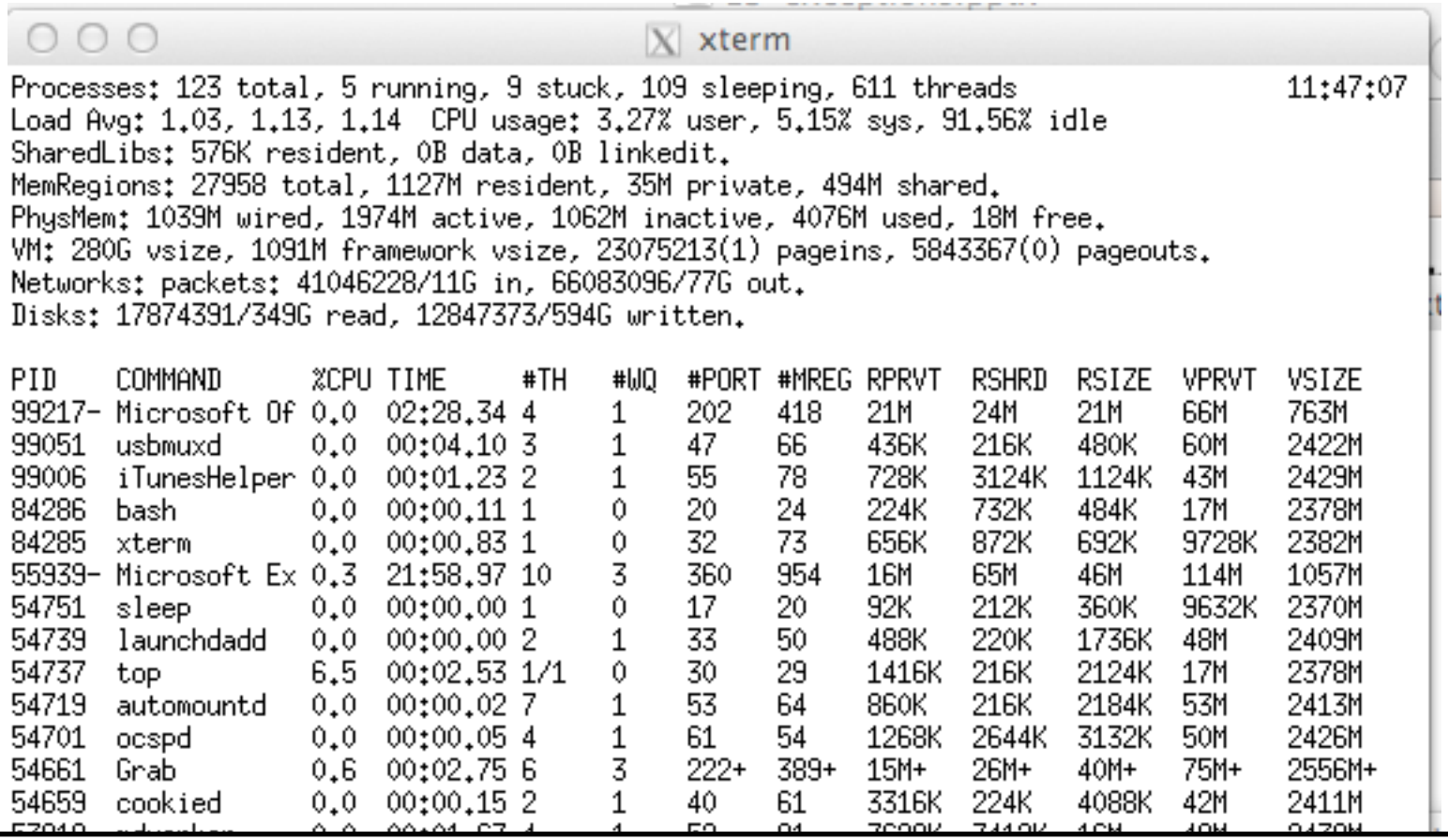


Multiprocessing: The Illusion



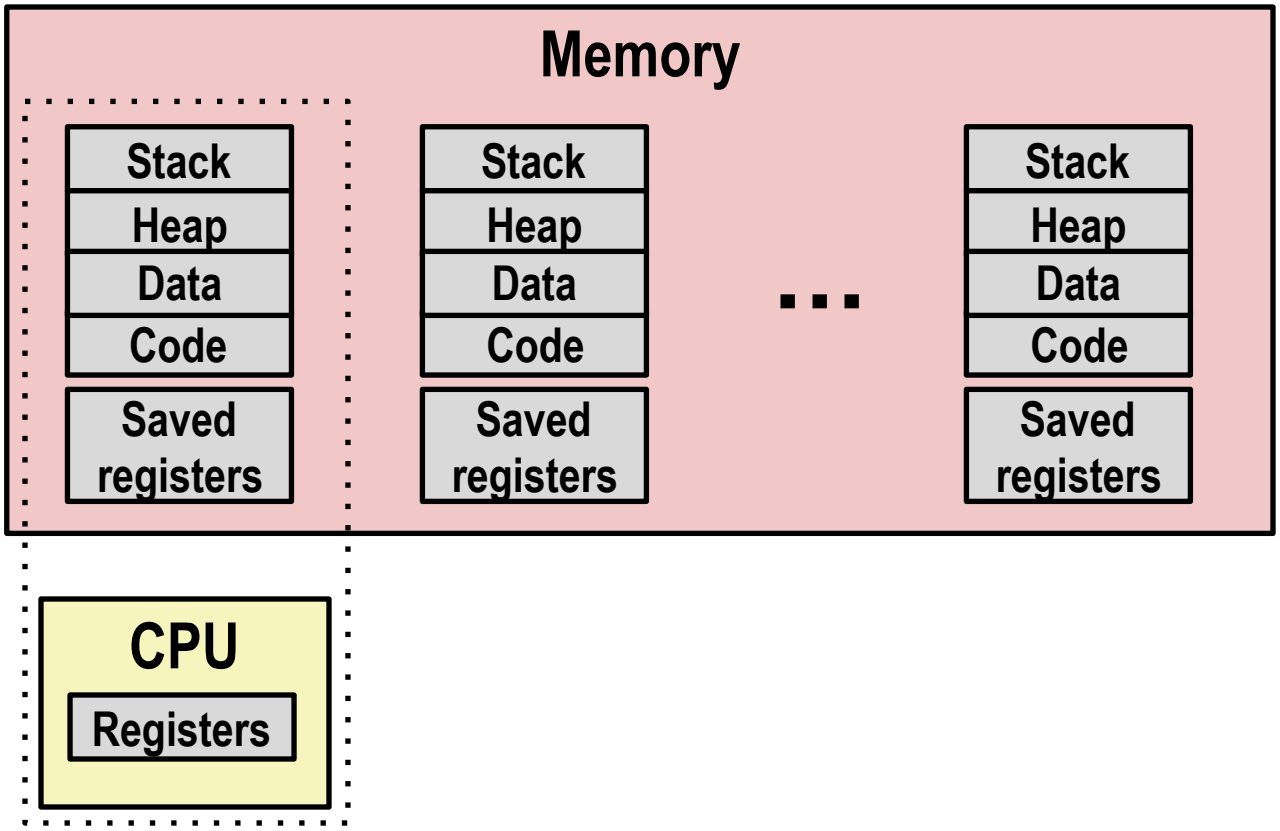
- Computer runs many processes simultaneously
  - Applications for one or more users
    - Web browsers, email clients, editors, …
  - Background tasks
    - Monitoring network & I/O devices

Multiprocessing Example



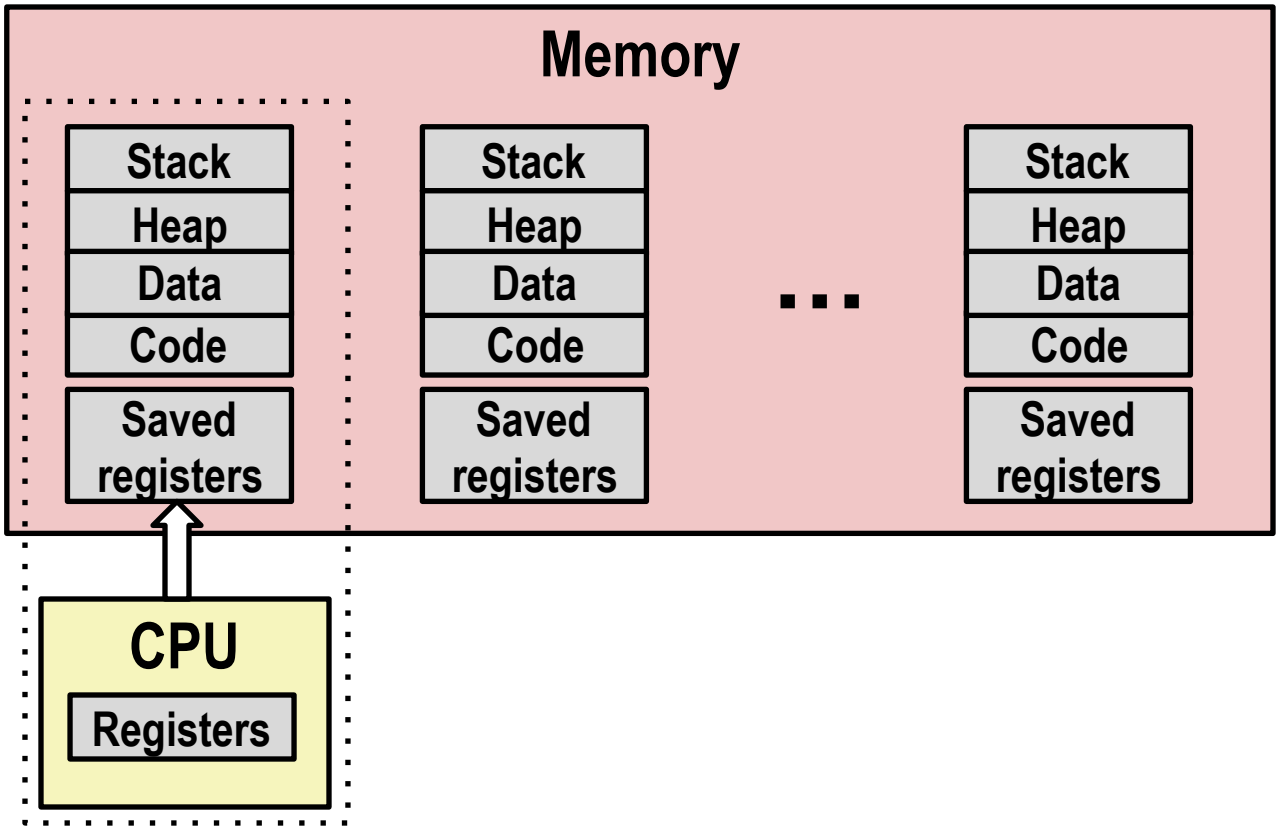
- Running program “top” on Mac
  - System has 123 processes, 5 of which are active
  - Identified by Process ID (PID)

Multiprocessing: The (Traditional) Reality



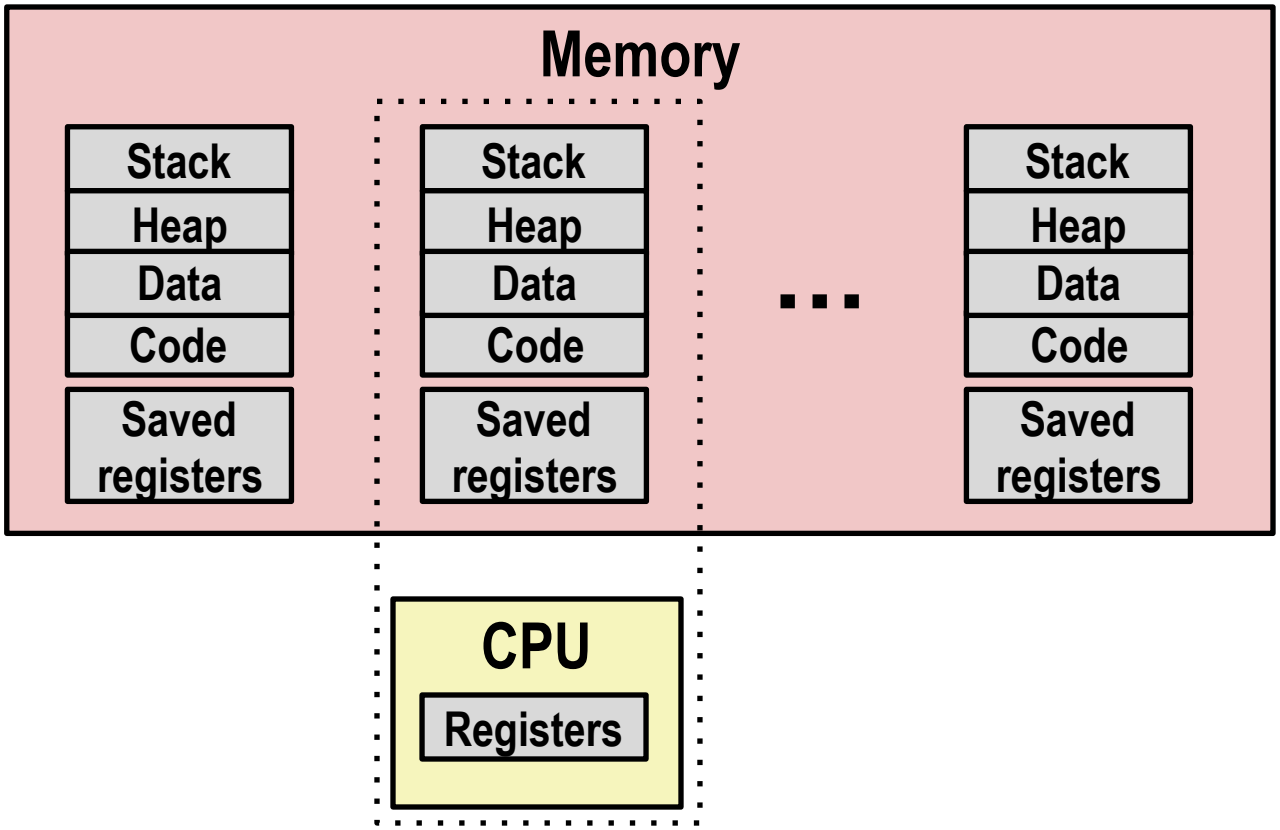
- Single processor executes multiple processes concurrently
  - Process executions interleaved (multitasking)
  - Address spaces managed by virtual memory system (later in course)
  - Register values for nonexecuting processes saved in memory

Multiprocessing: The (Traditional) Reality



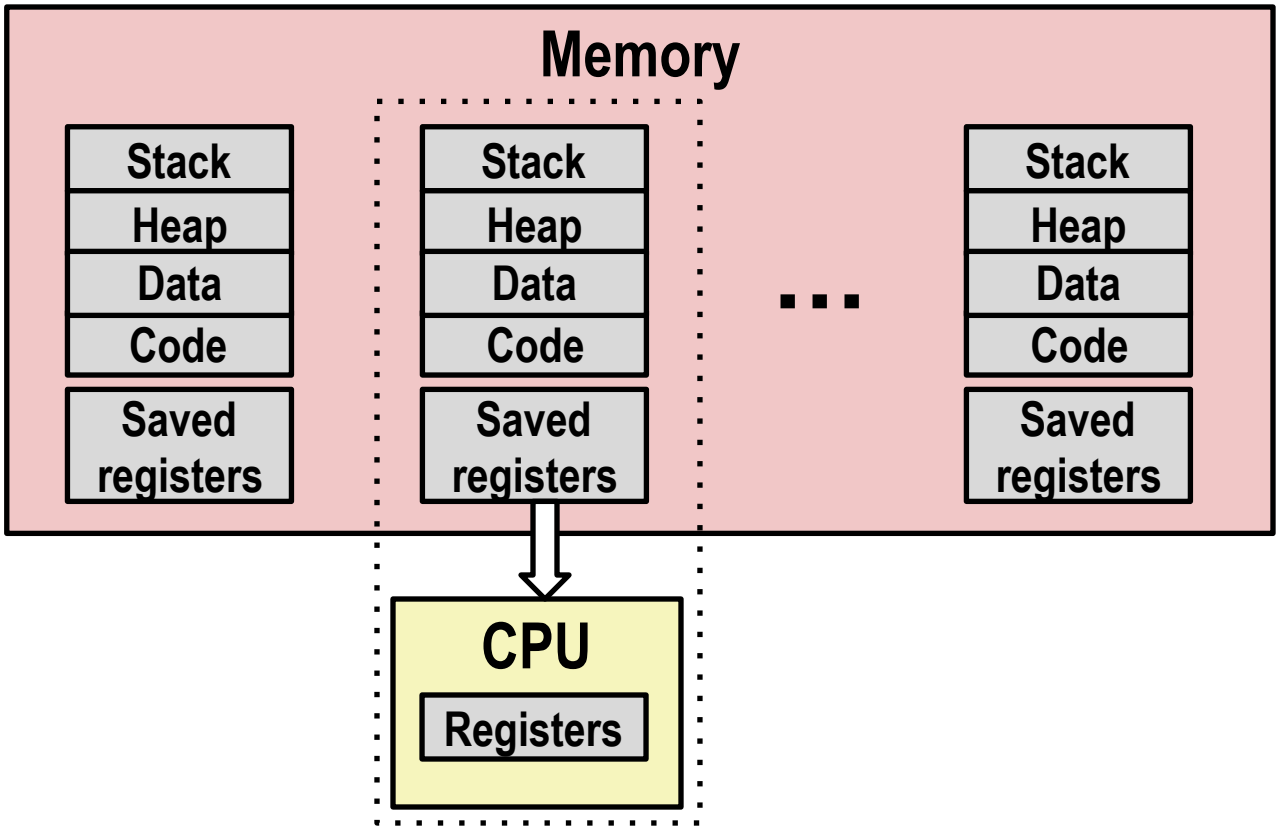
- Save current registers in memory

Multiprocessing: The (Traditional) Reality



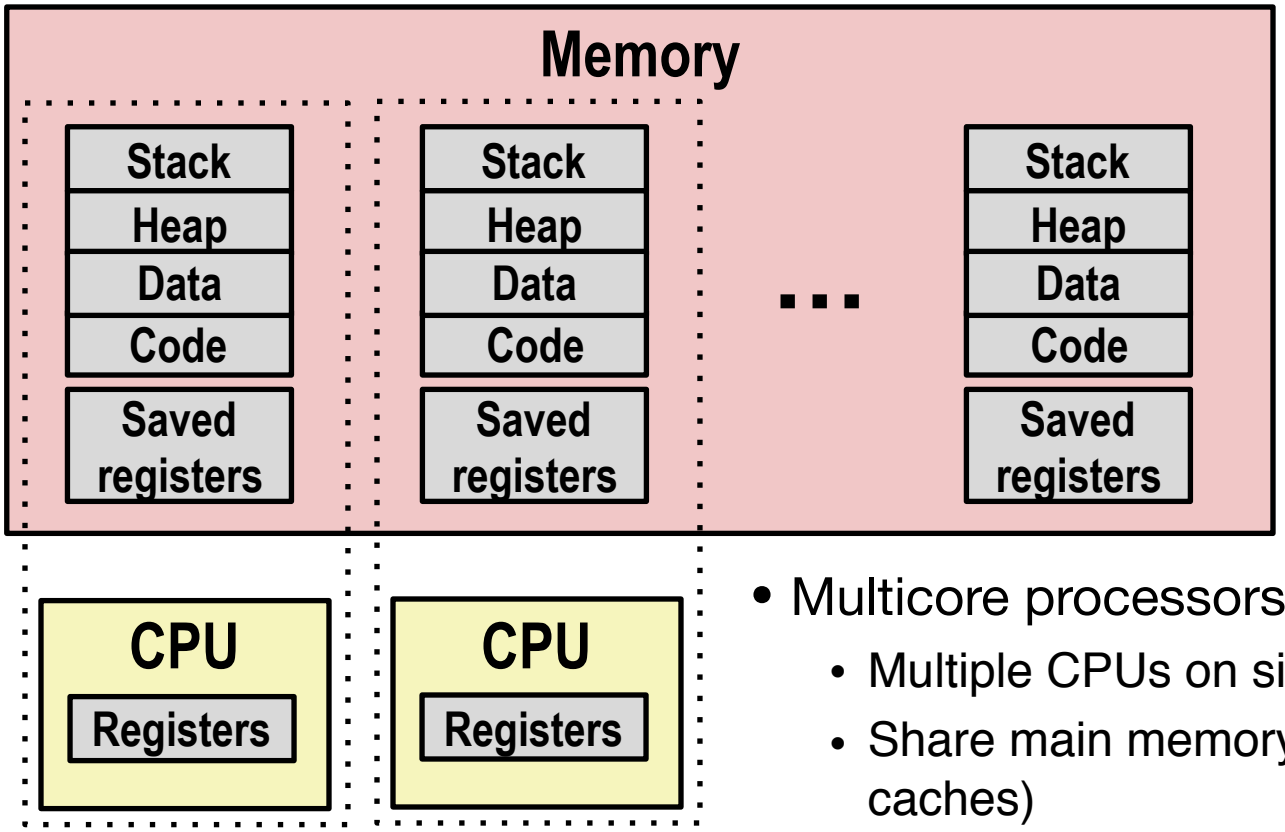
- Schedule next process for execution

Multiprocessing: The (Traditional) Reality



- Load saved registers and switch address space (context switch)

Multiprocessing: The (Modern) Reality



- Multicore processors
  - Multiple CPUs on single chip
  - Share main memory (and some of the caches)
  - Each can execute a separate process
    - Scheduling of processors onto cores done by kernel

Concurrent Processes

- Each process is a logical control flow.
- Two processes *run concurrently* (*are concurrent)* if their flows overlap in time
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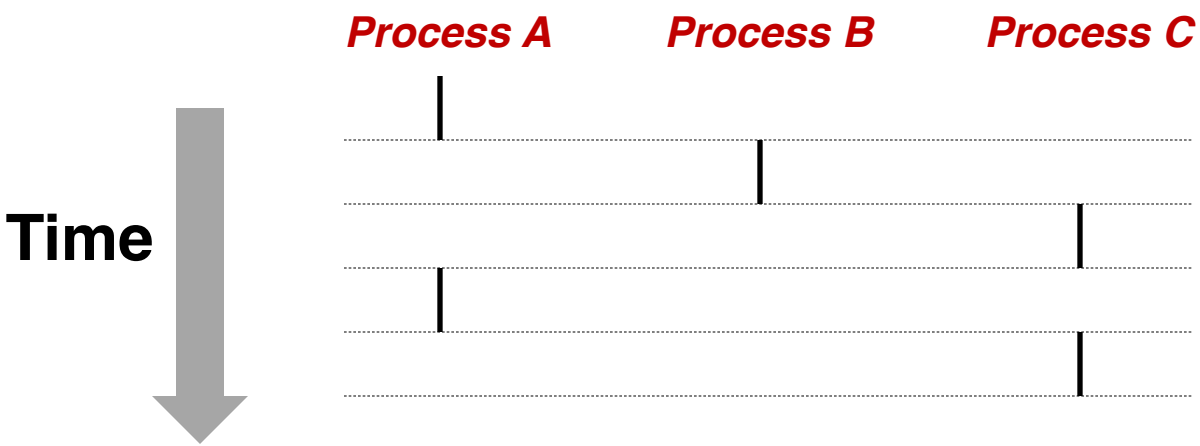

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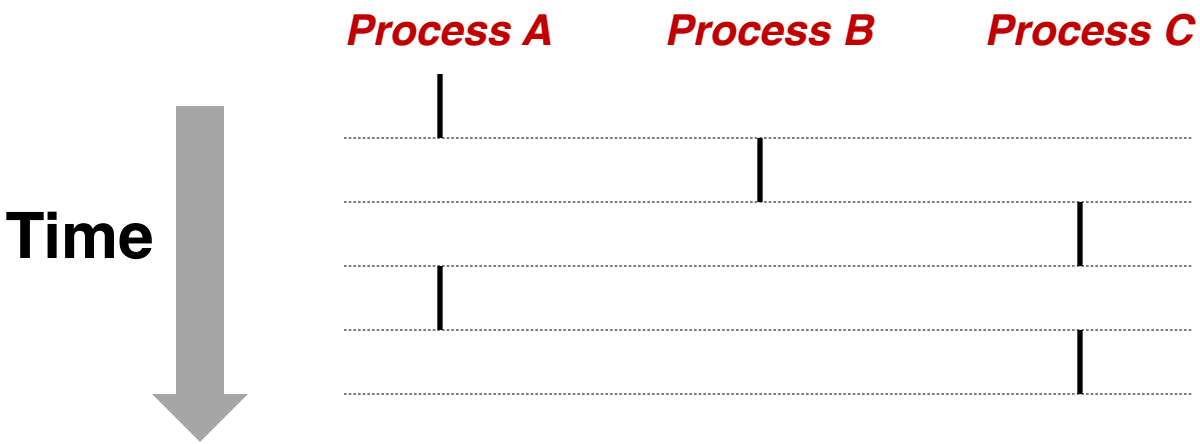

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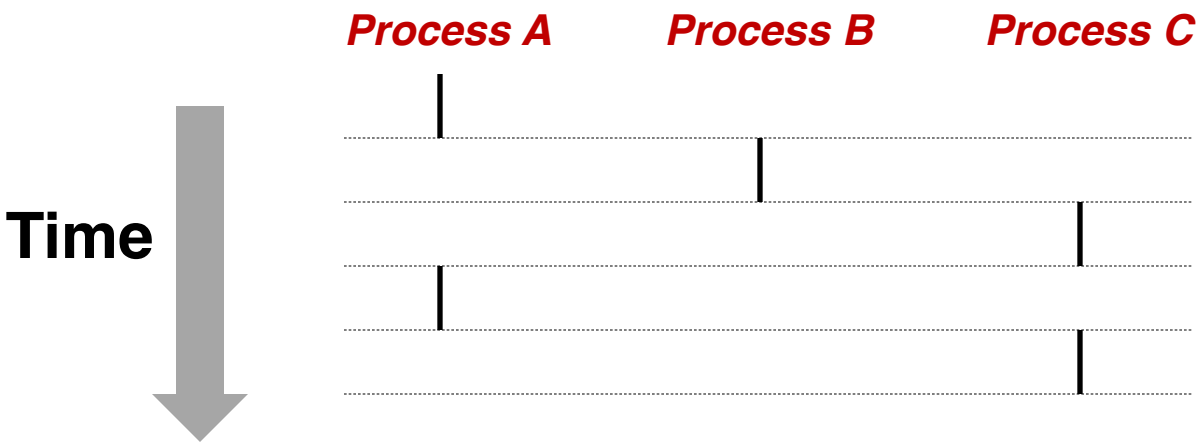
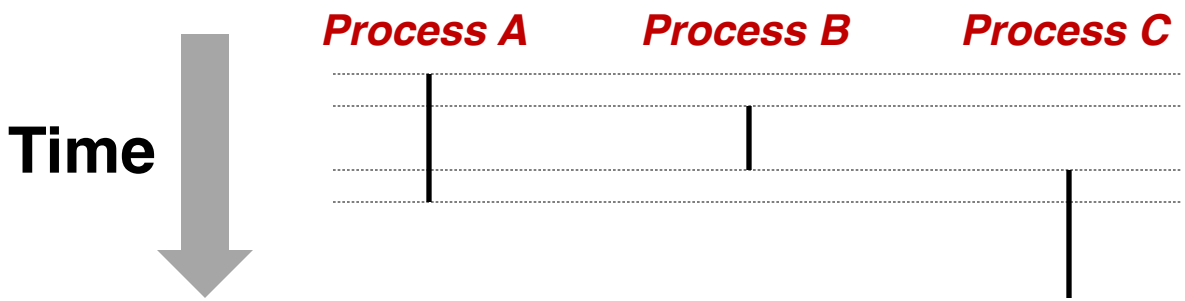


User View of Concurrent Processes

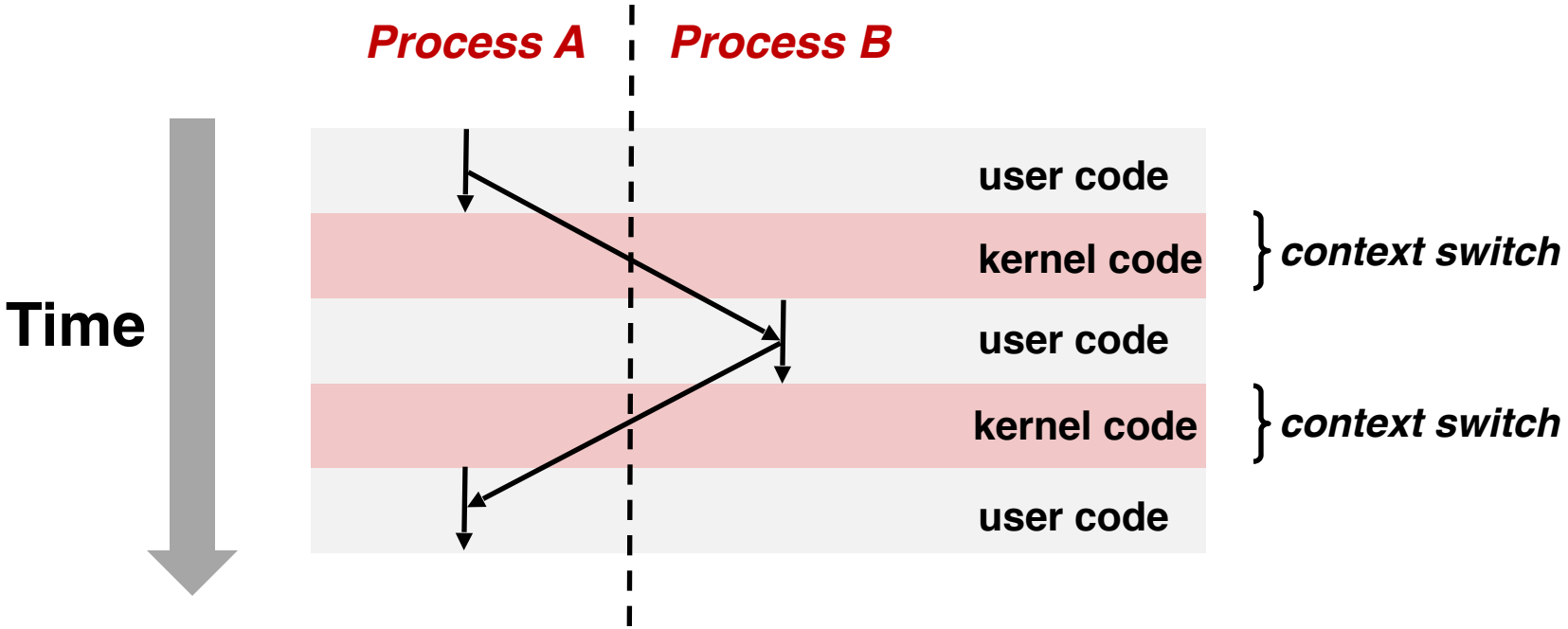
- Control flows for concurrent processes are physically disjoint in time

- However, we can think of concurrent processes as running in parallel with each other



Context Switching

- Processes are managed by a shared chunk of memory-resident OS code called the *kernel*
  - Important: the kernel is not a separate process, but rather runs as part of some existing process.
- Control flow passes from one process to another via a *context switch*



Today

- Exceptions/Interrupts
- Processes and Signals: Special kinds of exception
  - Processes
  - Process Control
  - Signals

Obtaining Process IDs

- `pid_t getpid(void)`
  - Returns PID of current process

- `pid_t getppid(void)`
  - Returns PID of parent process

Creating and Terminating Processes

From a programmer's perspective, we can think of a process as being in one of three states

- Running
  - Process is either executing, or waiting to be executed and will eventually be *scheduled* (i.e., chosen to execute) by the kernel
- Stopped
  - Process execution is suspended and will not be scheduled until further notice (through something call **signals**)
- Terminated
  - Process is stopped permanently

Terminating Processes

- Process becomes terminated for one of three reasons:
  - Receiving a signal whose default action is to terminate
  - Returning from the `main` routine
  - Calling the `exit` function

- `void exit(int status)`
  - Terminates with an *exit status* of `status`
  - Convention: normal return status is 0, nonzero on error
  - Another way to explicitly set the exit status is to return an integer value from the main routine

- `exit` is called once but never returns.