CSC 252: Computer Organization
Spring 2020: Lecture 22

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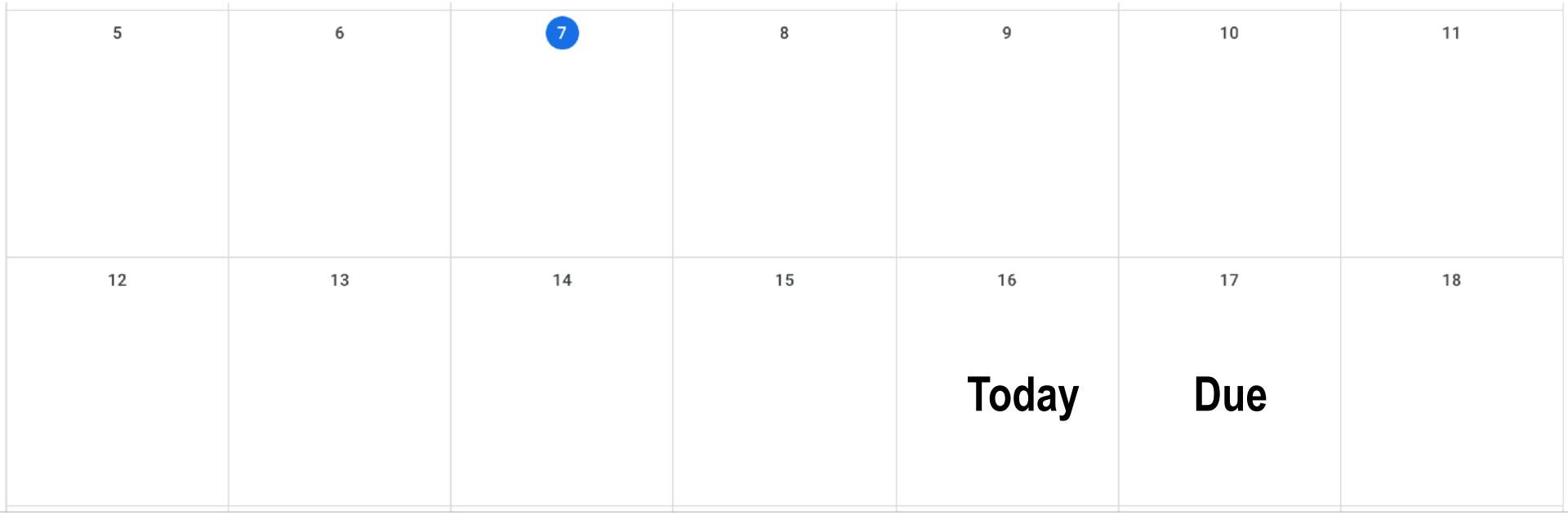
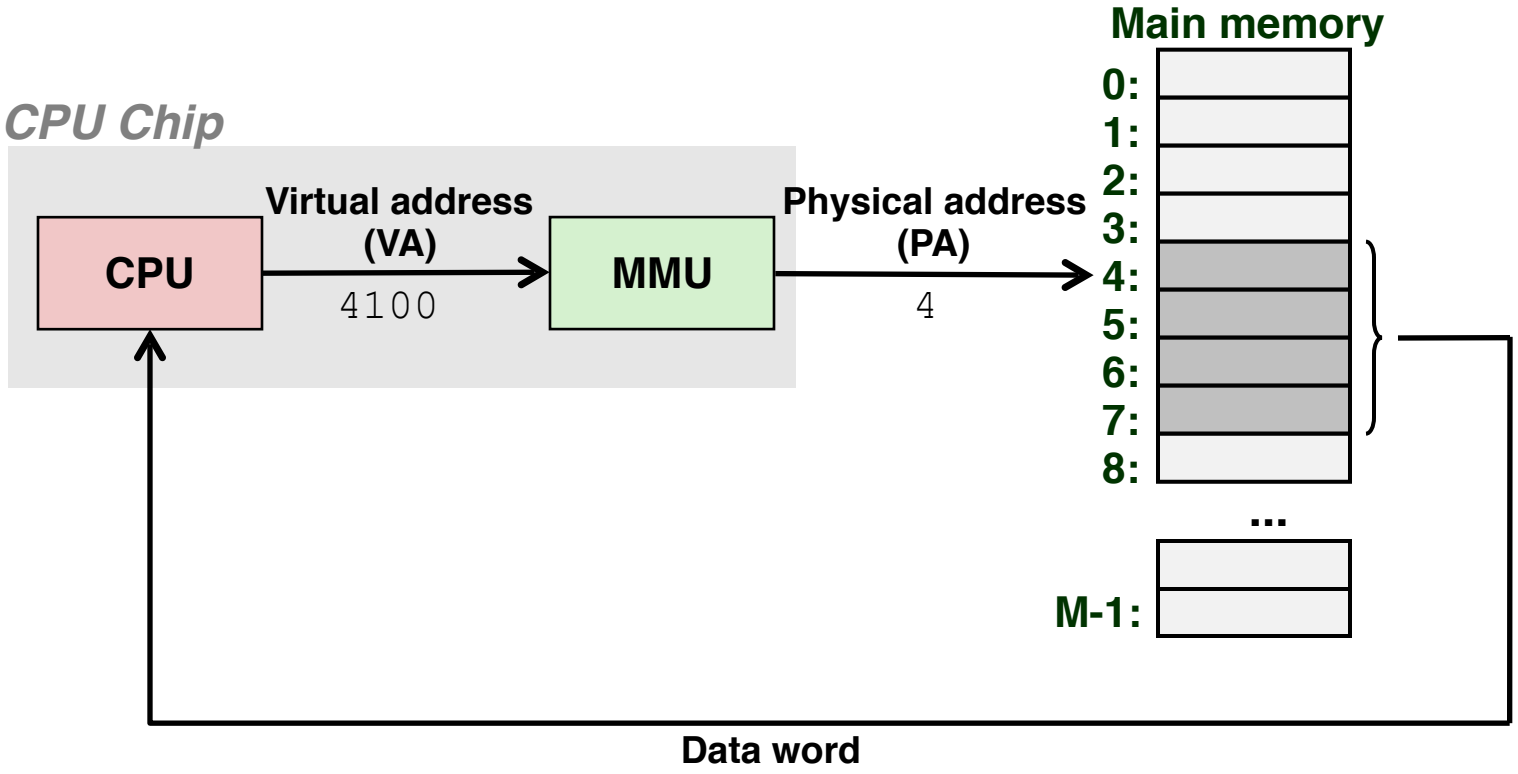
Department of Computer Science
University of Rochester

Announcement

- Programming assignment 4 is out
  - Details: https://www.cs.rochester.edu/courses/252/spring2020/labs/assignment4.html
  - Due on **Apr. 17**, 11:59 PM
  - You (may still) have 3 slip days



A System Using Virtual Addressing



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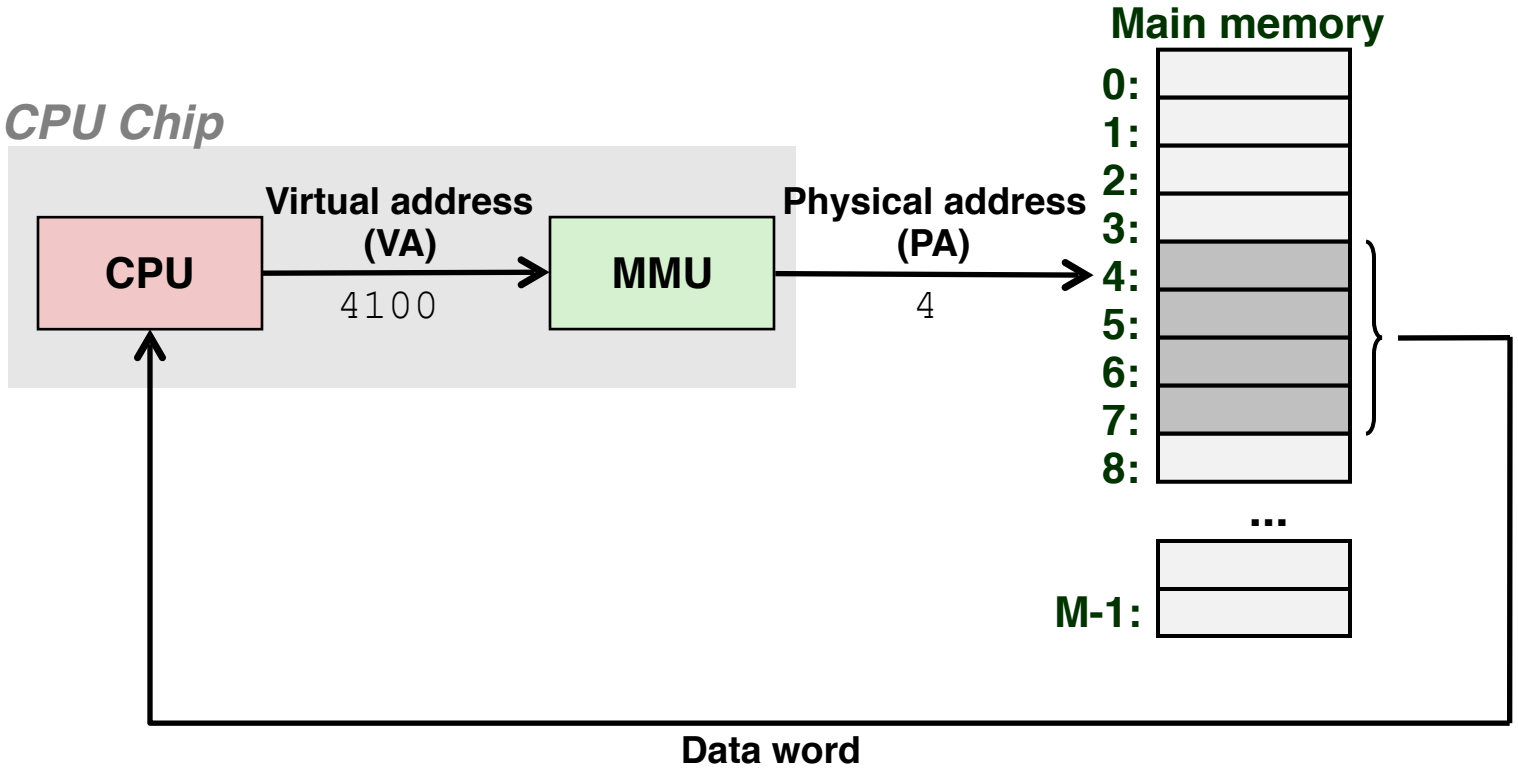


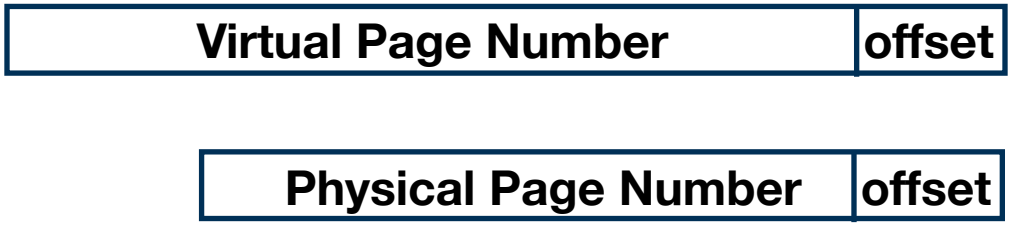
- On a 64-bit machine, virtual memory size = 2^{64}
- Physical memory size is much much smaller:
  - iPhone 8: 2 GB (2^{31})
  - 15-inch Macbook Pro 2017: 16 GB (2^{34})

VM Concepts

- Conceptually, *virtual memory* is an array of N *pages* stored on disk.
- The physical memory is an array of M *pages* stored in DRAM.
- M << N
- Store only the most frequently used pages in the physical memory
- If a page is not on the physical memory, have to first swap it from the disk to the DRAM.

VM Concepts

- Divide both virtual memory (VM) and physical memory (PM) into “pages”



VM Concepts

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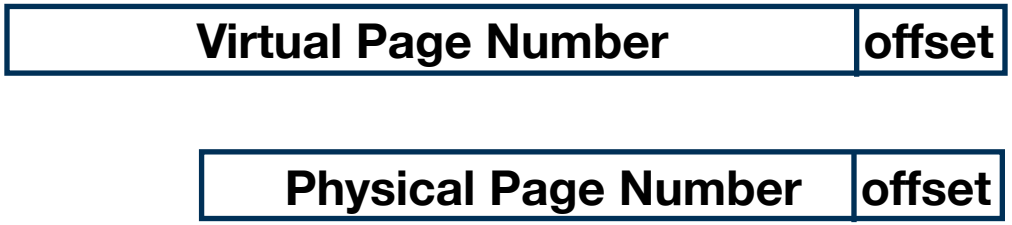

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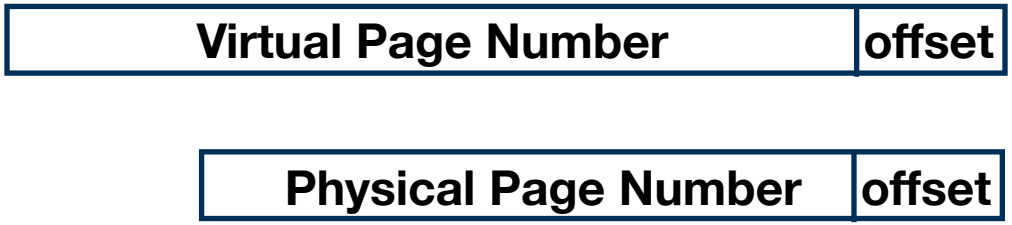

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- How many bits for page offset?
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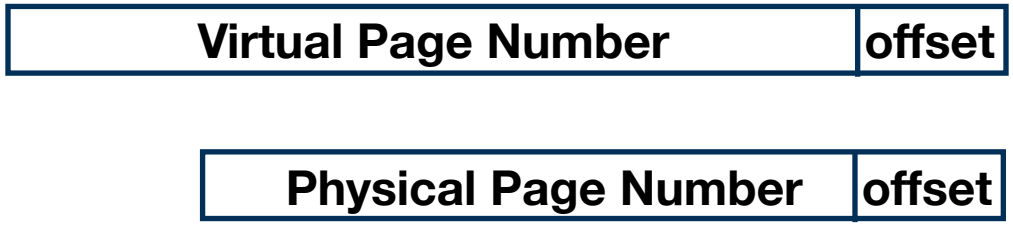

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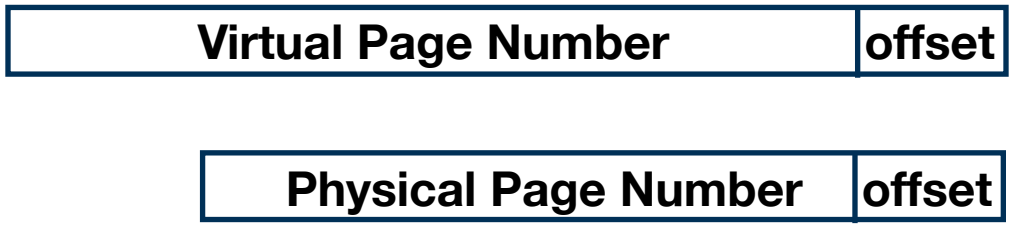
- How many bits for Virtual Page Number?
  - 52, i.e., 2^{52} virtual pages



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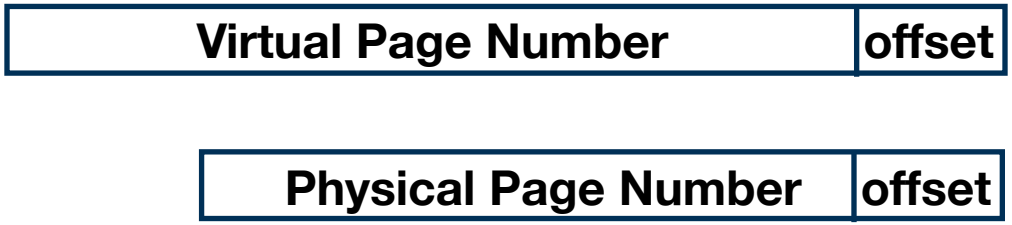
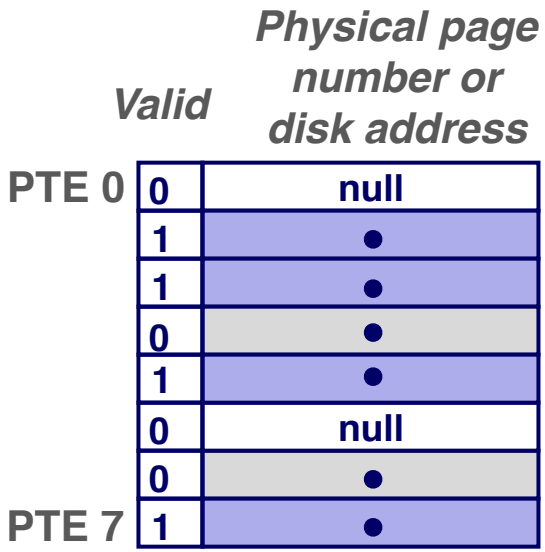
- How many bits for page offset?
  - 12. Same for VM and PM
- How many bits for Virtual Page Number?
  - 52, i.e., 2^{52} virtual pages
- How many bits for Physical Page Number?
  - 20, i.e., 2^{20} physical pages



Page Table: Enabling VA to PA Translation

- A page table is an array of page table entries (PTEs) that maps every virtual page to its physical page.



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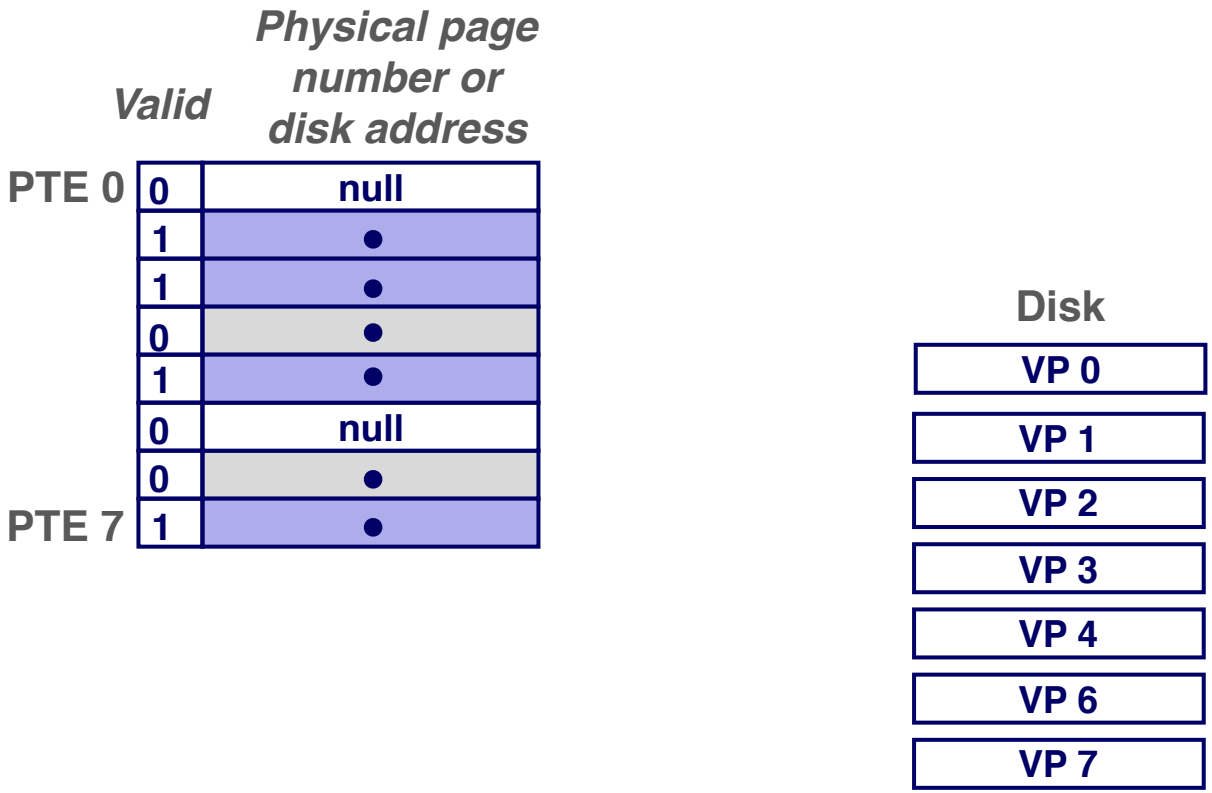

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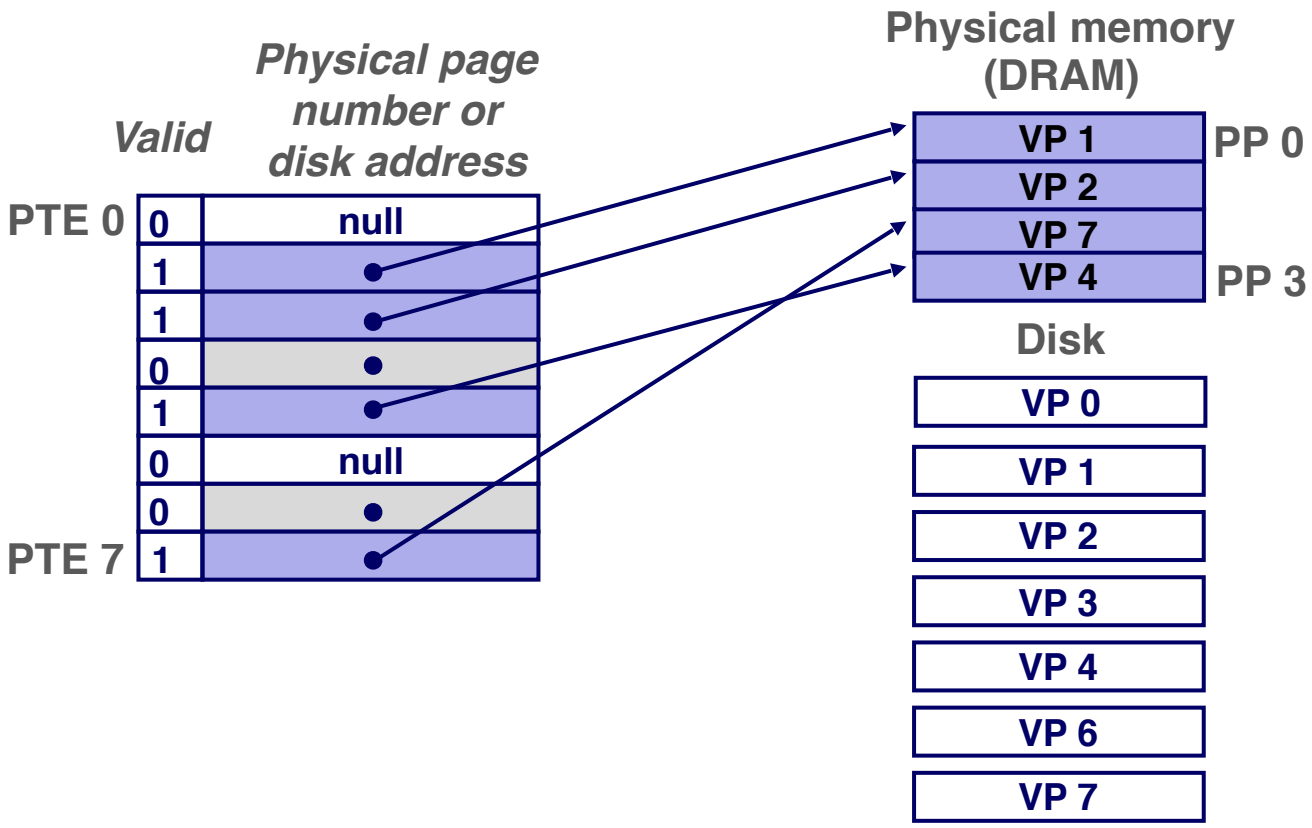

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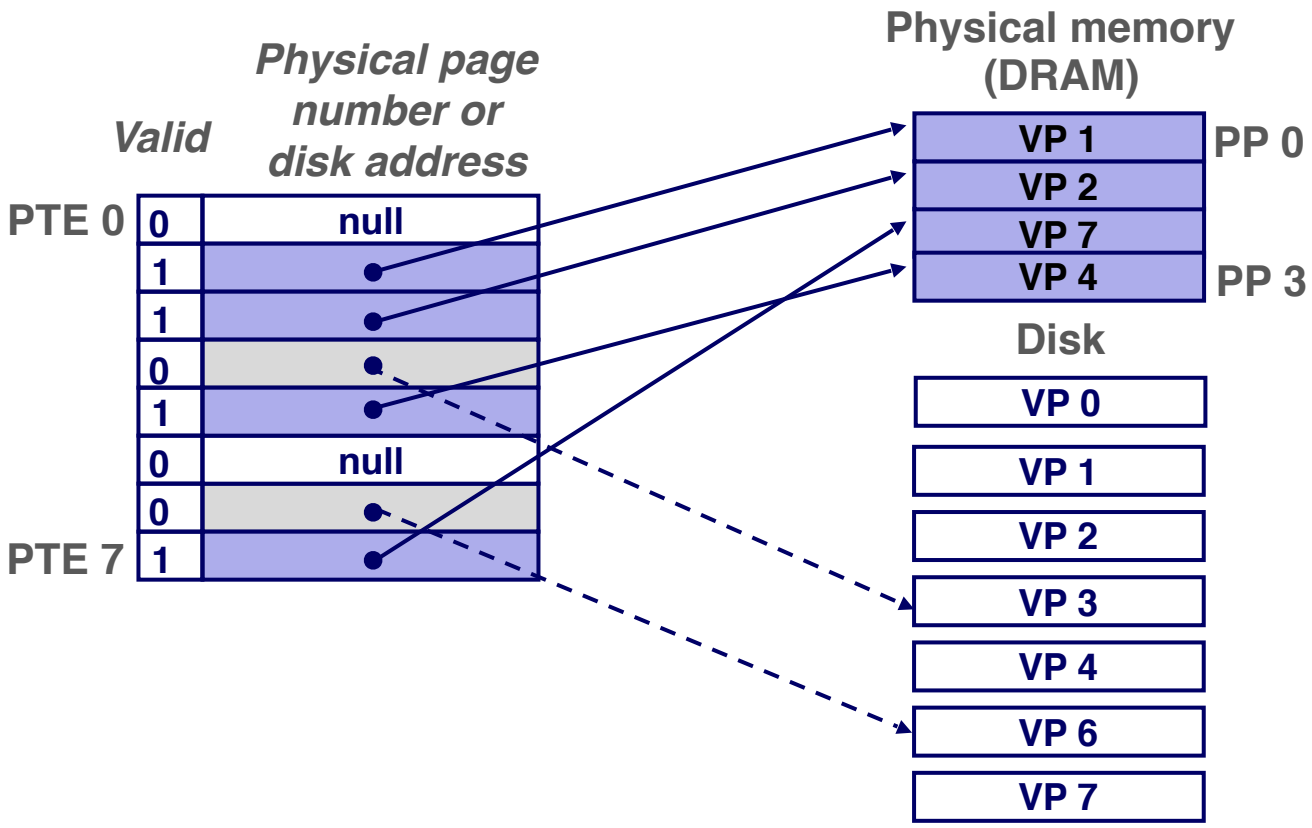
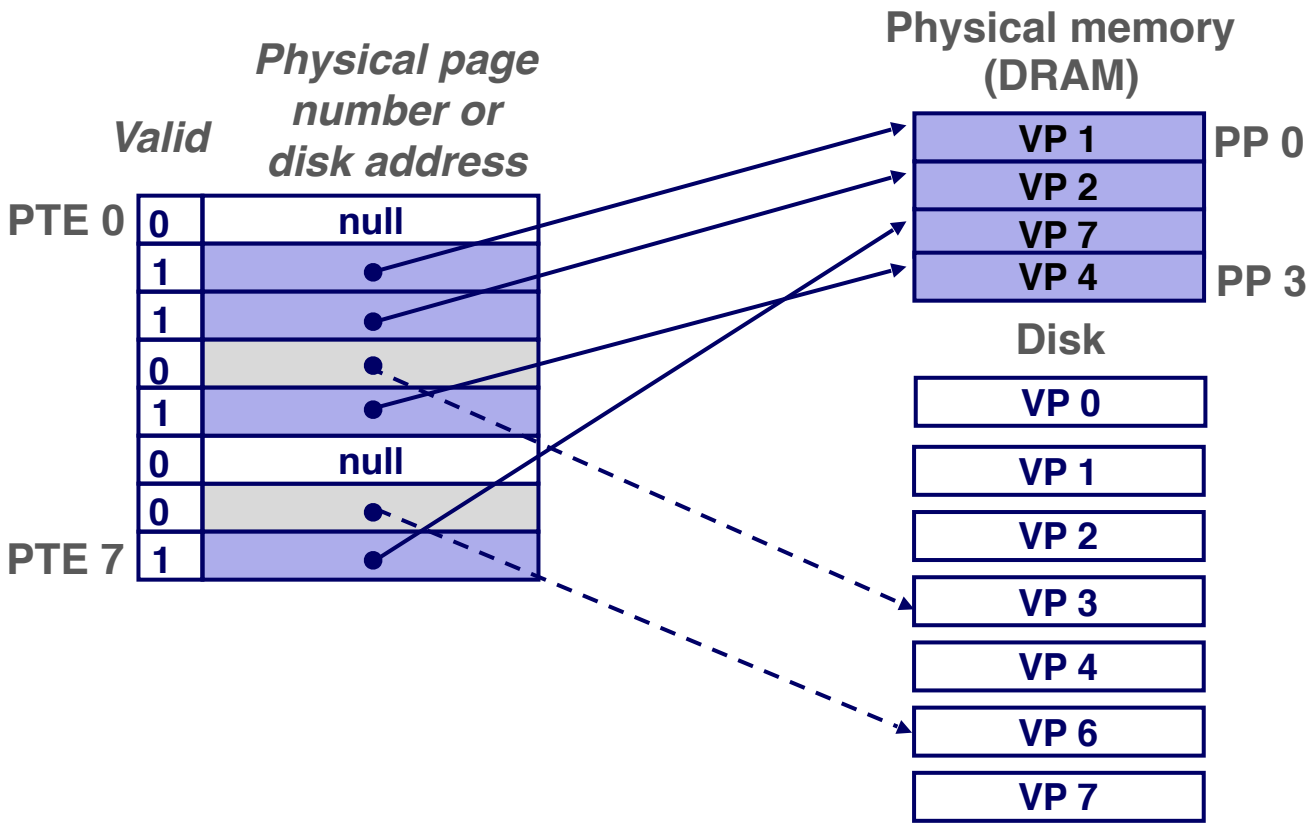
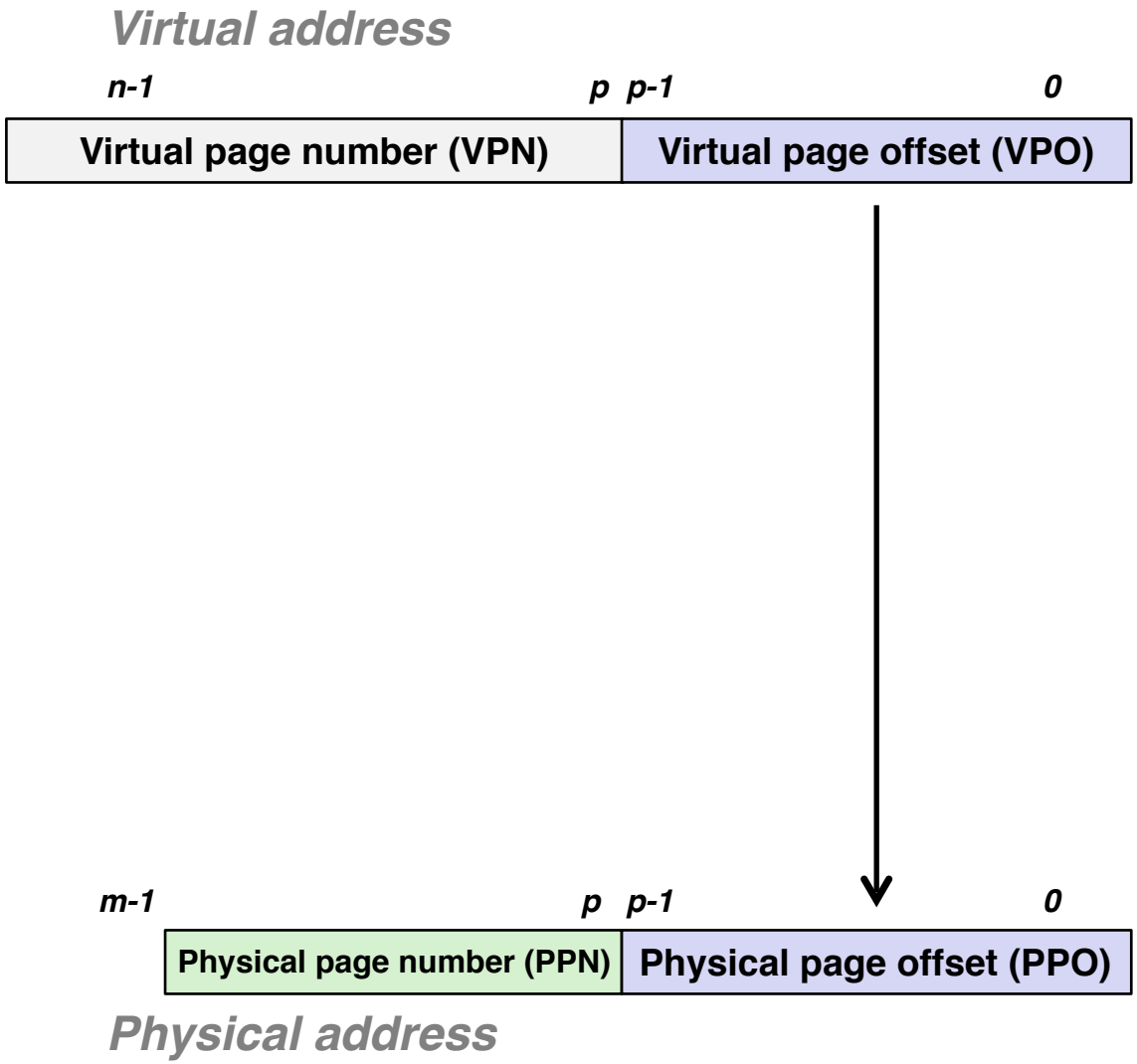


Page Table: Enabling VA to PA Translation

- A page table is an array of page table entries (PTEs) that maps every virtual page to its physical page.
- 64-bit machine, 4KB page size, how many PTEs?
  - Every virtual page has a PTE, so 2^{52} PTEs.



Address Translation With a Page Table



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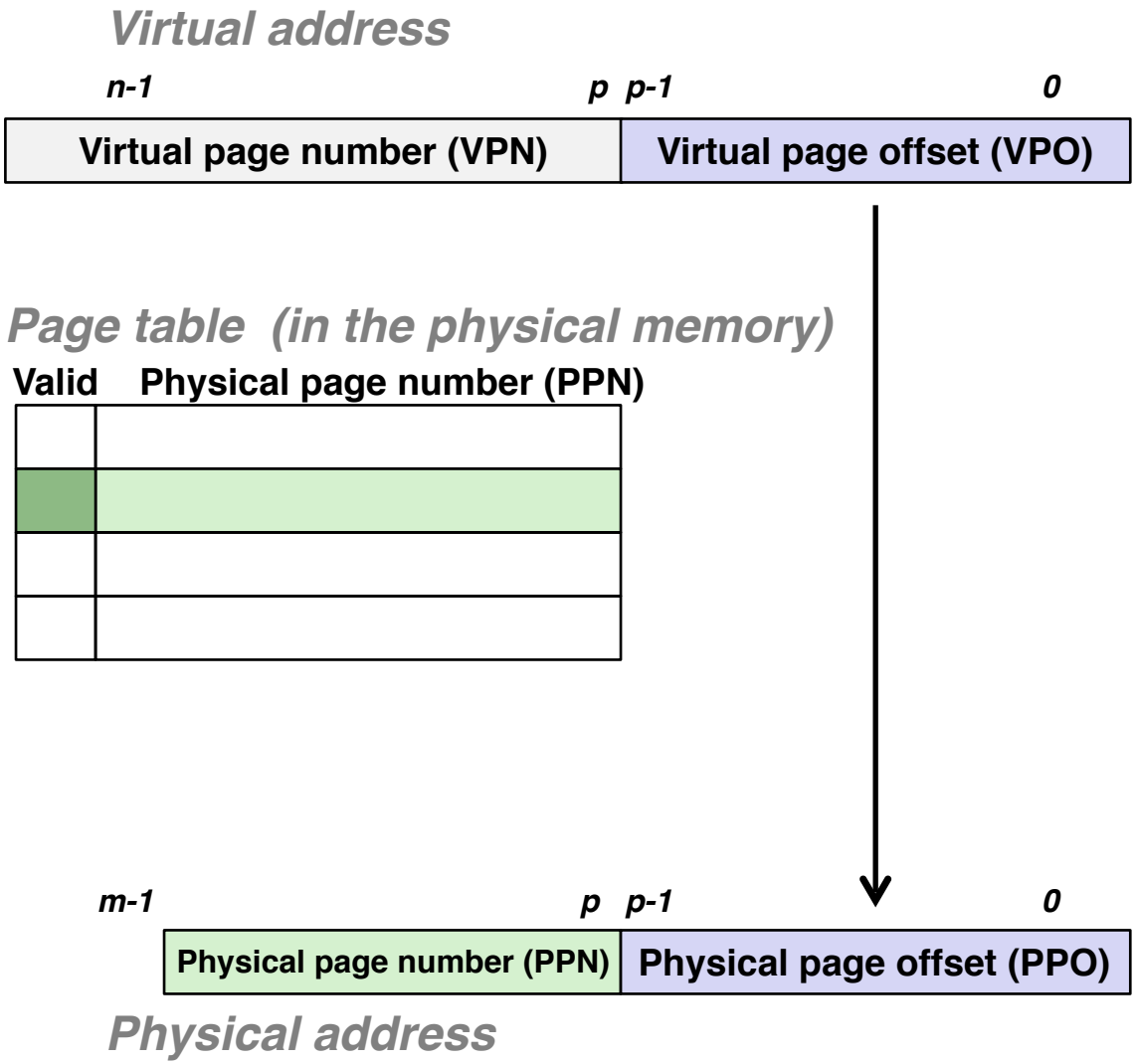

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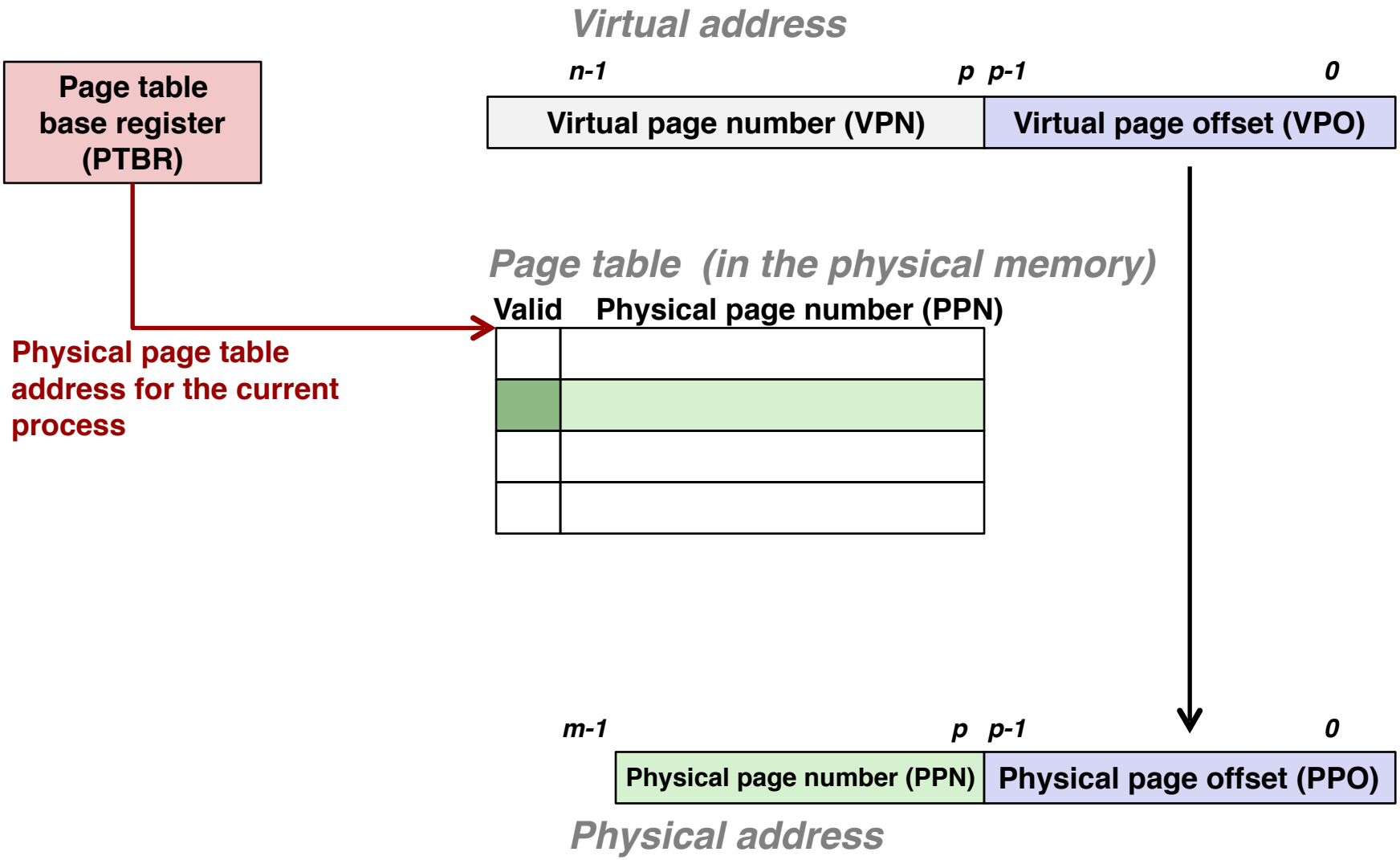

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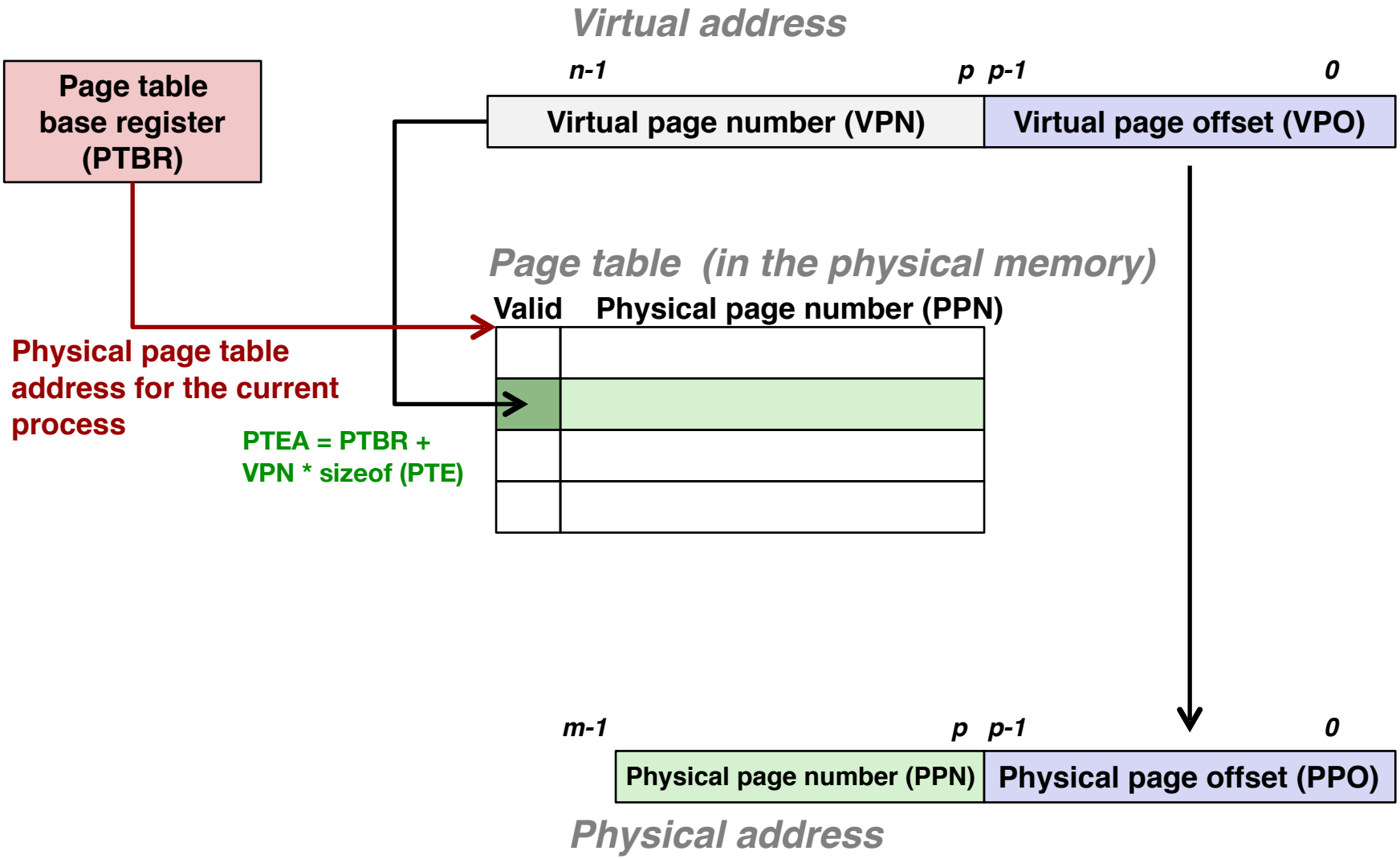

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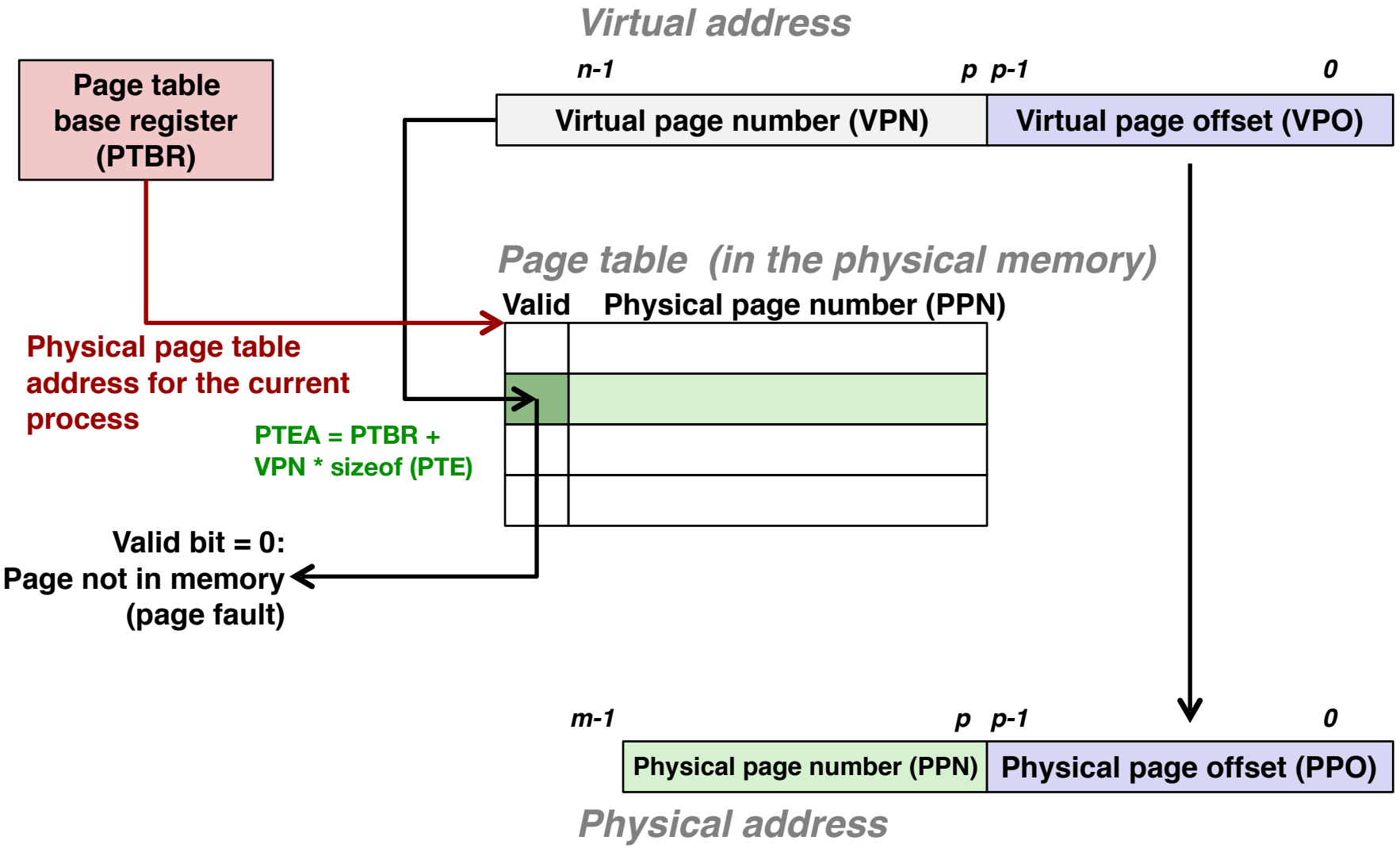

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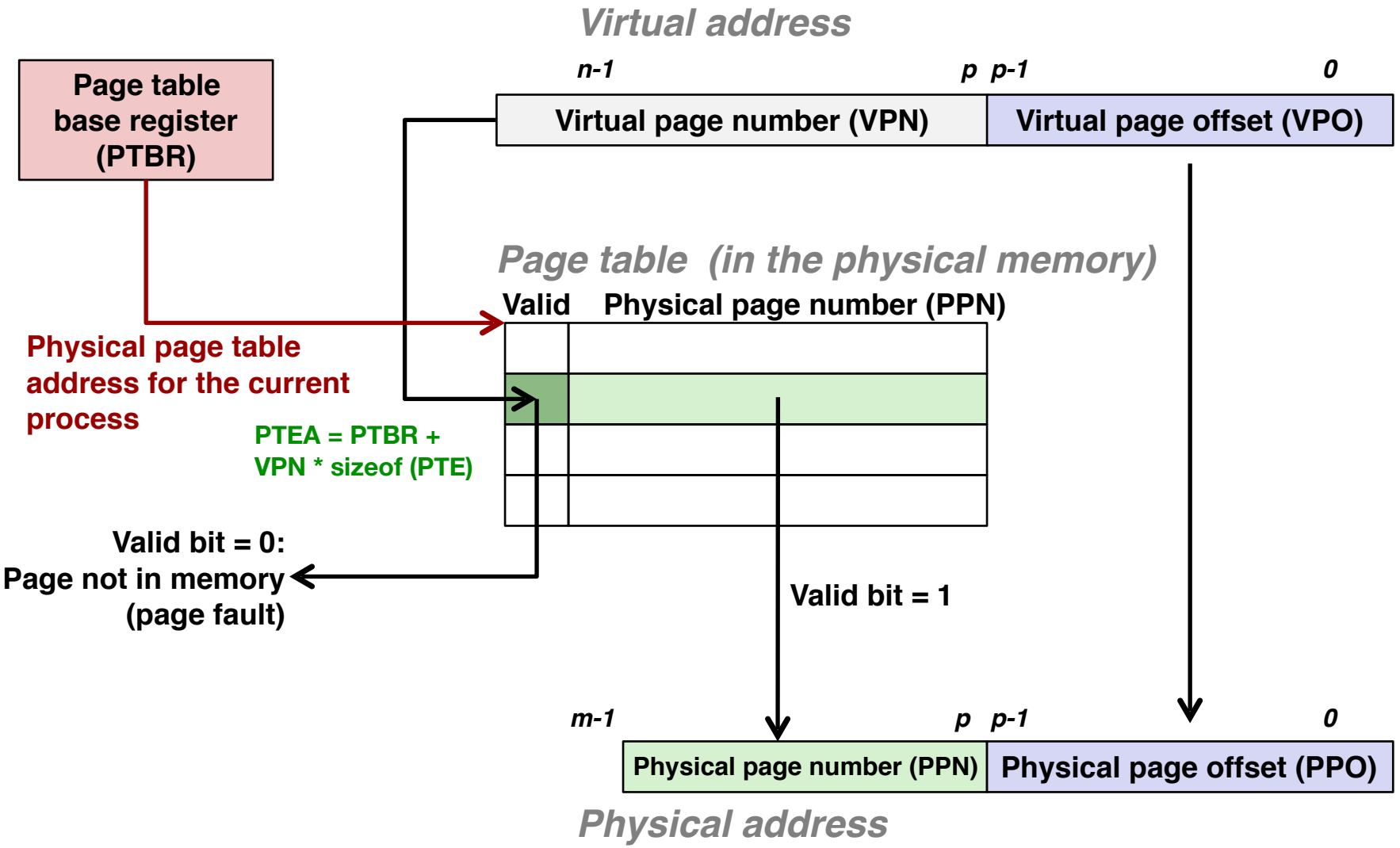
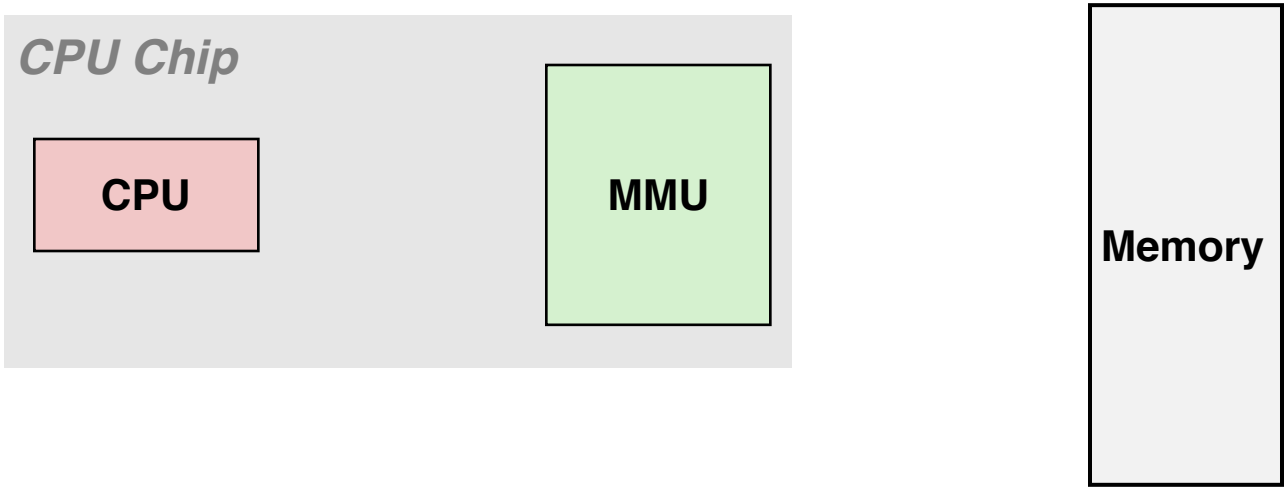


Address Translation: Page Hit



VA: virtual address, PA: physical address, PTE: page table entry, PTEA = PTE address

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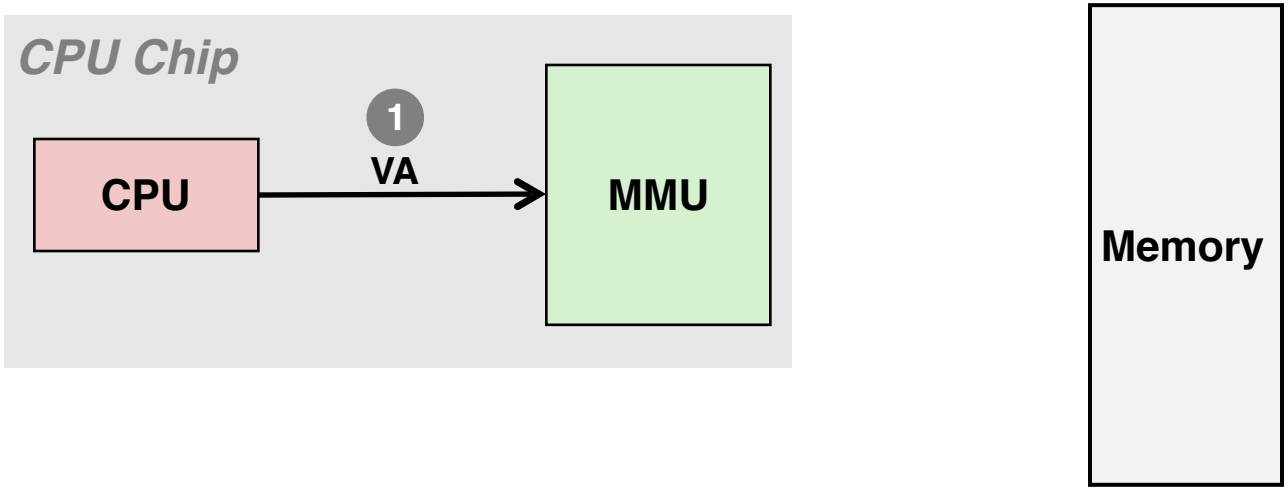

1) Processor sends virtual address to MMU

VA: virtual address, PA: physical address, PTE: page table entry, PTEA = PTE address

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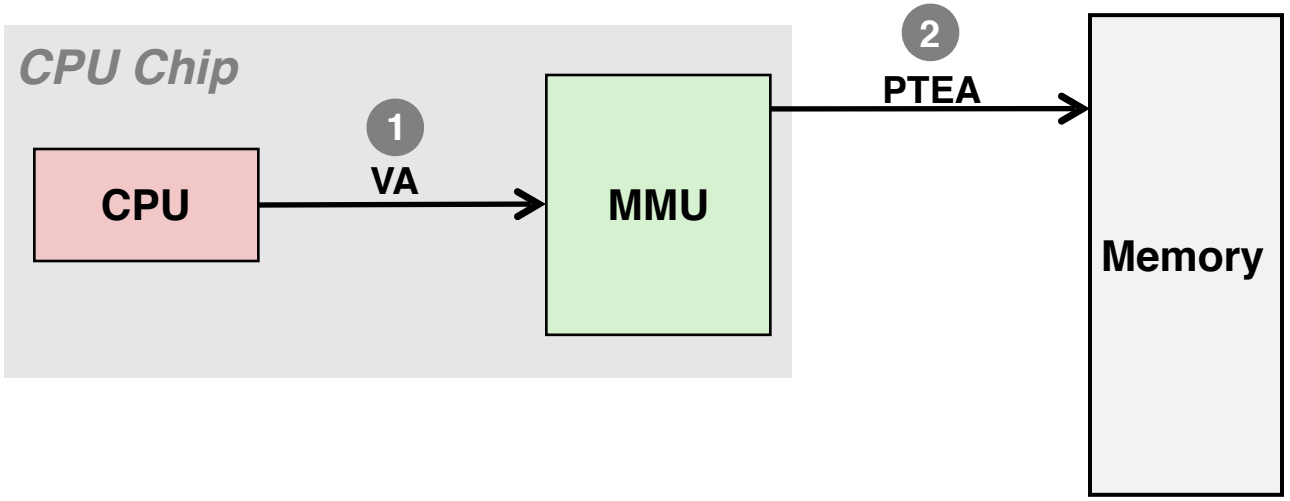

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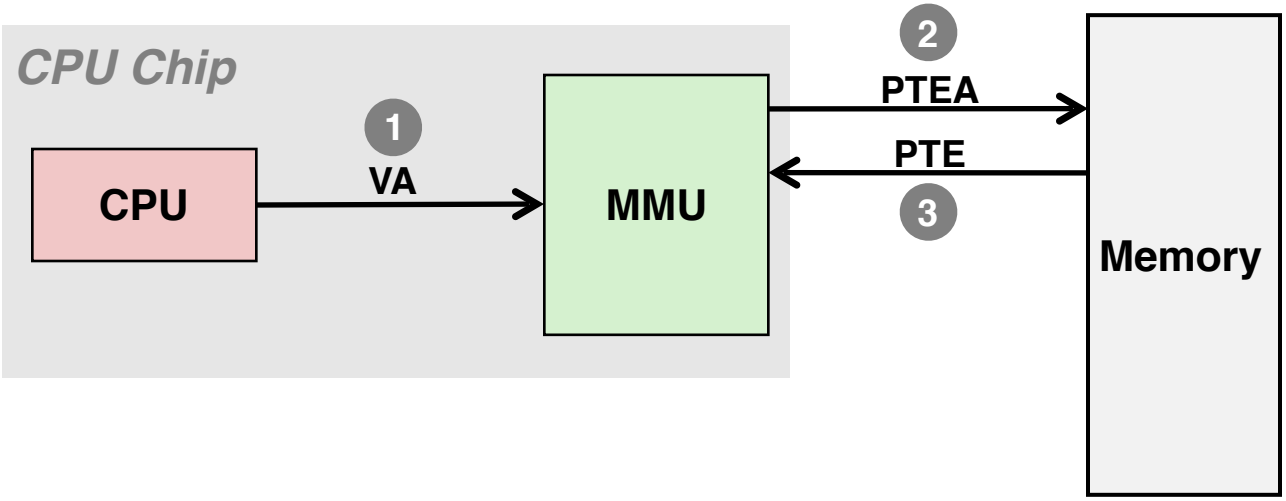

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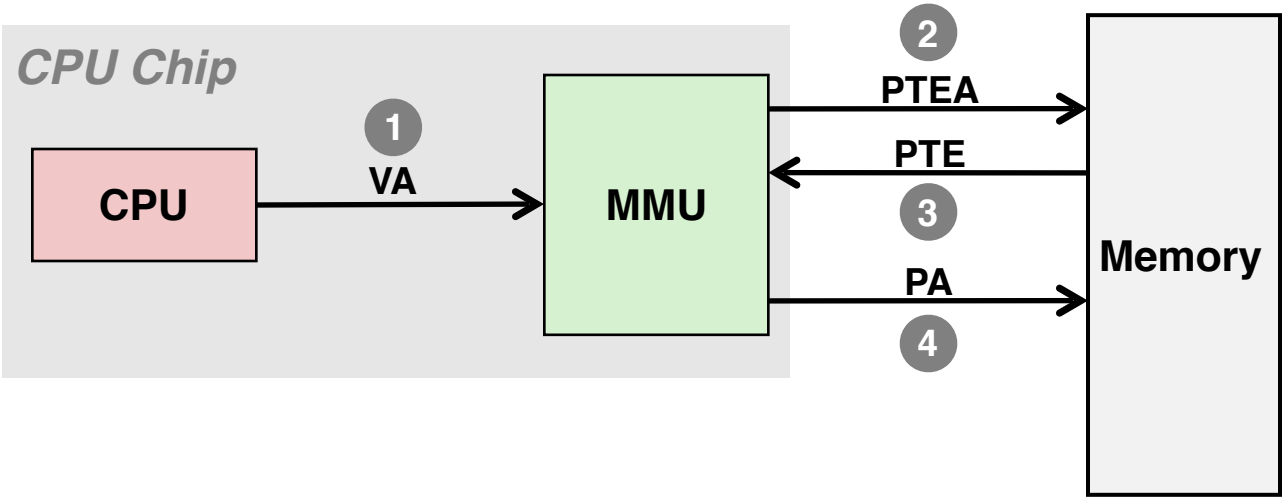

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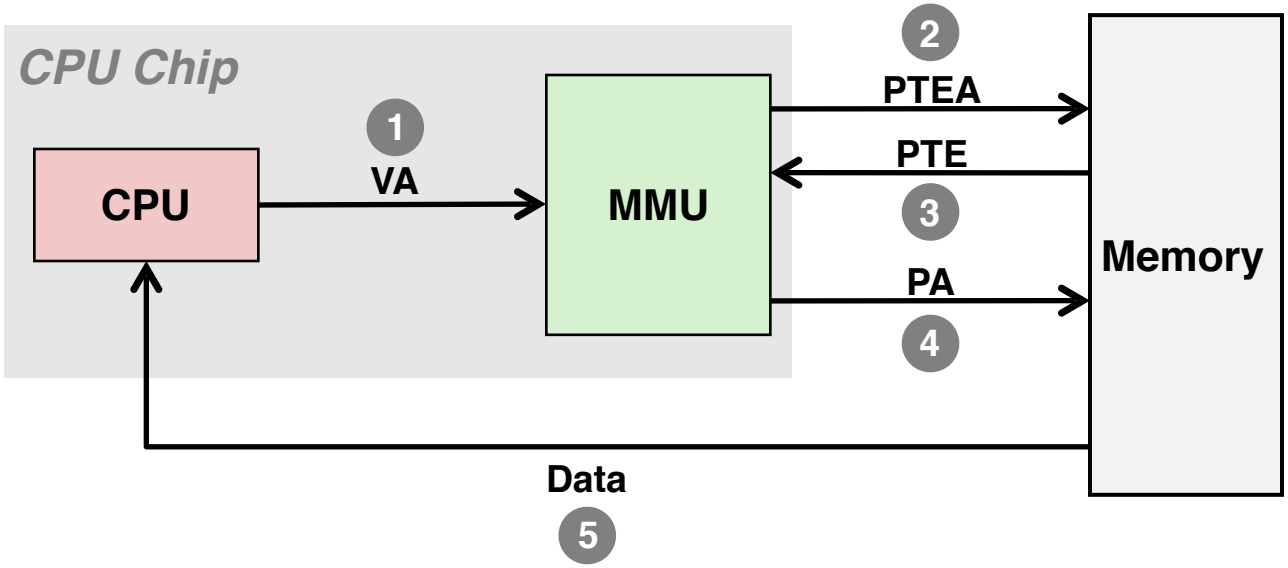

1) Processor sends virtual address to MMU

2-3) MMU fetches PTE from page table in memory

4) MMU sends physical address to cache/memory

5) Cache/memory sends data word to processor

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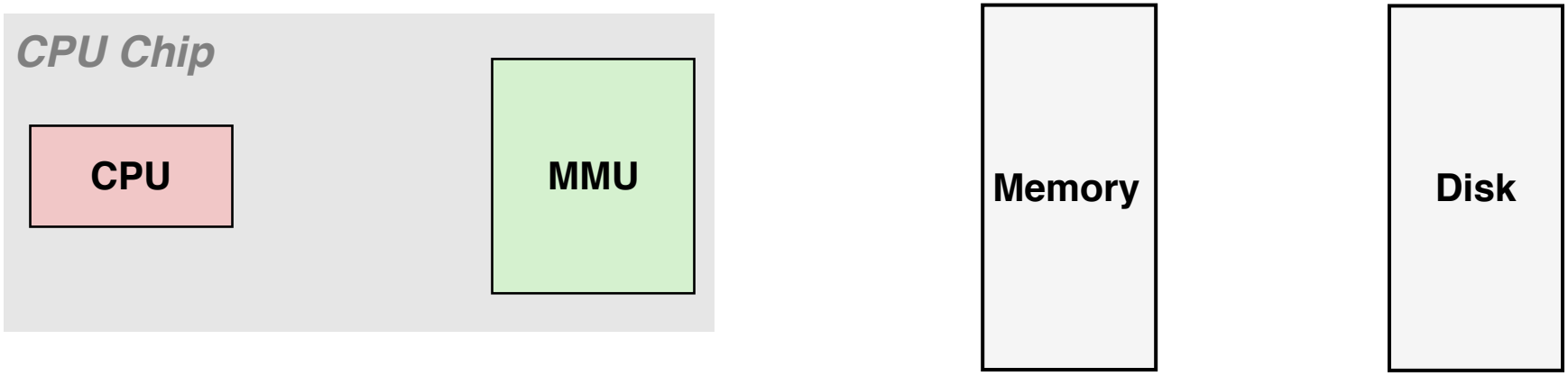

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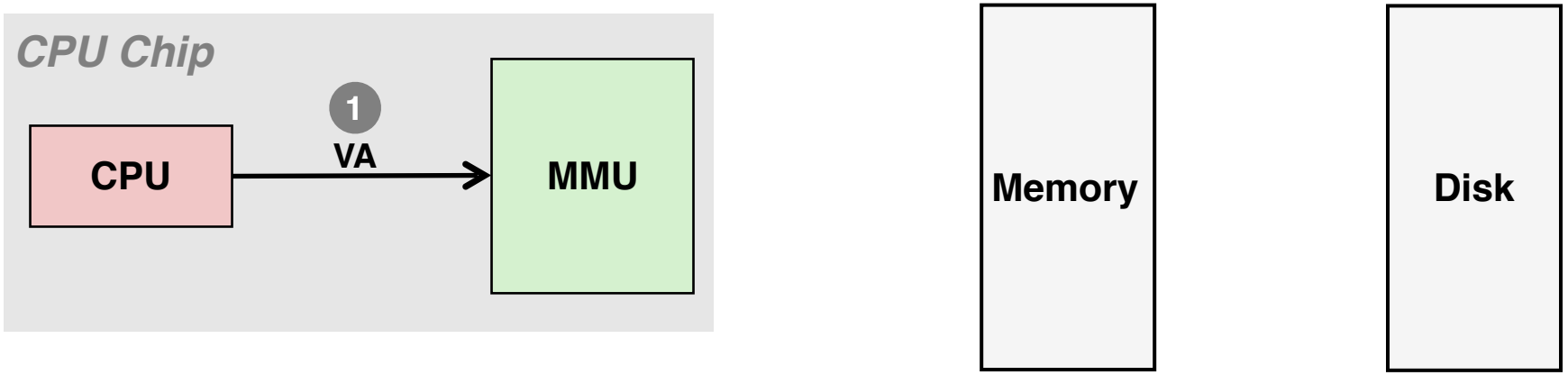

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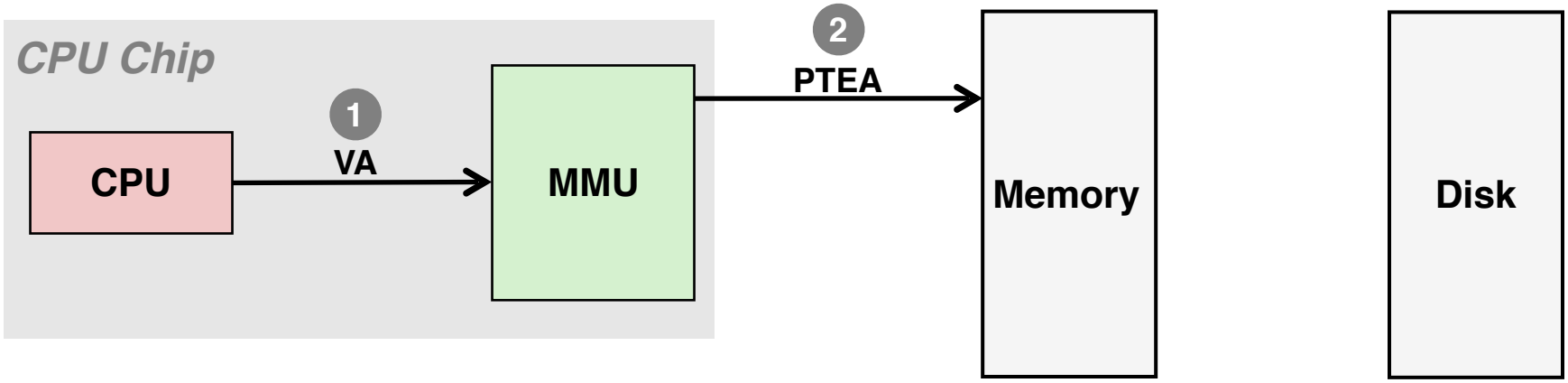

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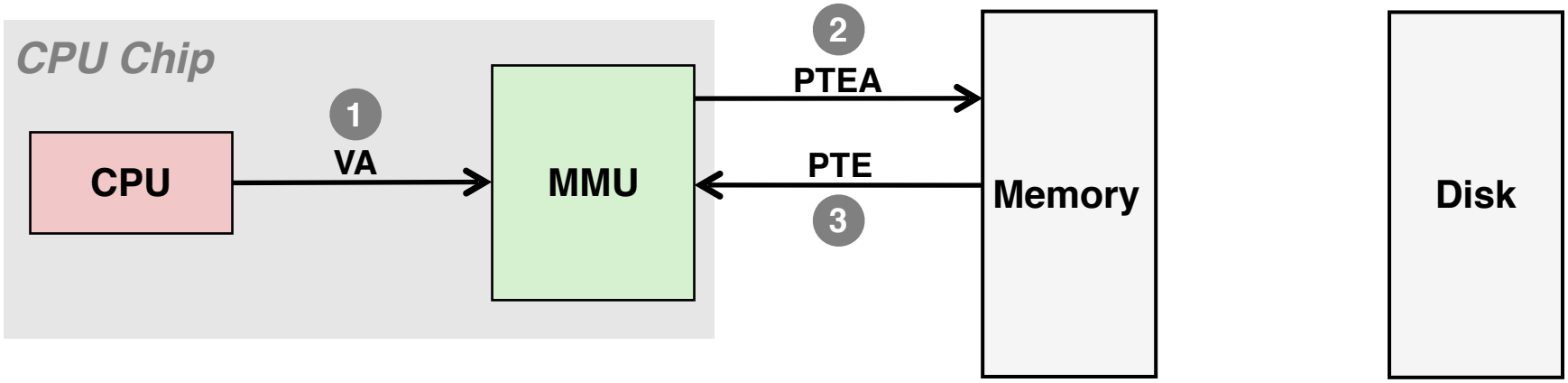

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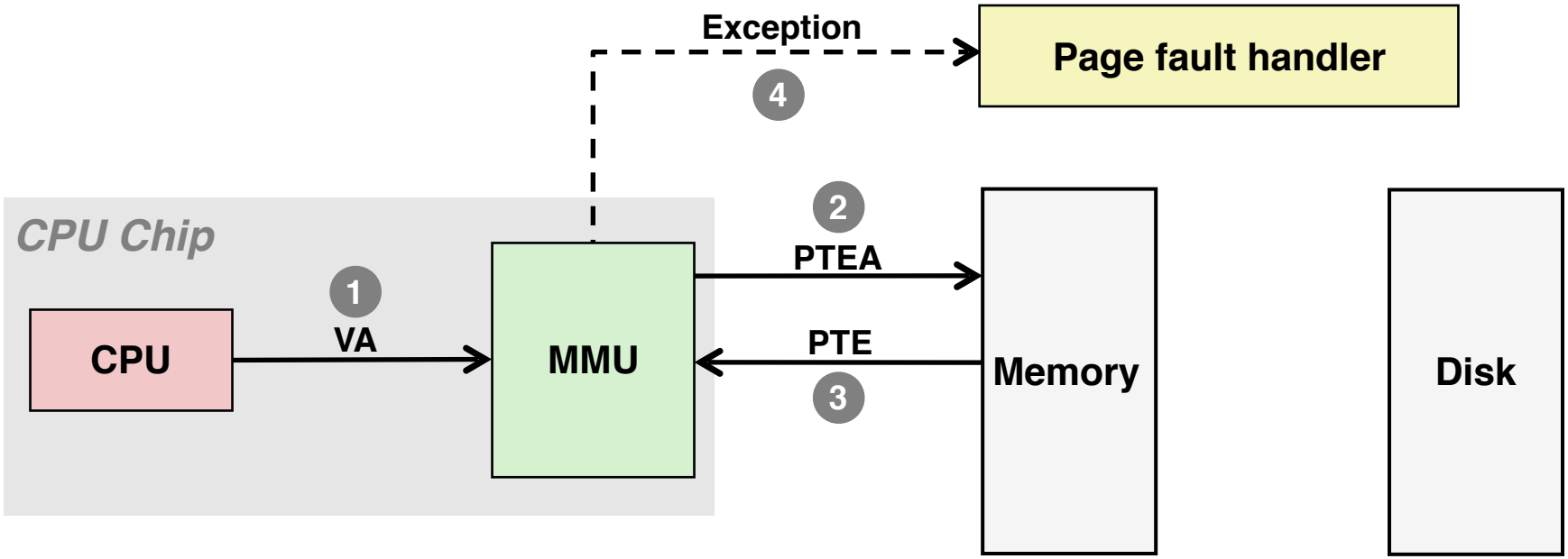

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4) Valid bit is zero, so MMU triggers page fault exception

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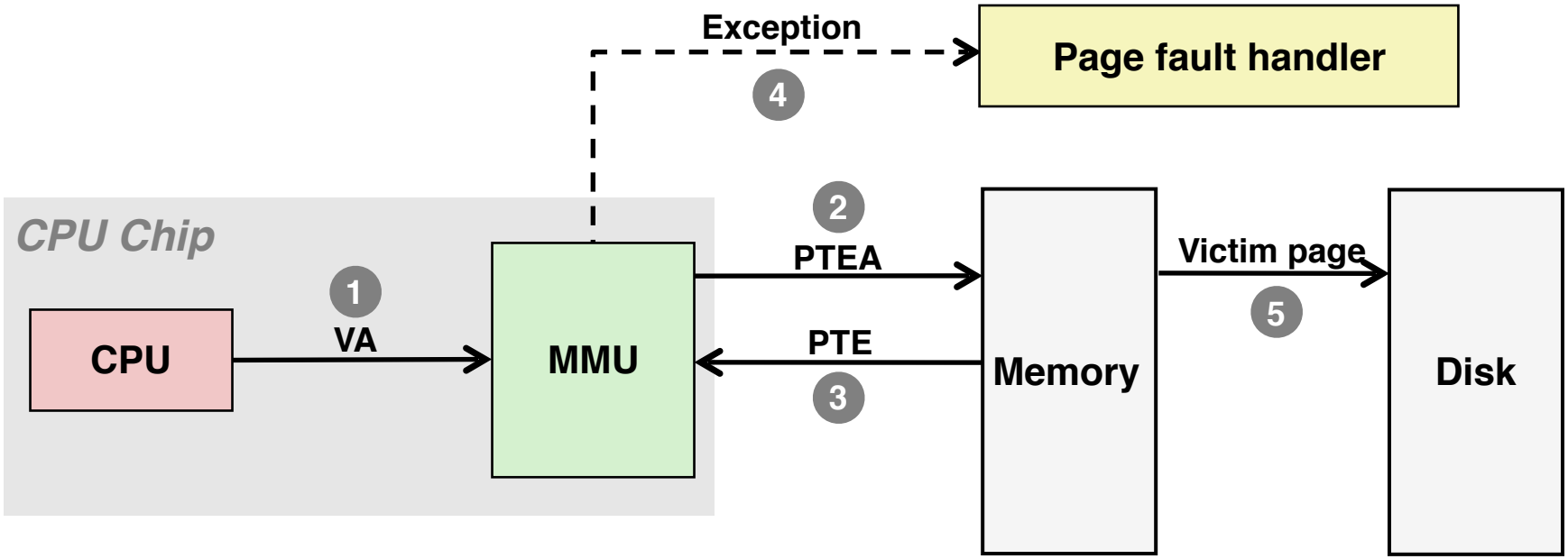

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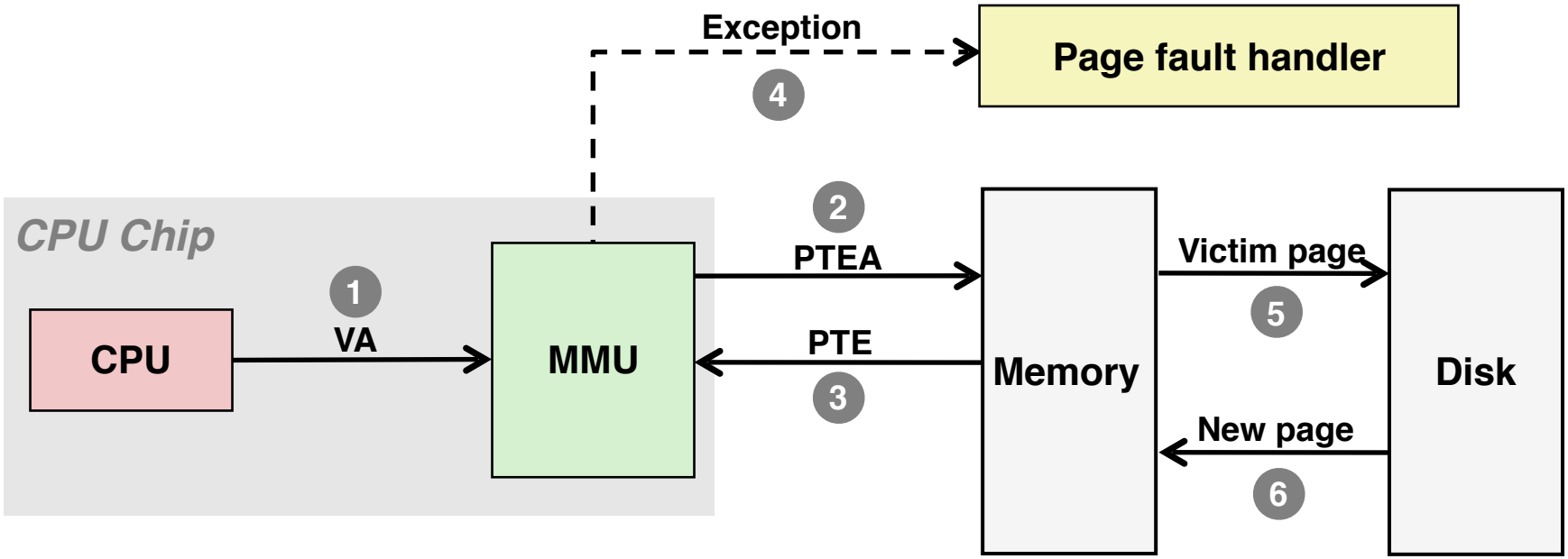

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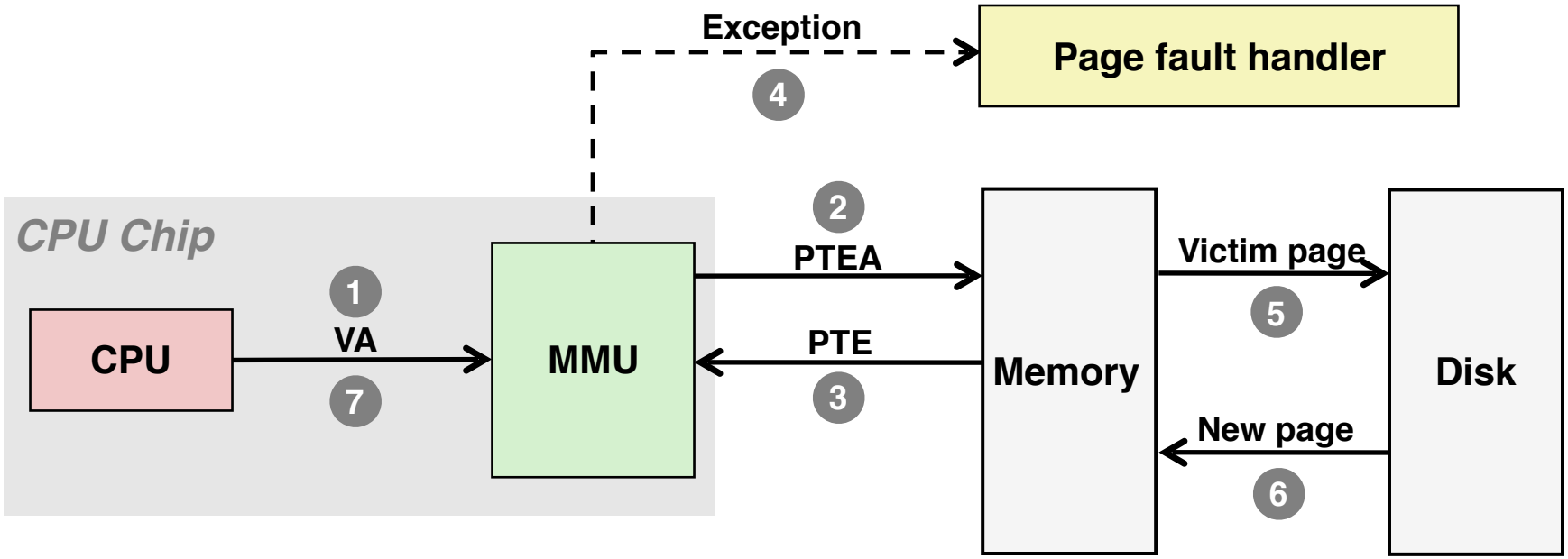

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7) Handler returns to original process, restarting faulting instruction

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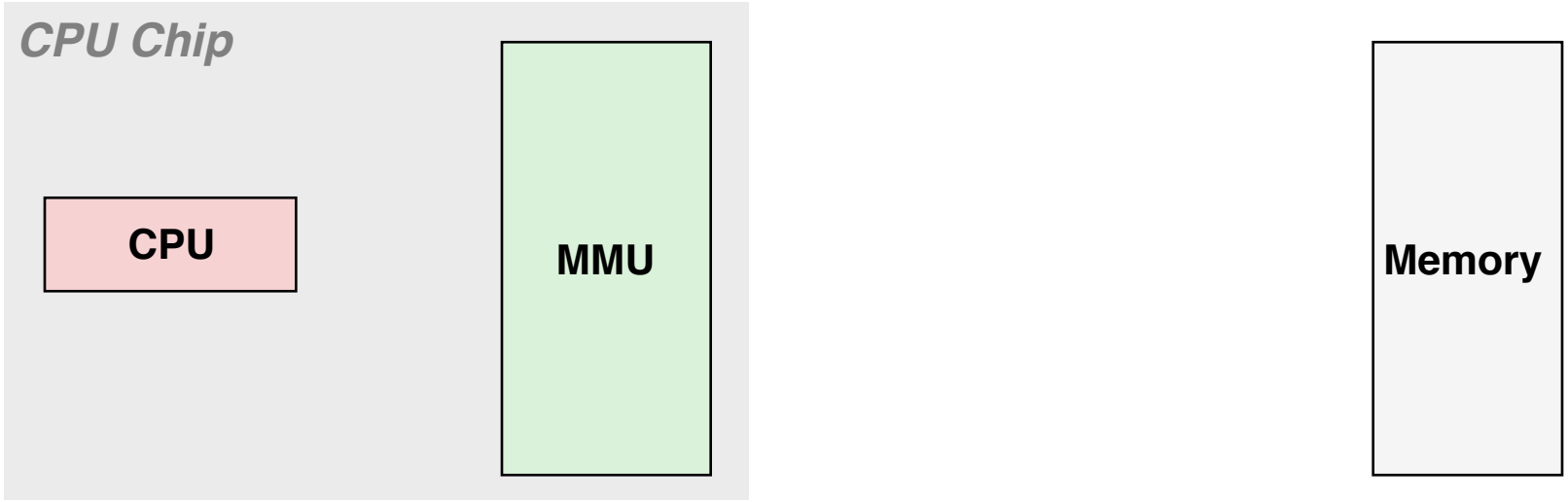
Integrating VM and Cache



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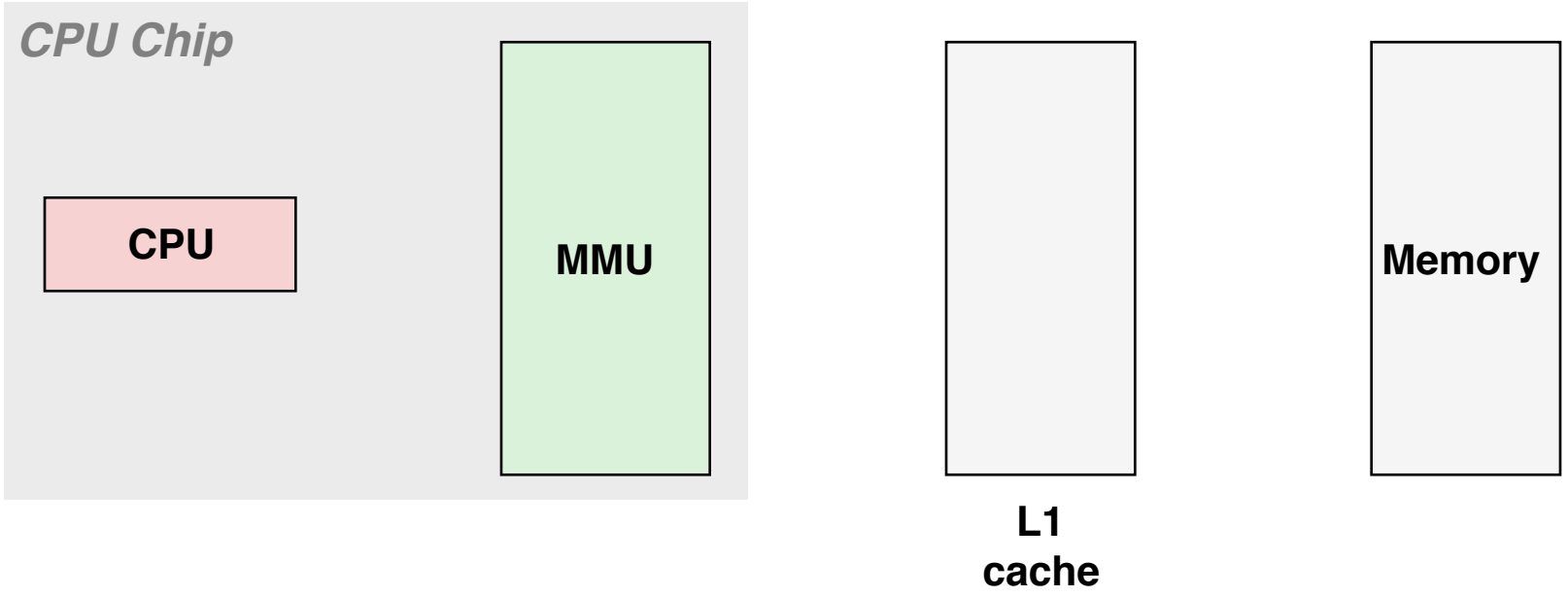

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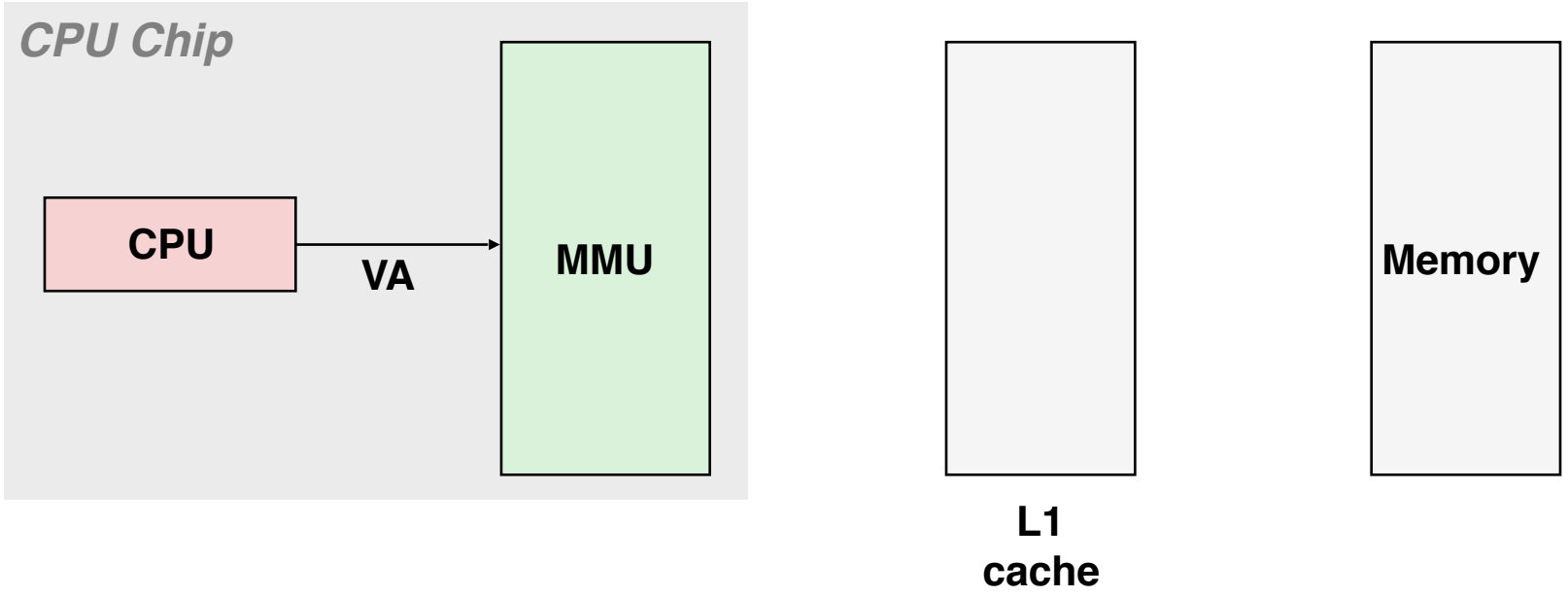

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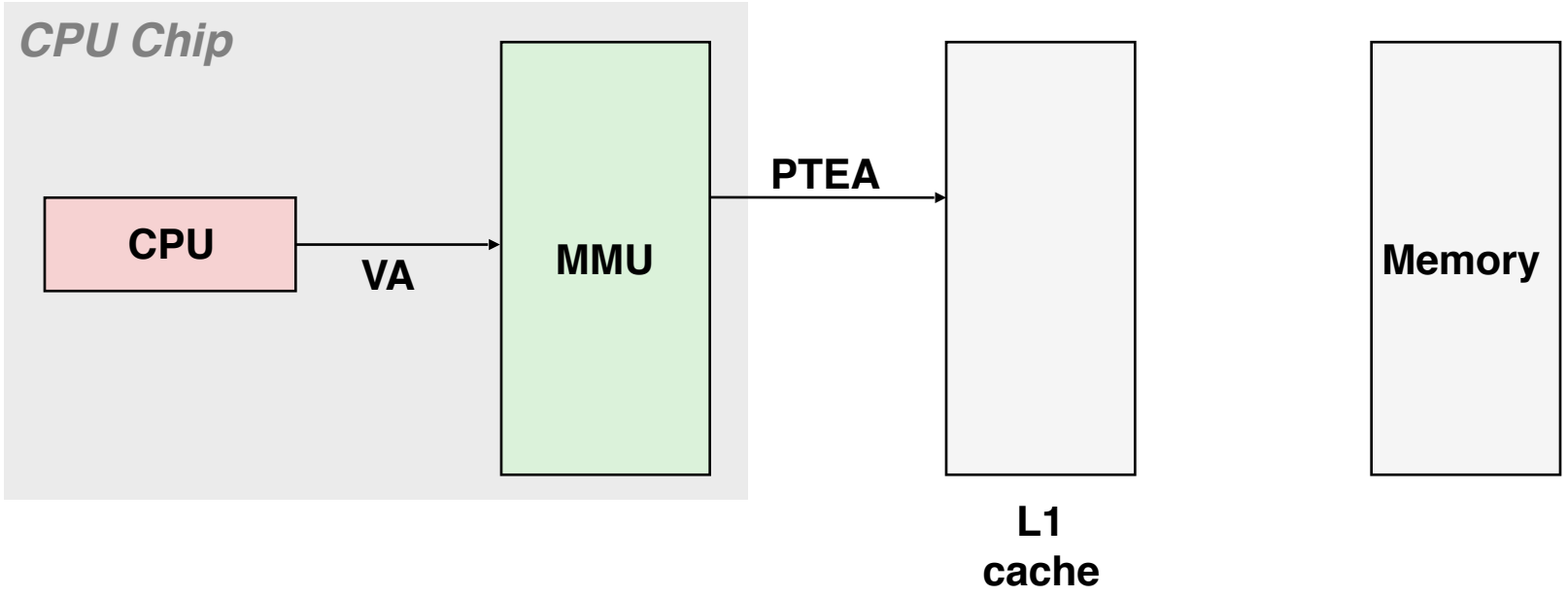

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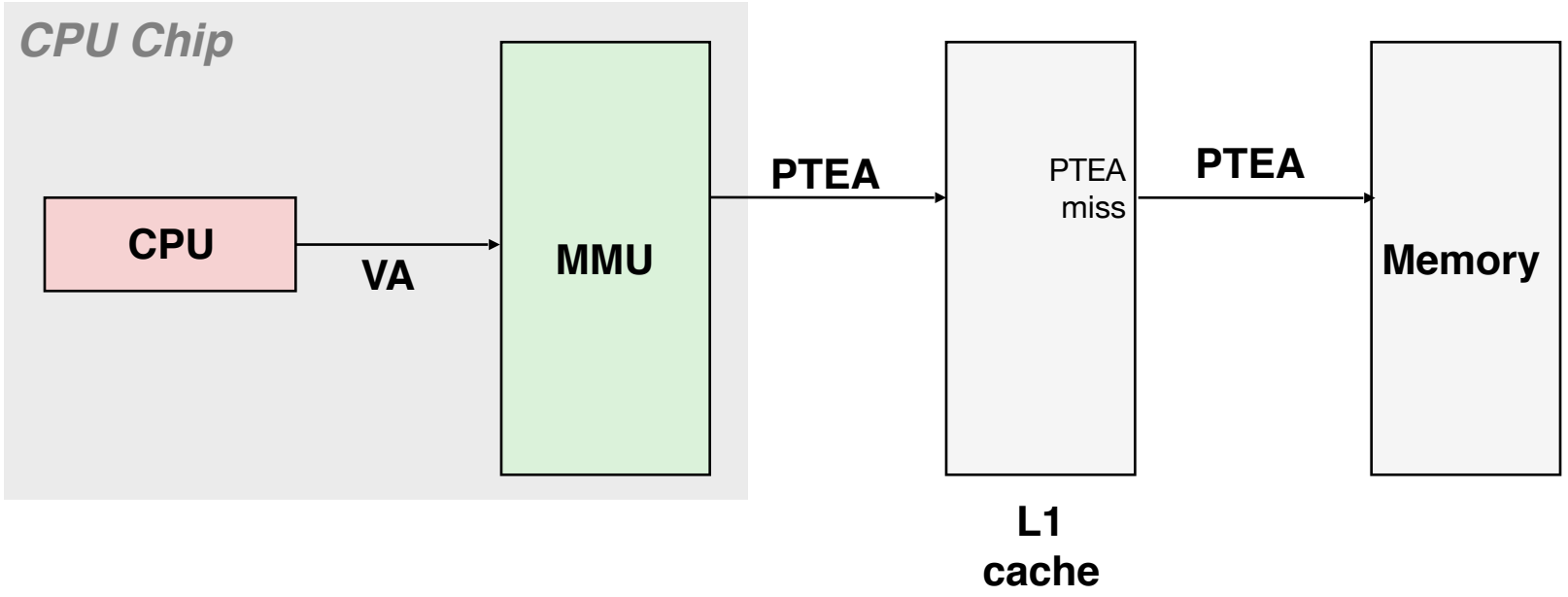

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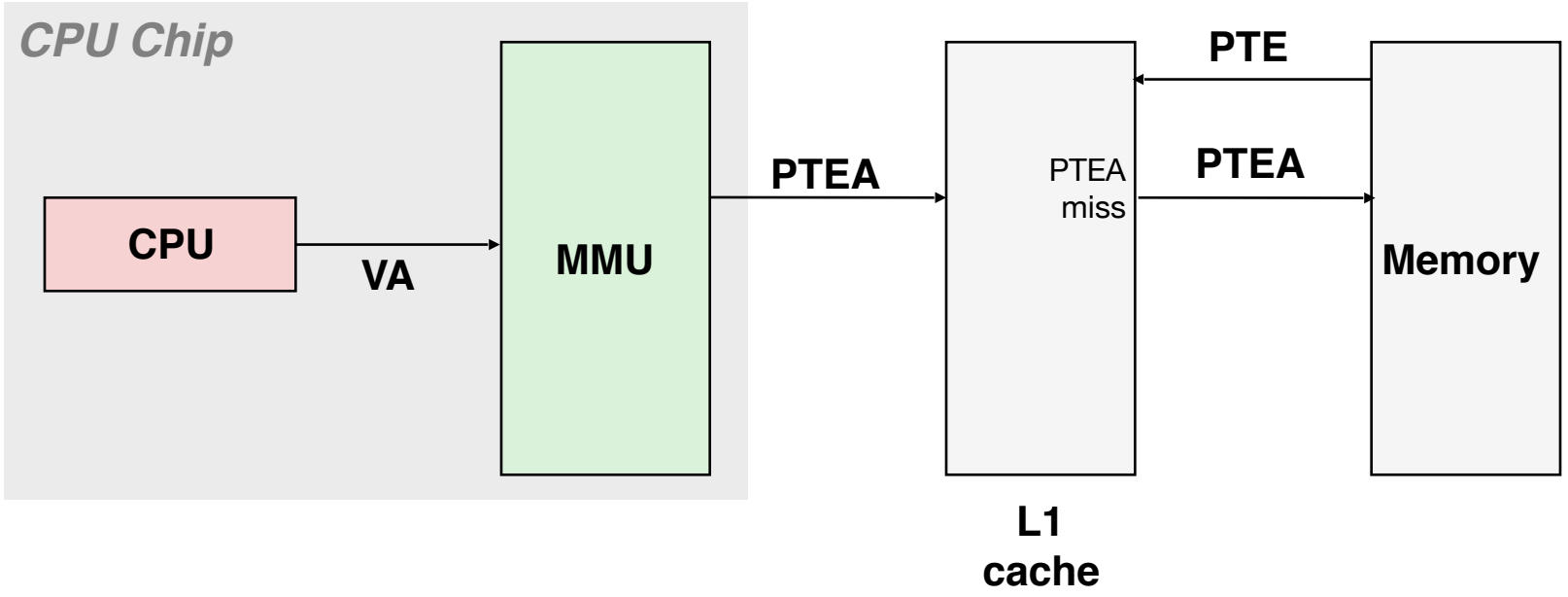

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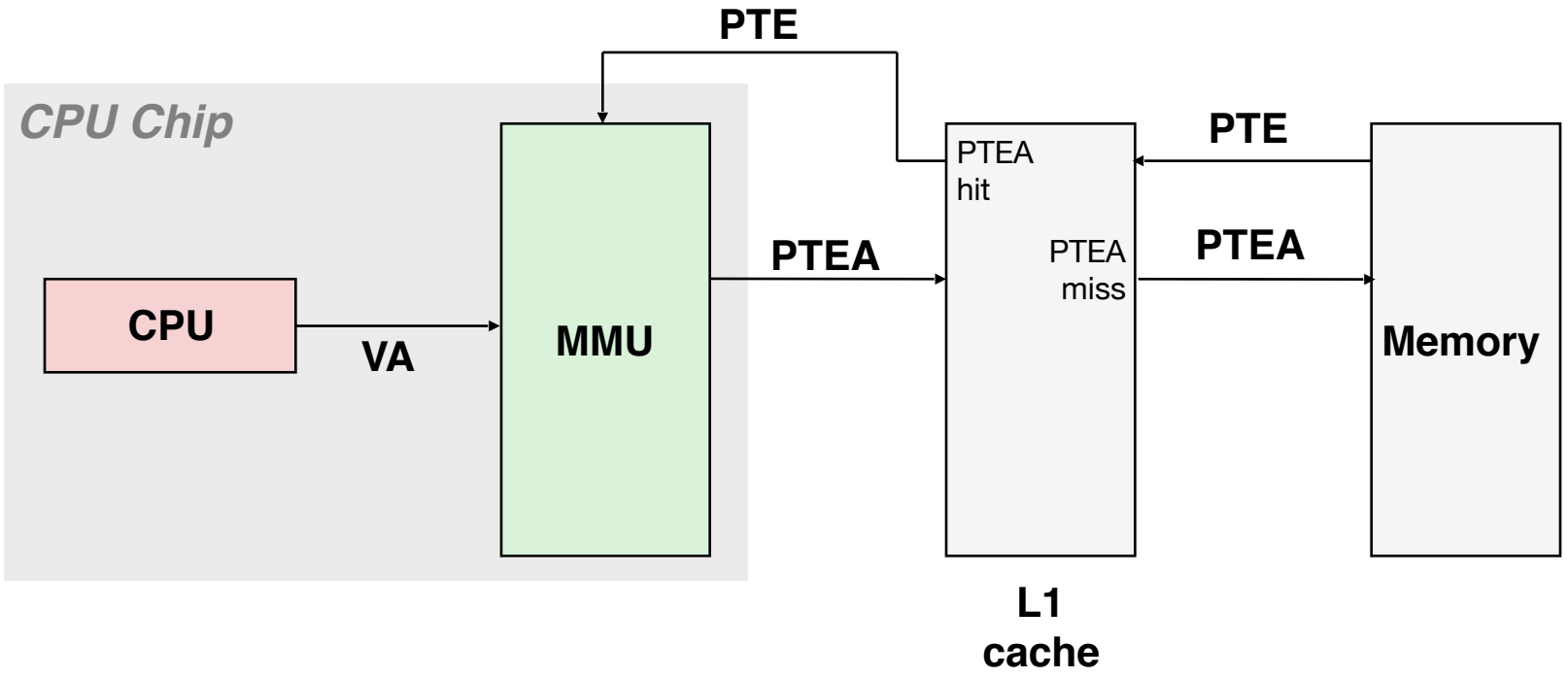

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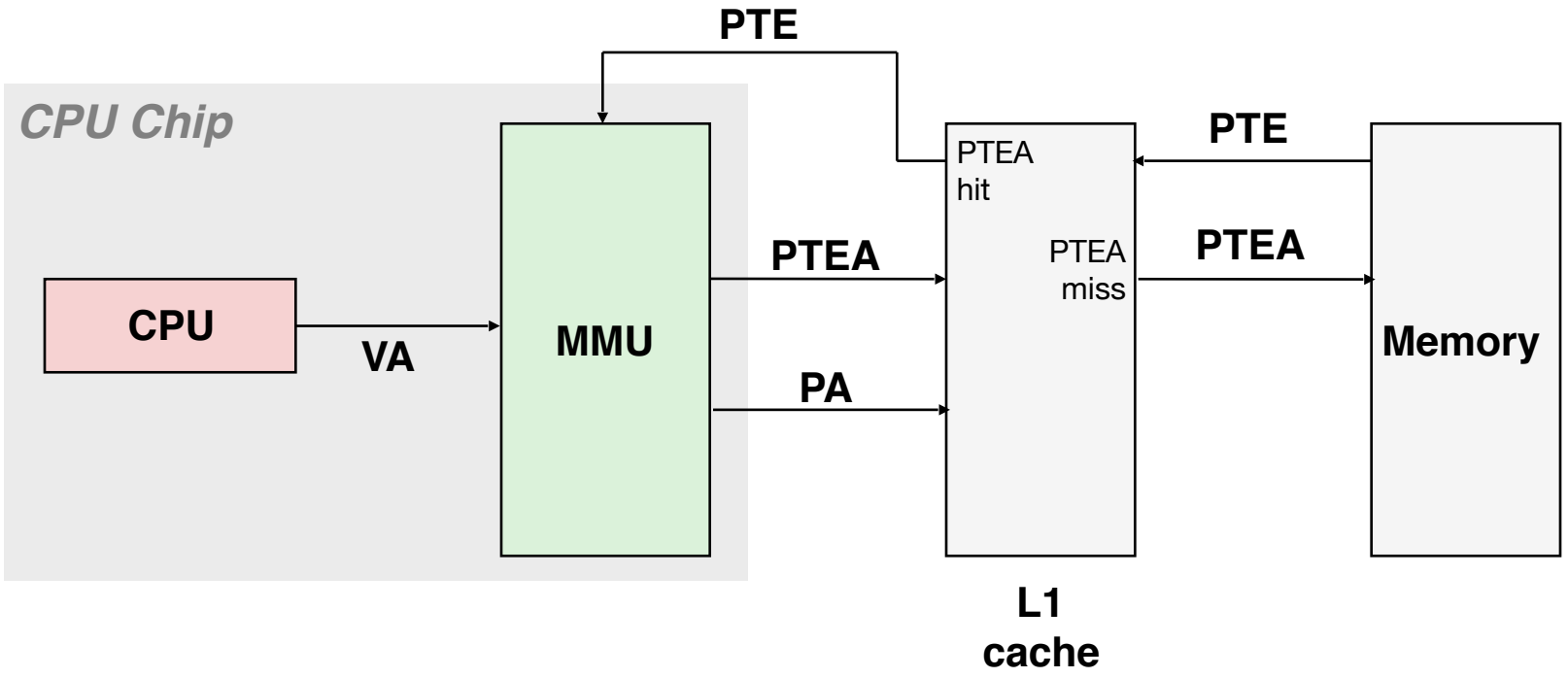

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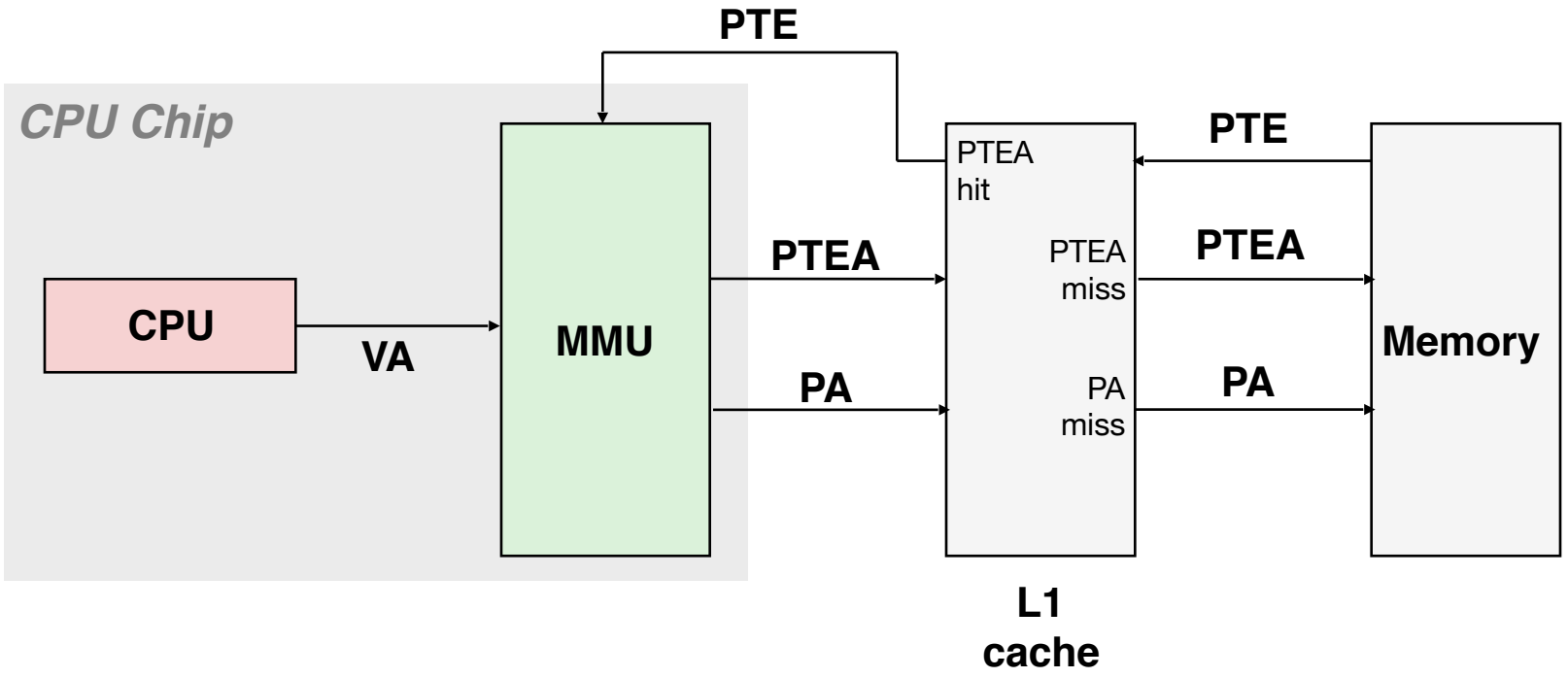

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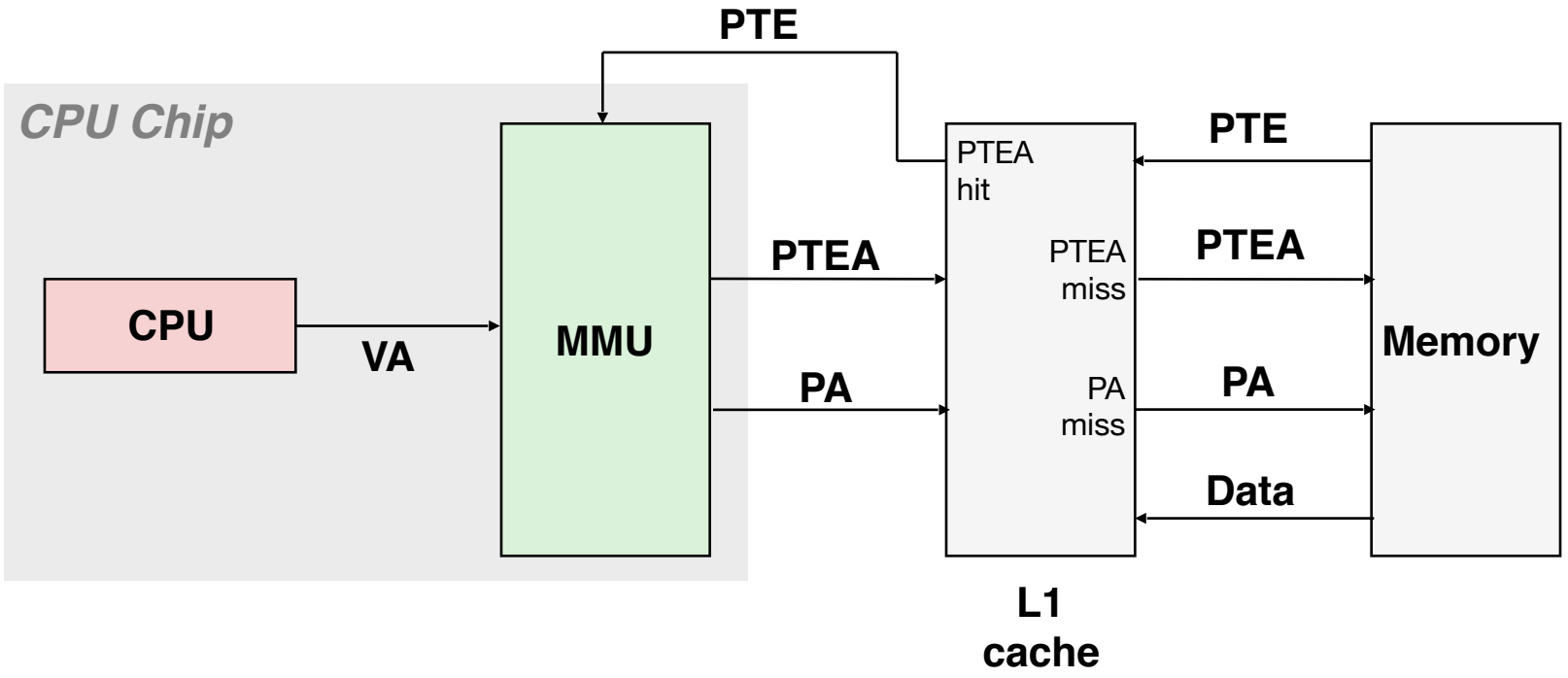

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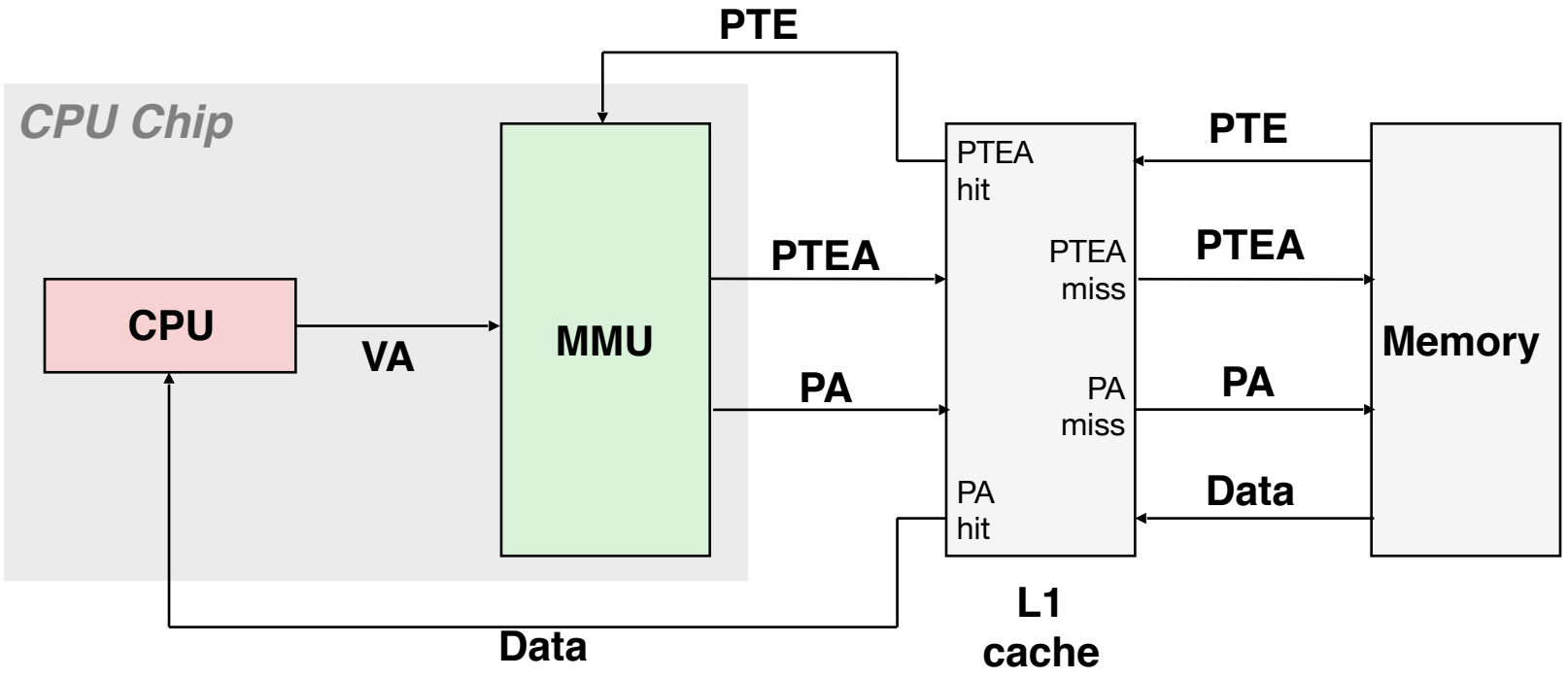

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Today

- Three Virtual Memory Optimizations
  - TLB
  - Page the page table (a.k.a., multi-level page table)
  - Virtually-indexed, physically-tagged cache
- Case-study: Intel Core i7/Linux example

Speeding up Address Translation

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- Problem: Every memory load/store requires two memory accesses: one for PTE, another for real
  - The PTE access is kind of an overhead
  - Can we speed it up?

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  - The PTE access is kind of an overhead
  - Can we speed it up?
- Page table entries (PTEs) are already cached in L1 data cache like any other memory data. But:
  - PTEs may be evicted by other data references
  - PTE hit still requires a small L1 delay

Speeding up Translation with a TLB

- Solution: *Translation Lookaside Buffer* (TLB)
  - Think of it as a dedicated cache for page table
  - Small set-associative hardware cache in MMU
  - Contains complete page table entries for a small number of pages

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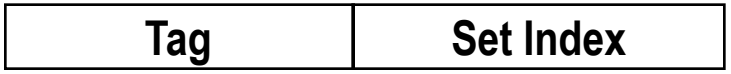

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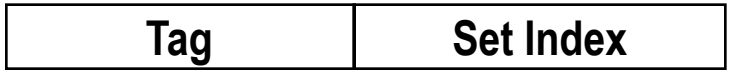

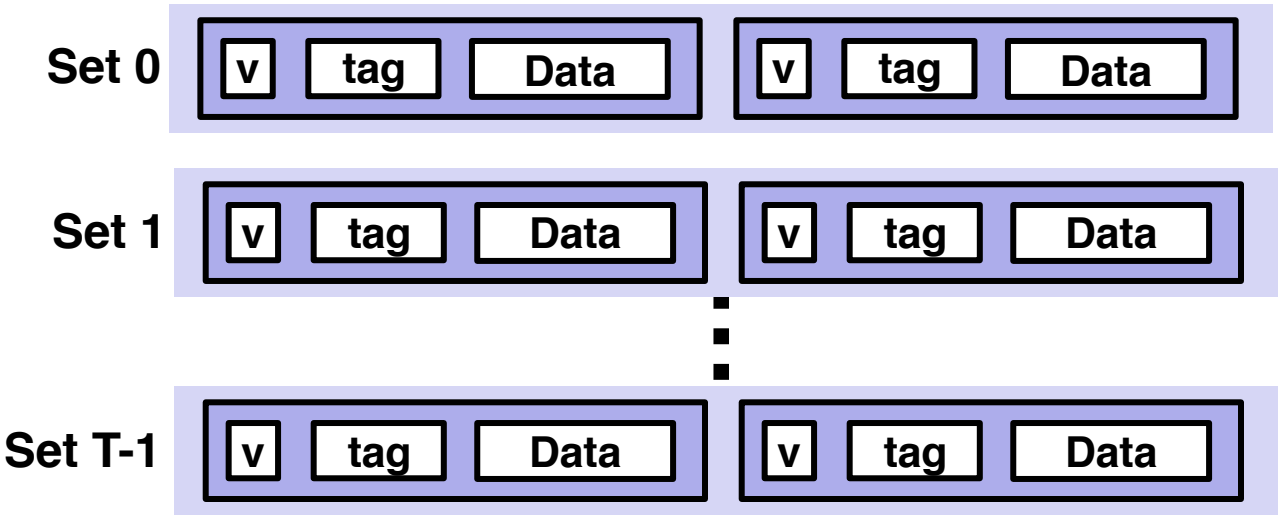

A Conventional Data Cache

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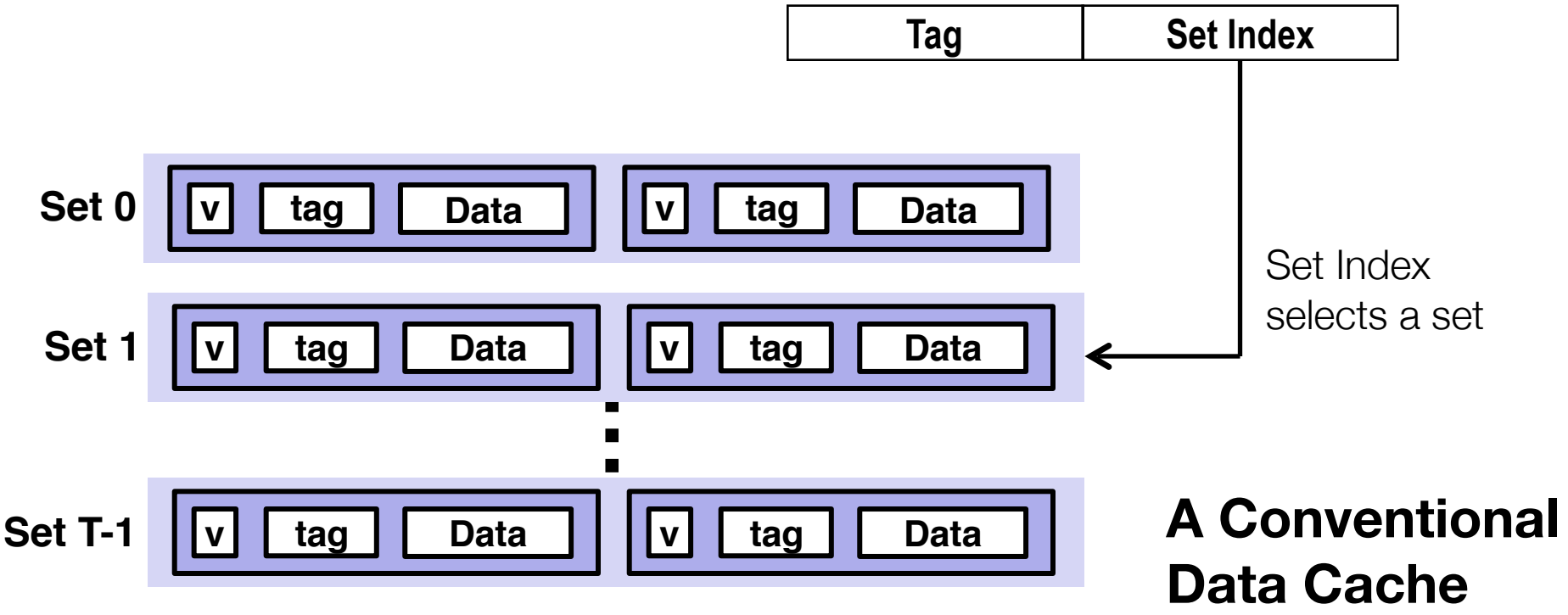

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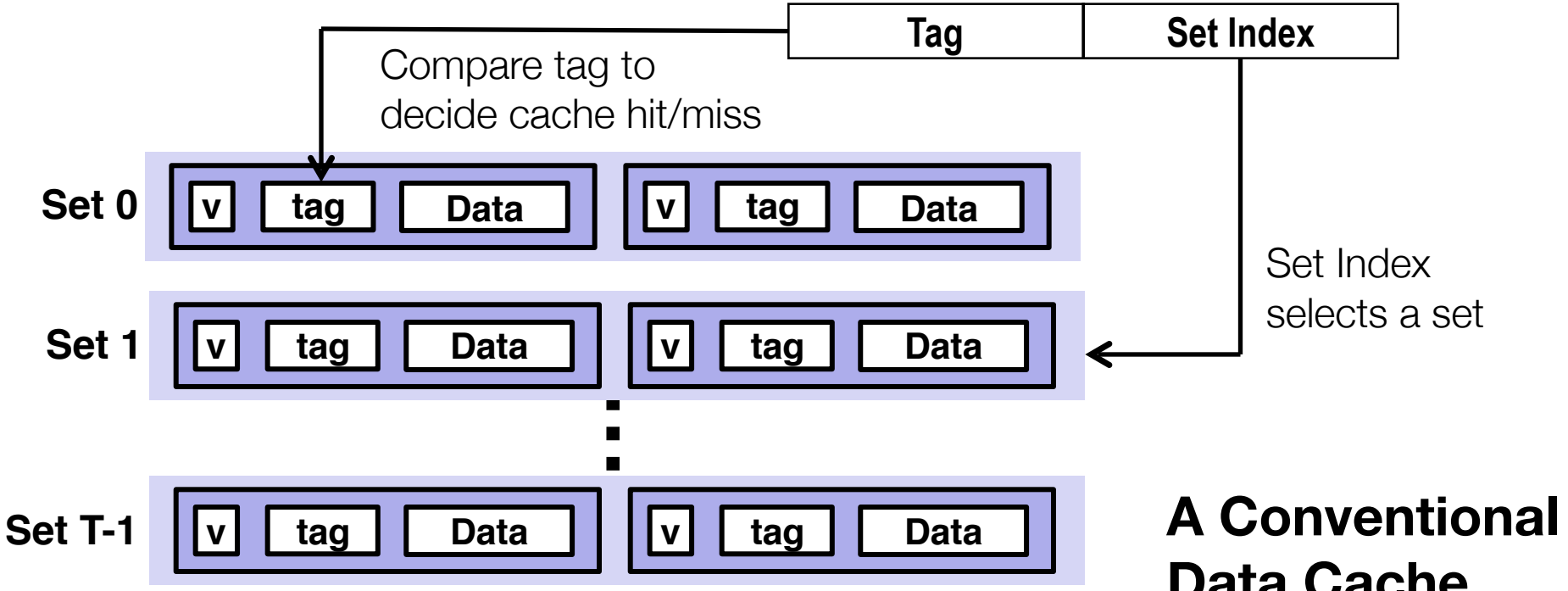

Accessing the TLB

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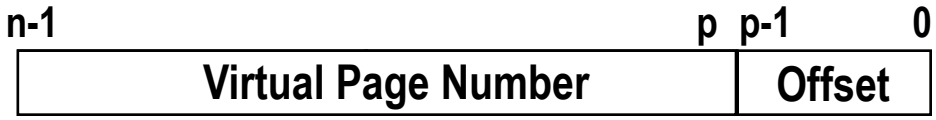

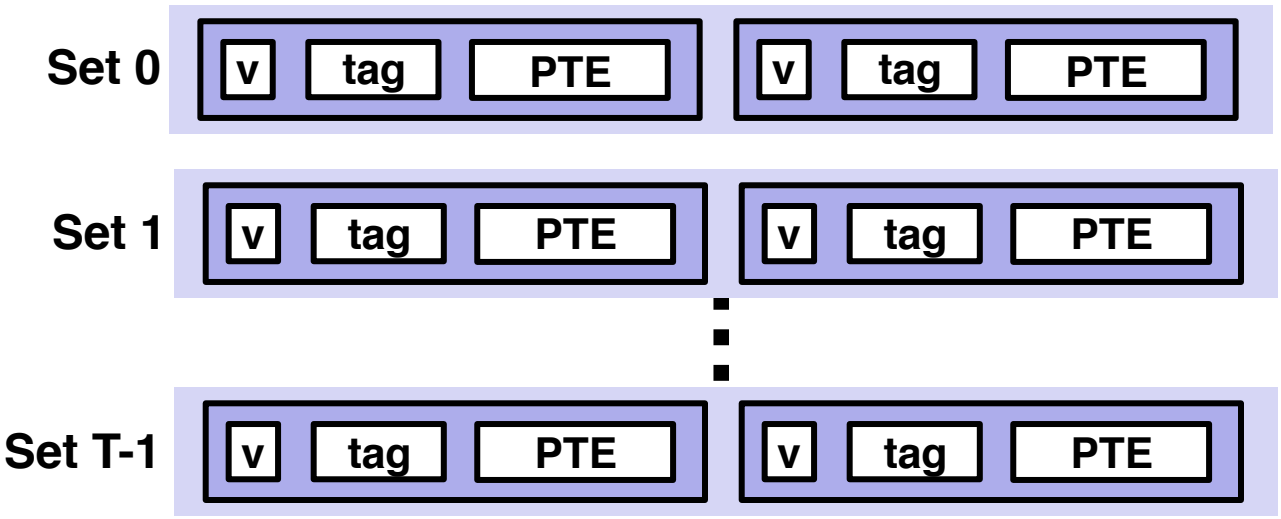

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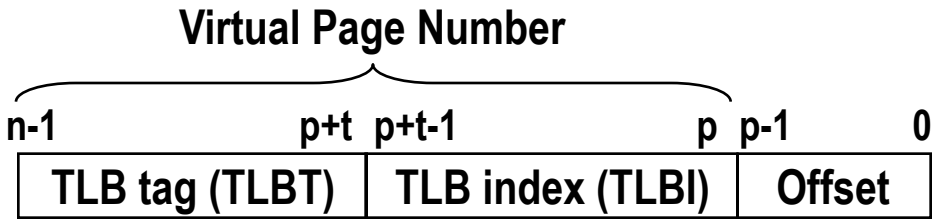

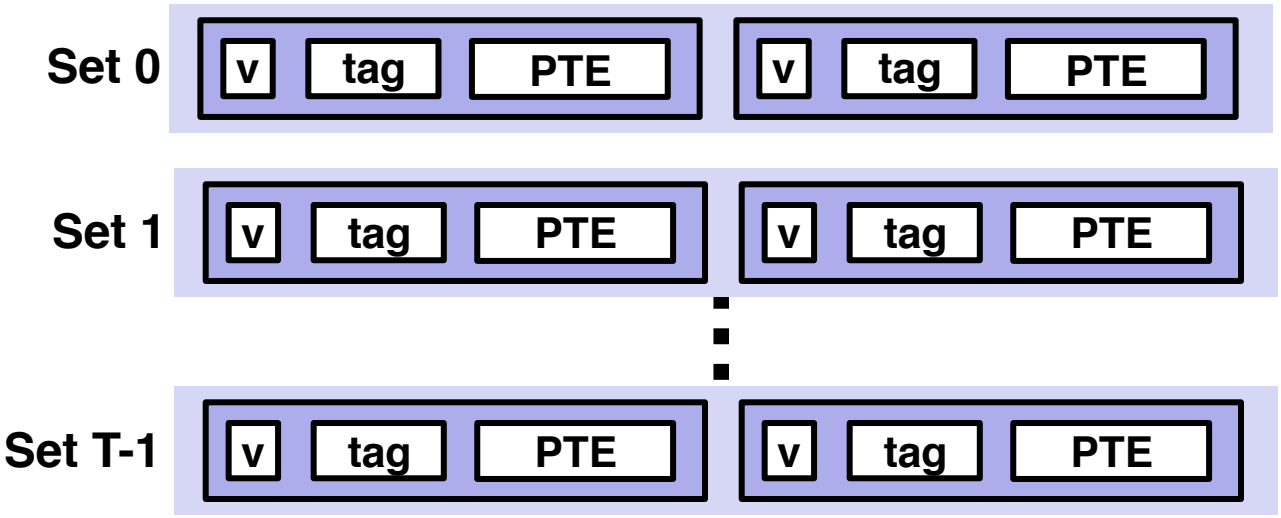

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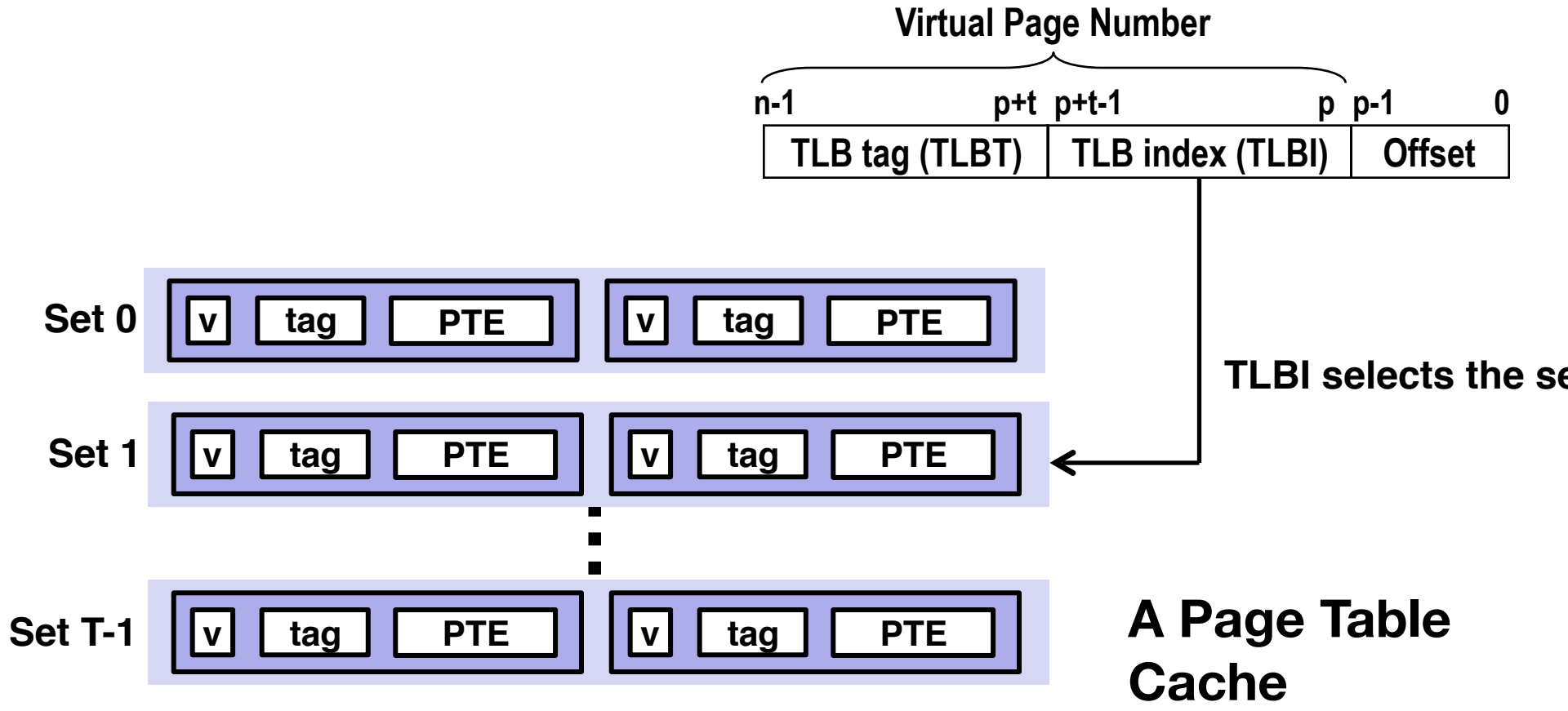

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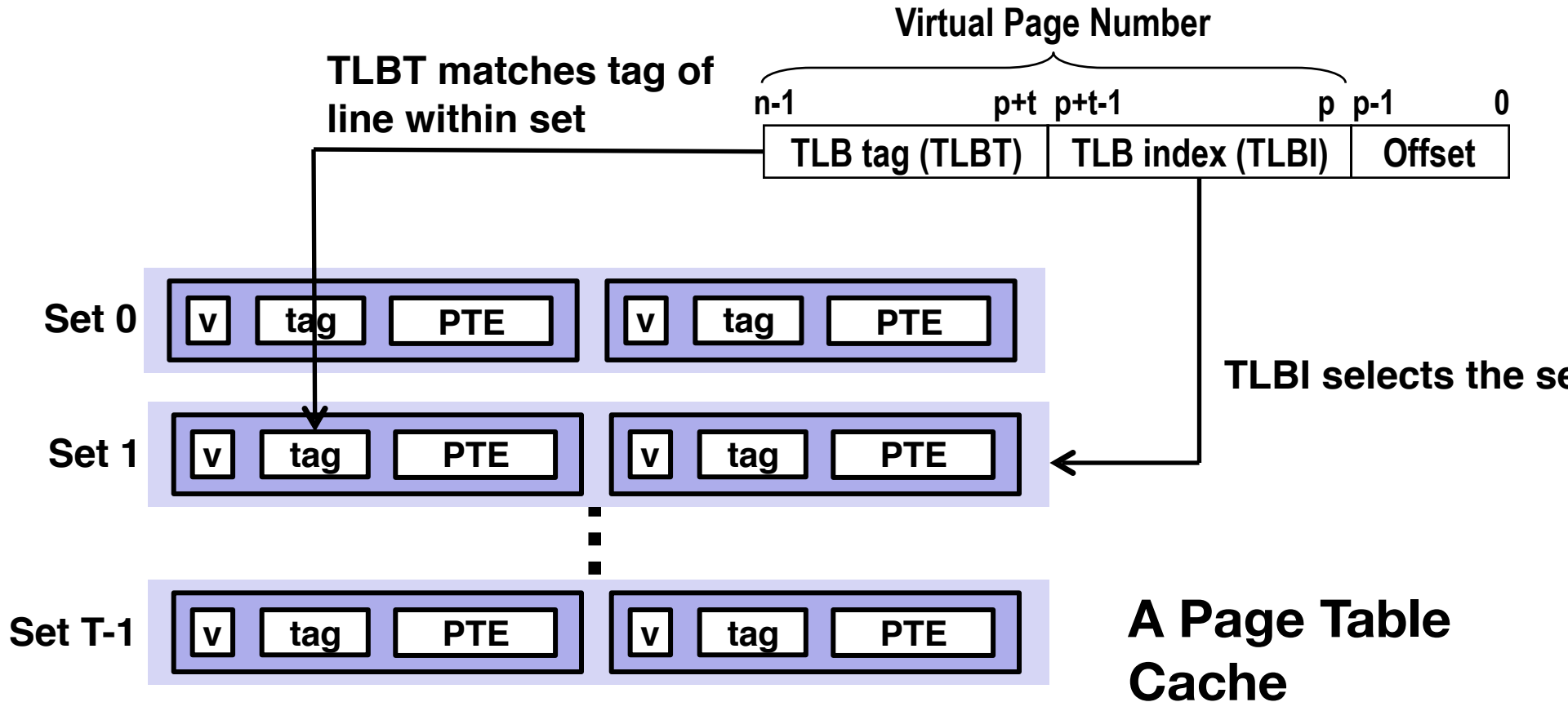

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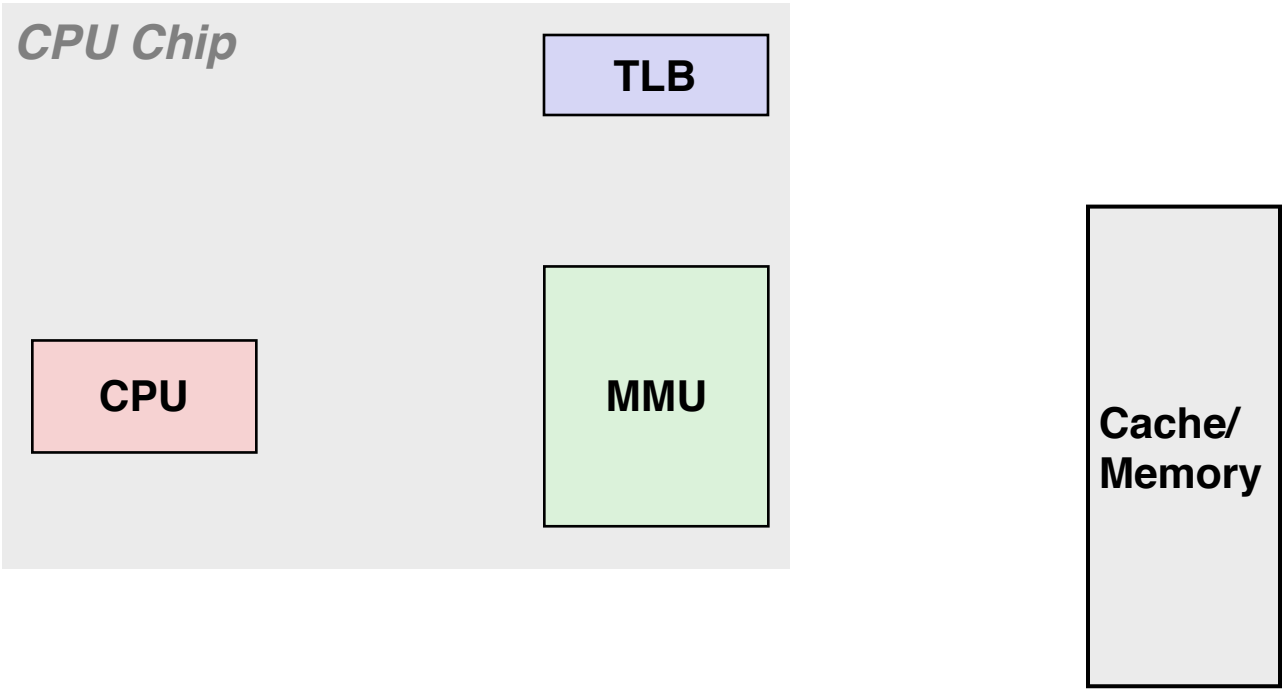

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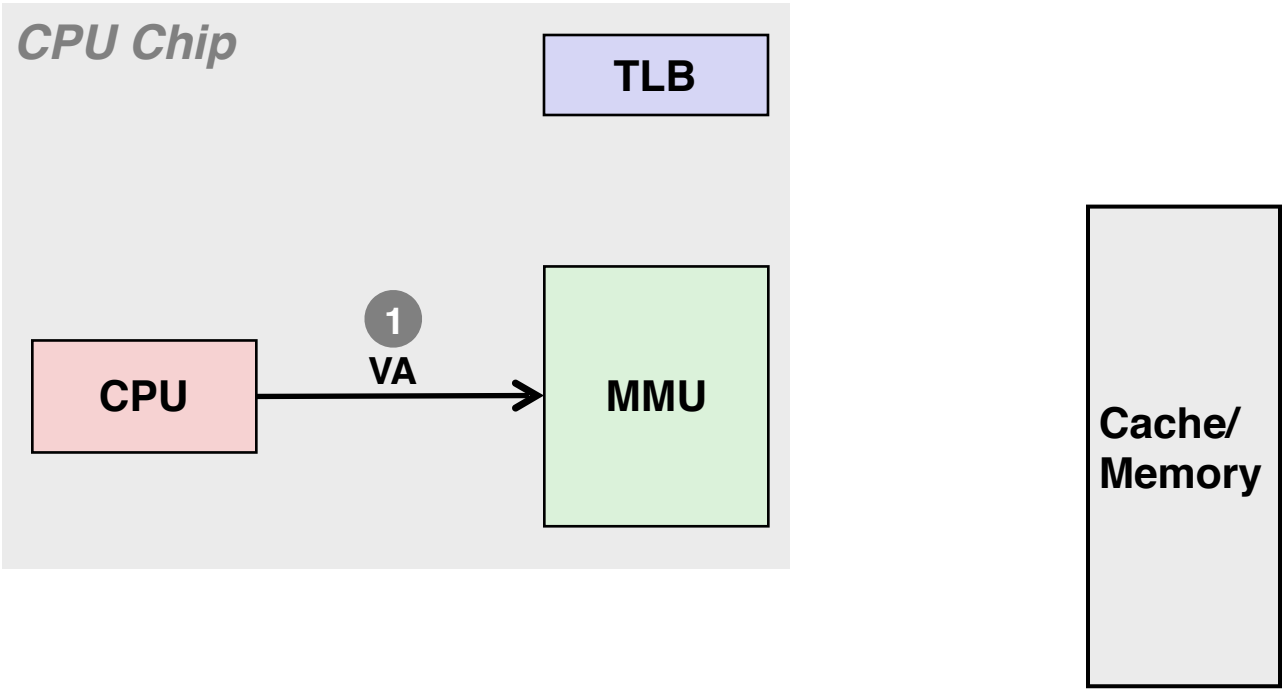

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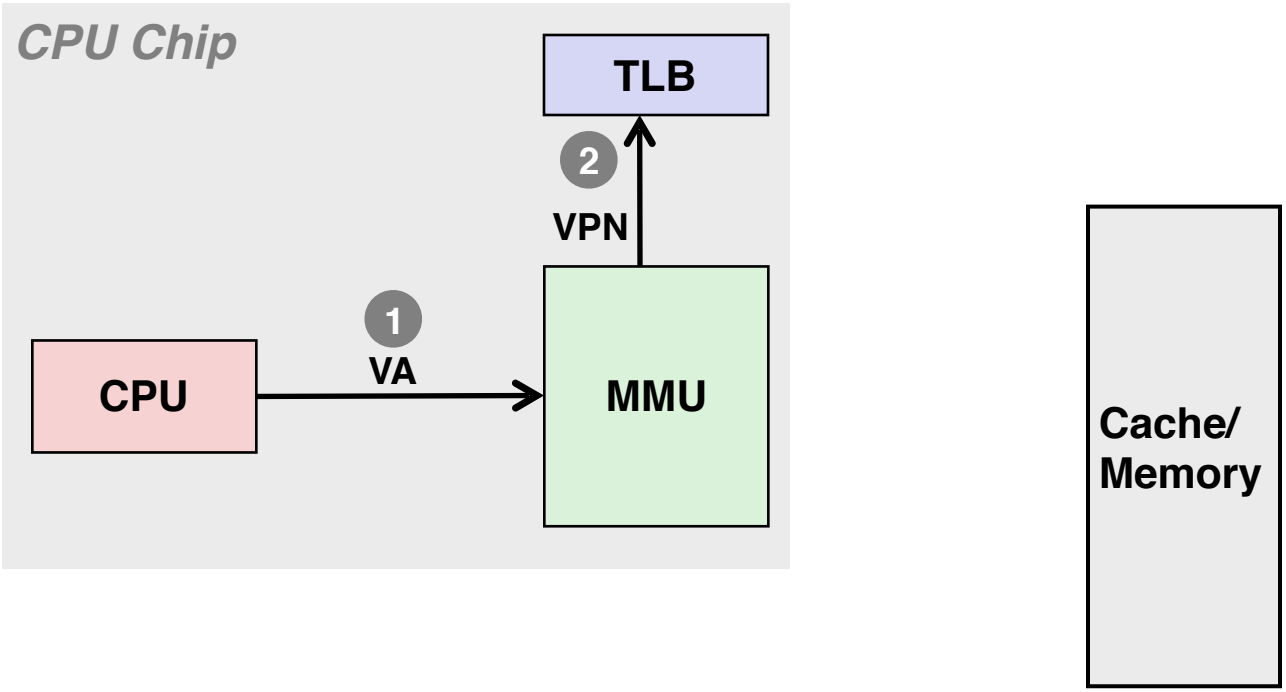

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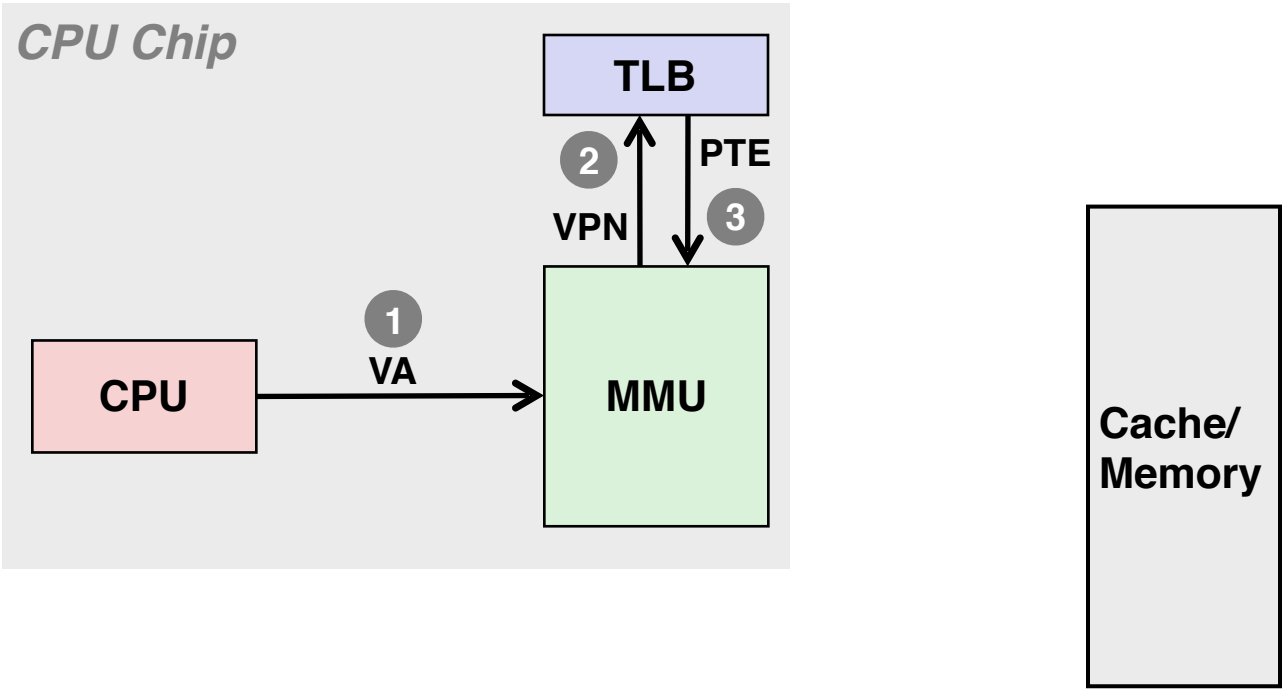

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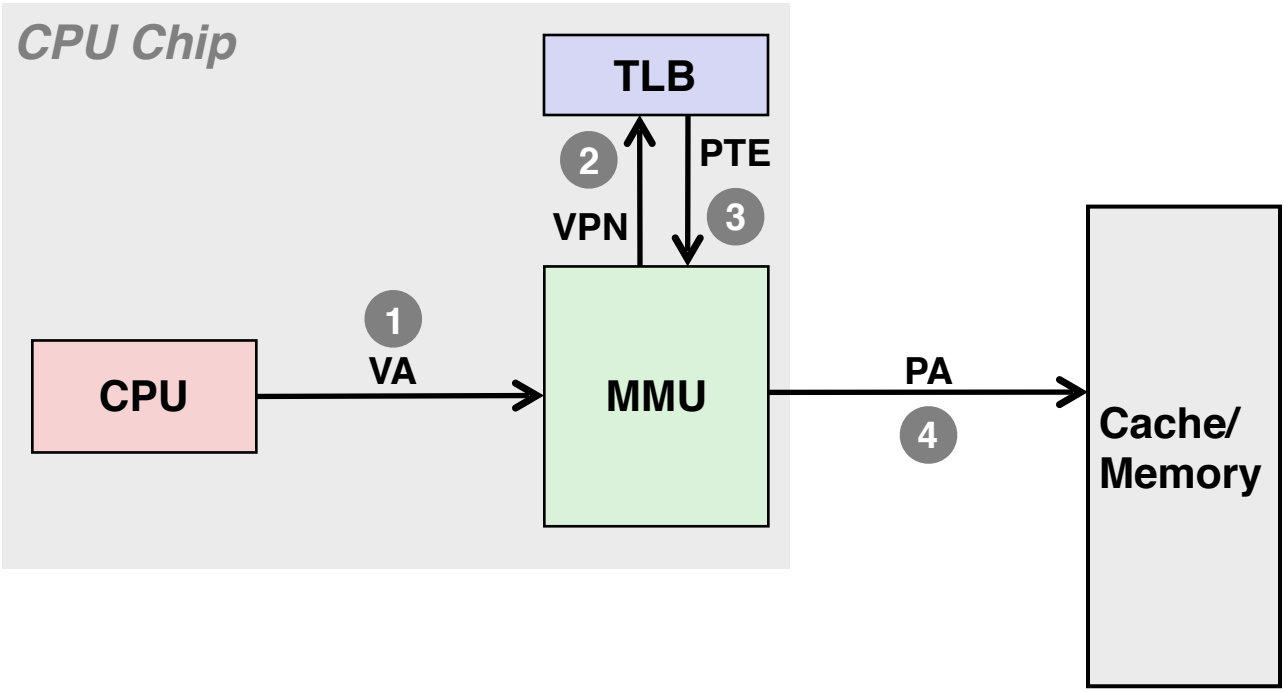

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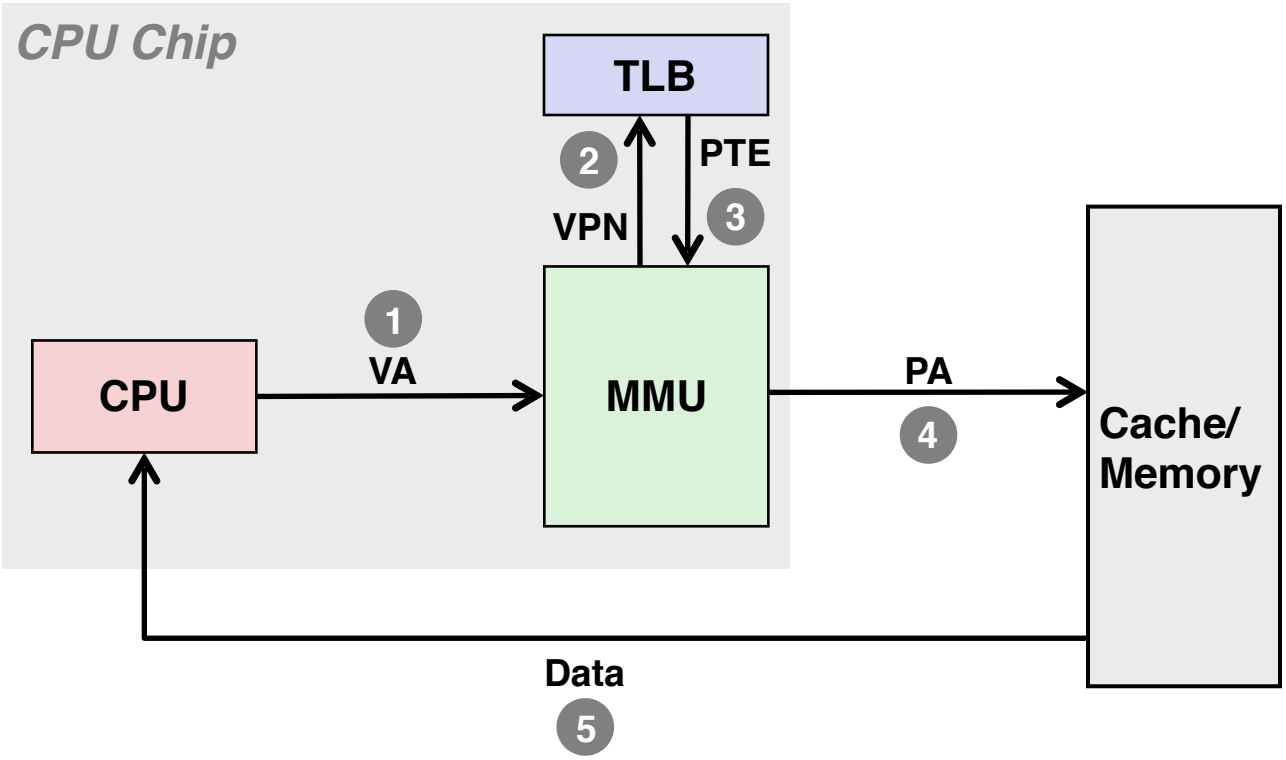

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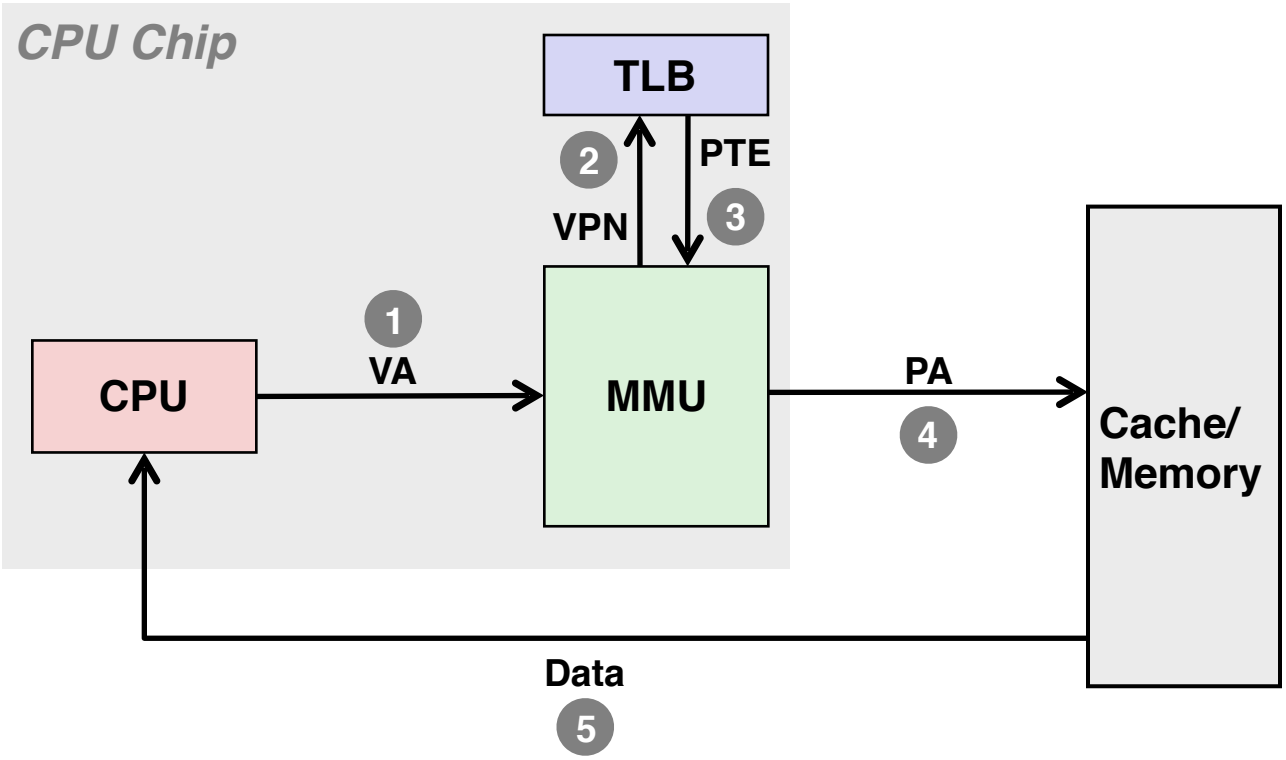
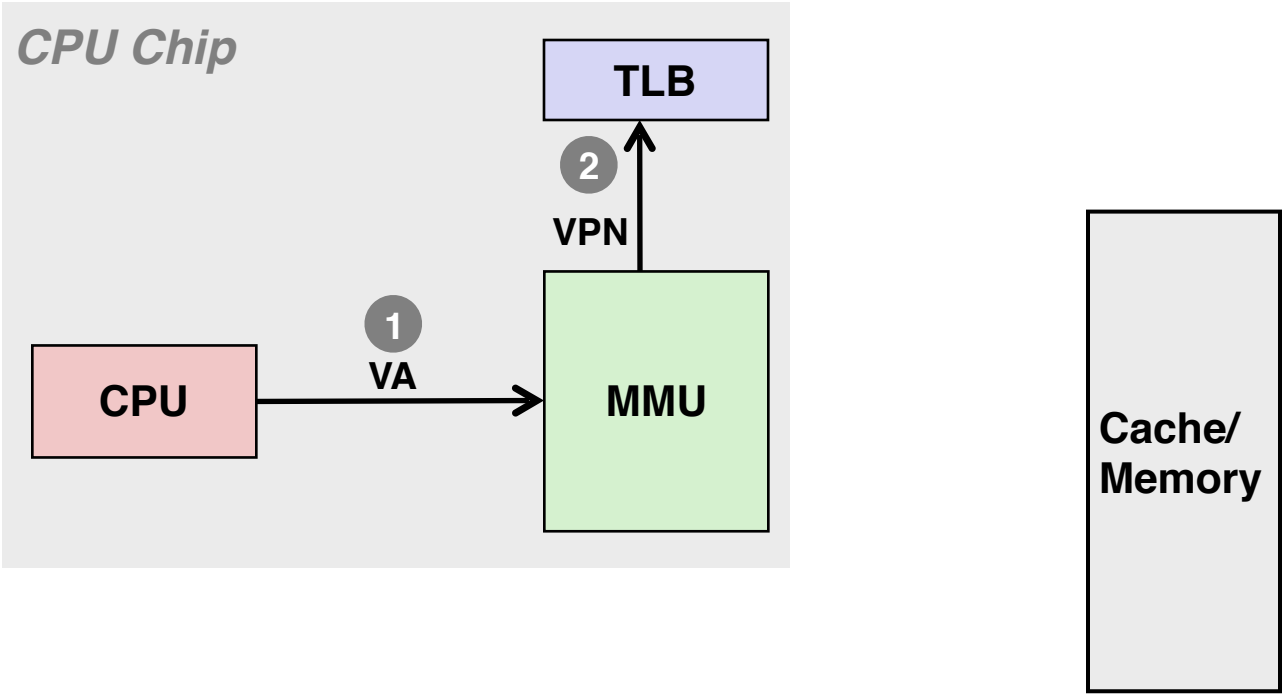


A TLB hit eliminates a memory access

TLB Miss



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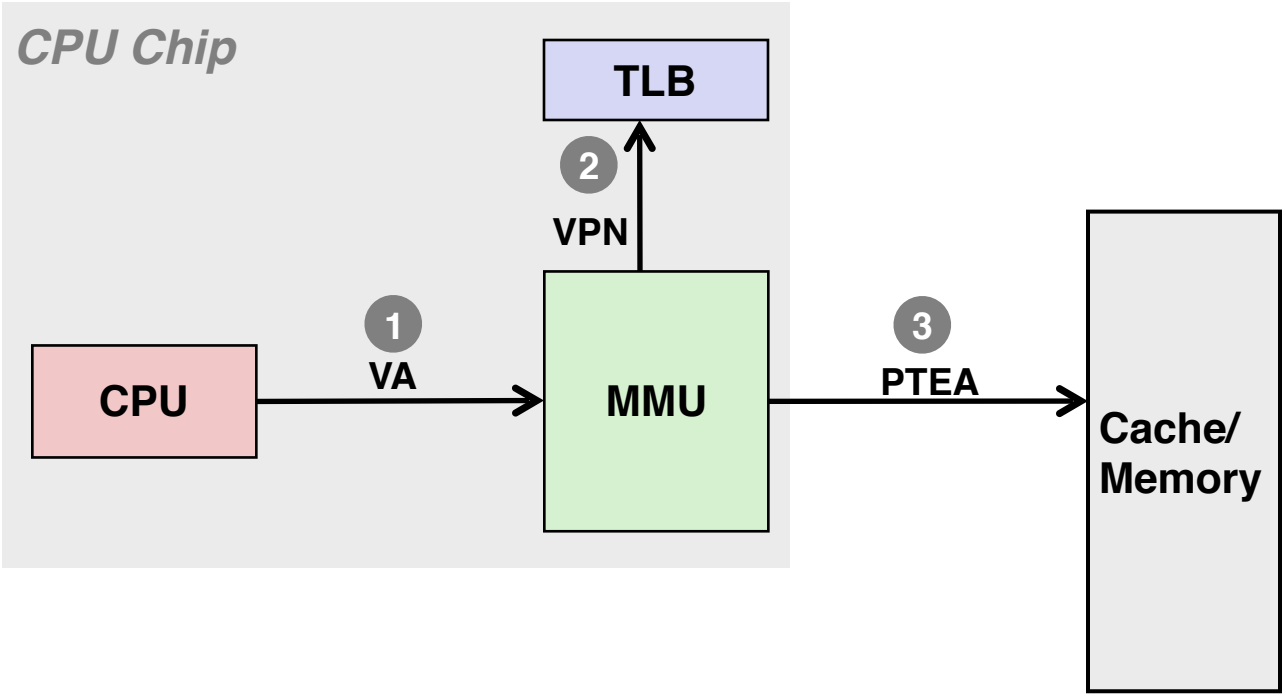

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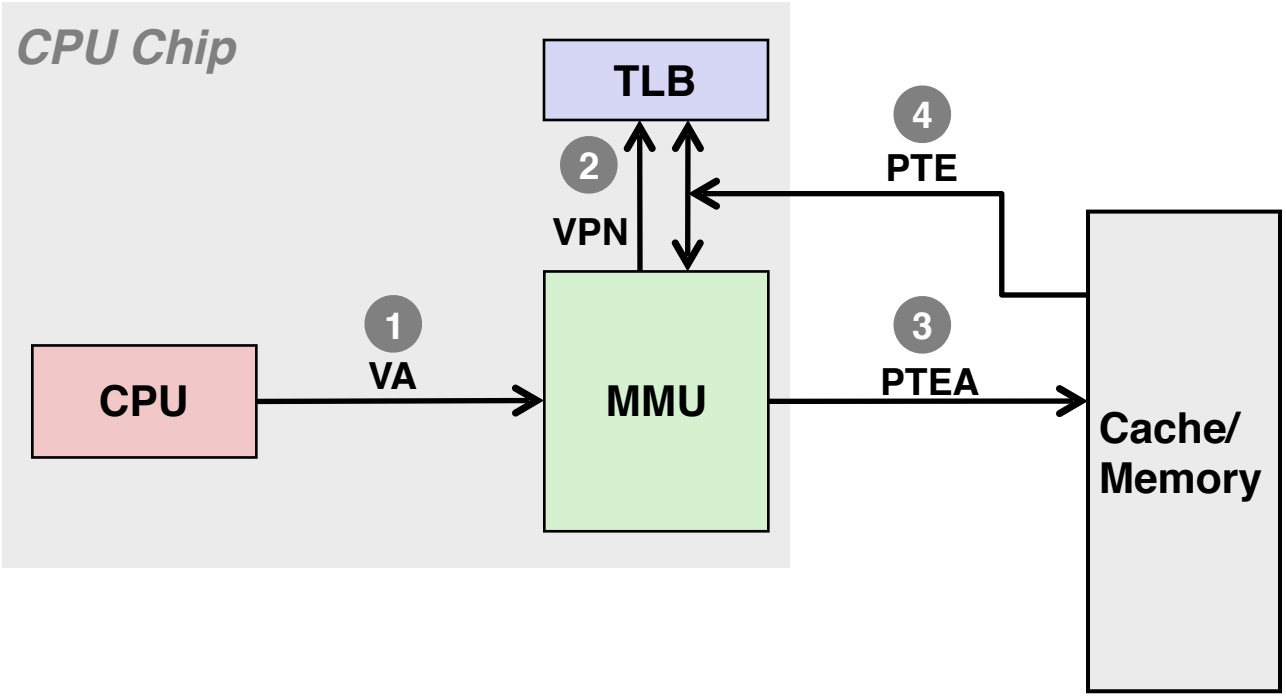

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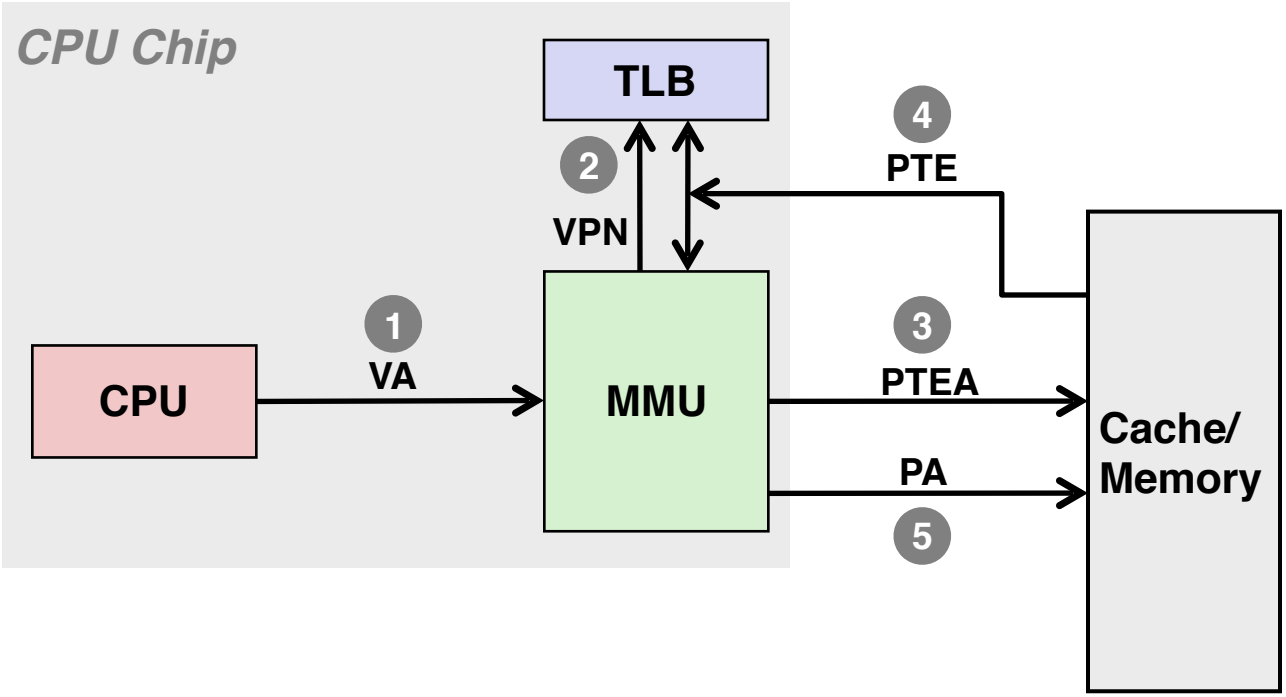

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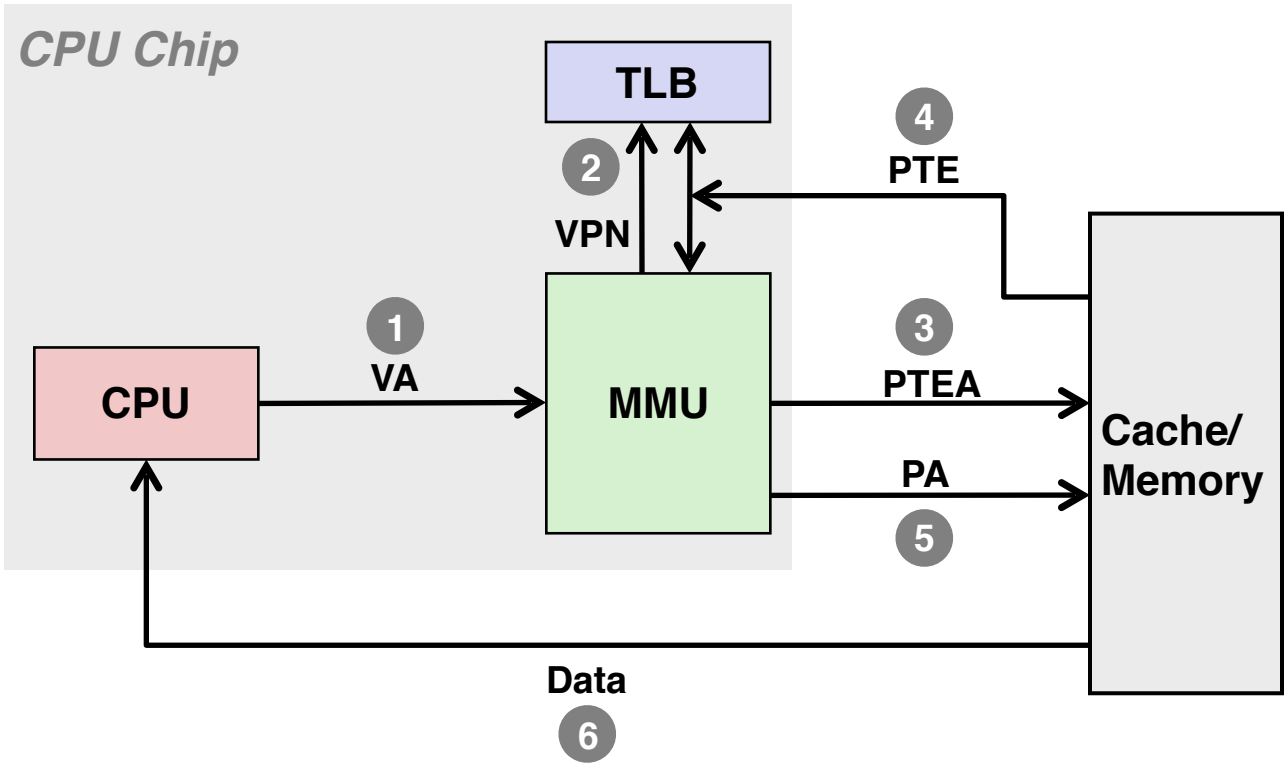
CPU Chip
TLB
4
PTE
2
VPN
1
VA
3
PTEA
CPU
MMU
Cache/
Memory
PA
5
Data
6

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  - 2^{36} PTEs in a page table
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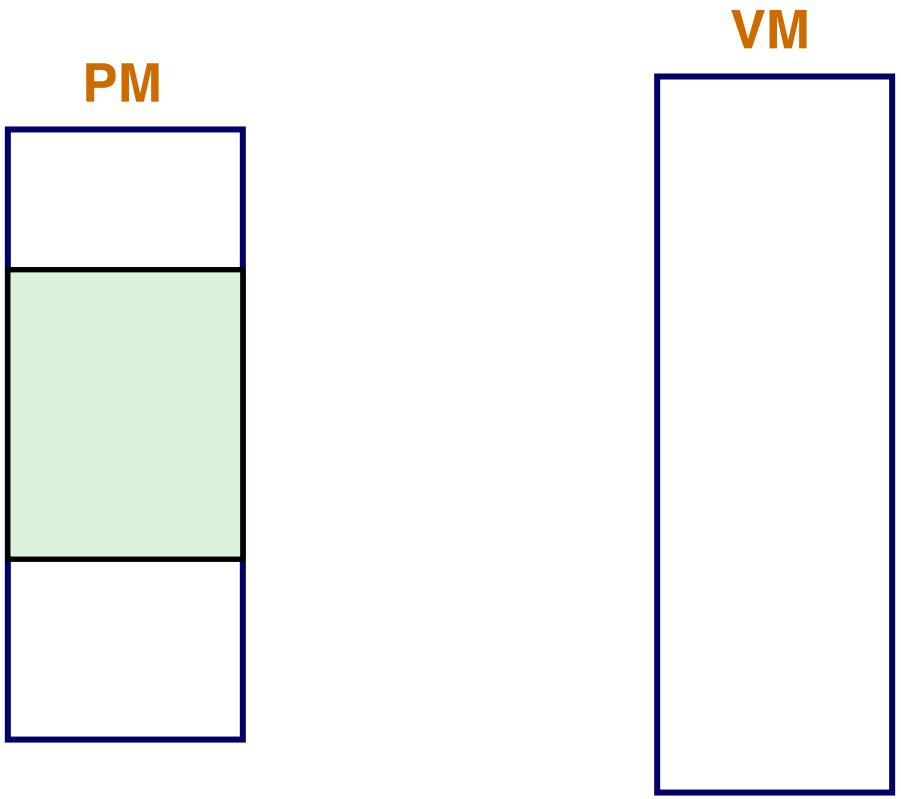
- Assume 4KB page, 48-bit virtual memory, each PTE is 8 Bytes
  - 2^{36} PTEs in a page table
  - 512 GB total size per page table??!!
- Problem: Page tables are huge
  - One table per process!
  - Storing them all in main memory wastes space

Solution: Page the Page Table

- Observation: Only a small number of pages (working set) are accessed during a certain period of time, due to locality
- Put only the relevant page table entires in main memory
- Idea: Put Page Table in Virtual Memory and swap it just like data



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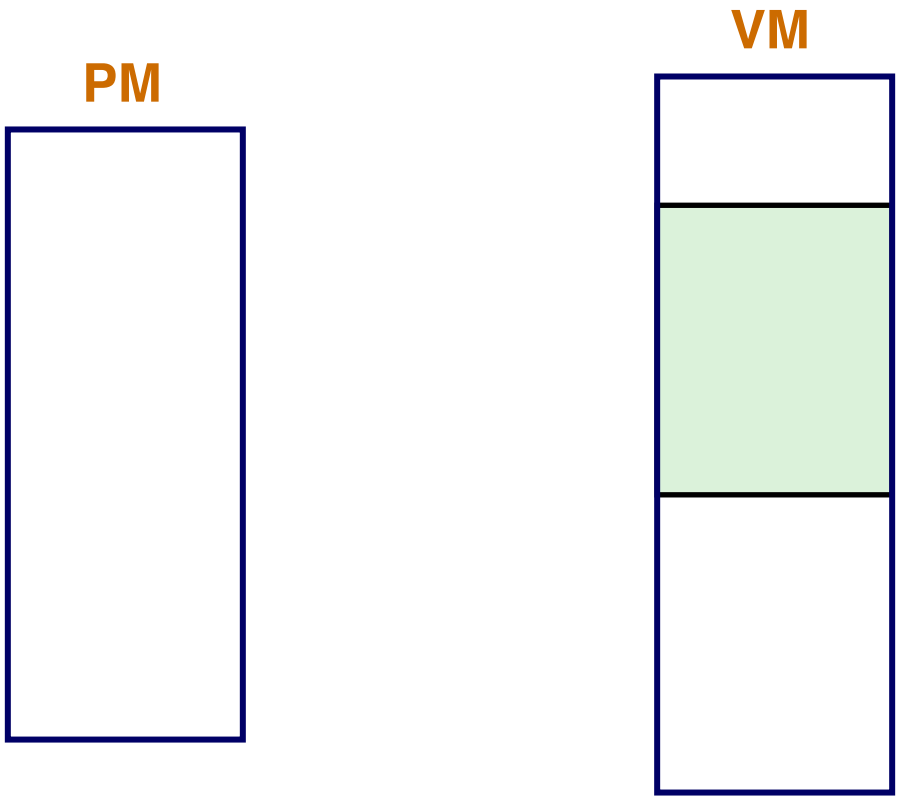

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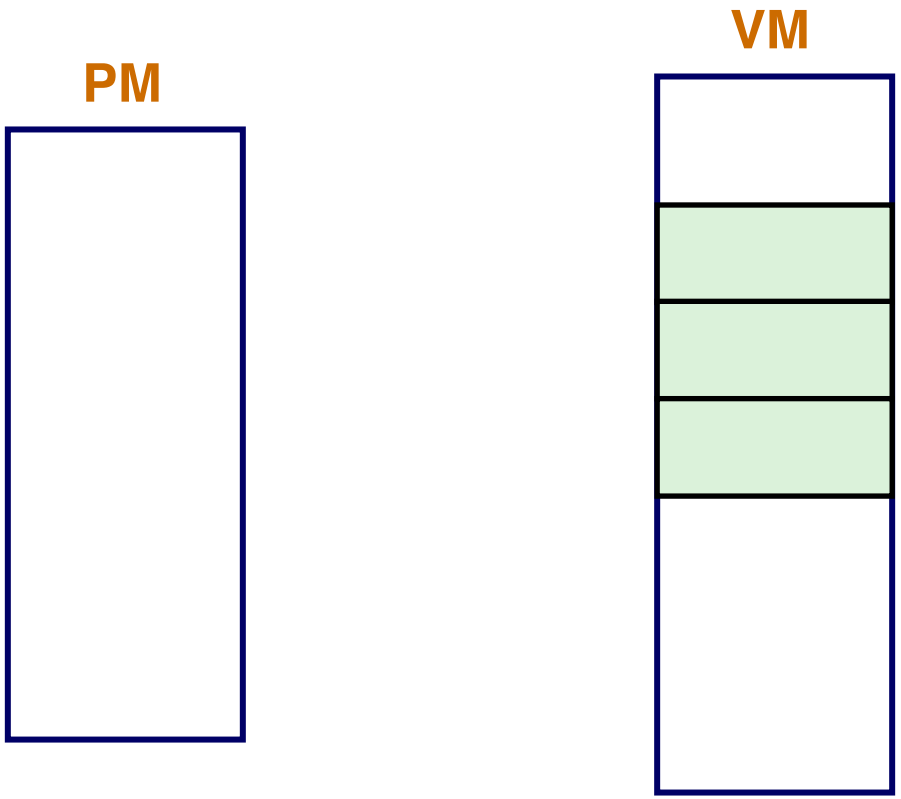

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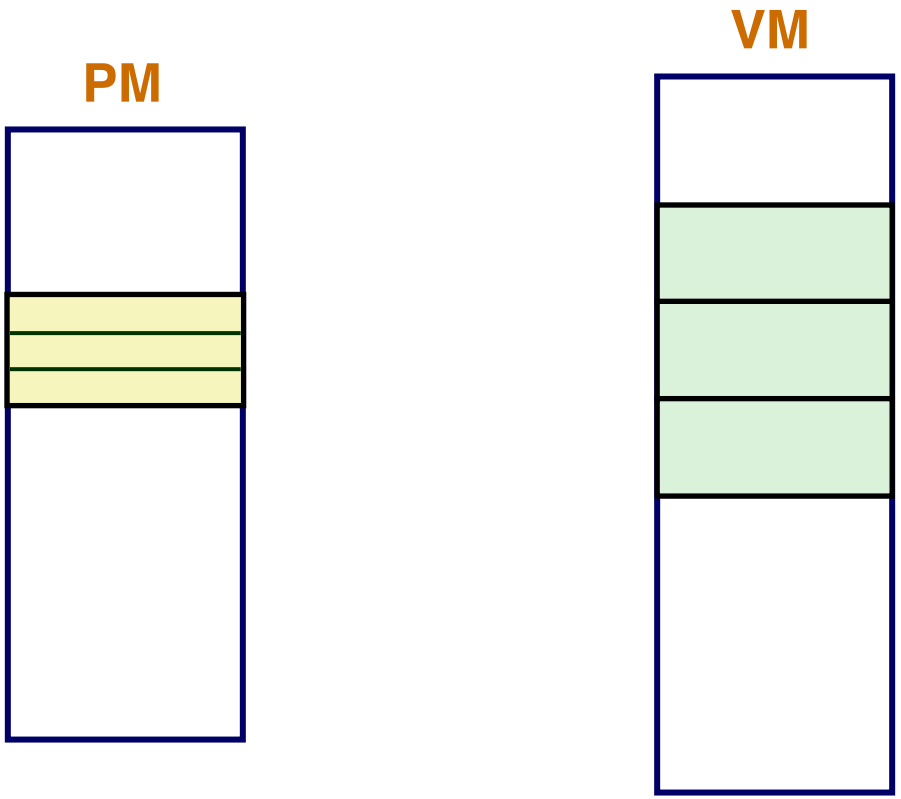

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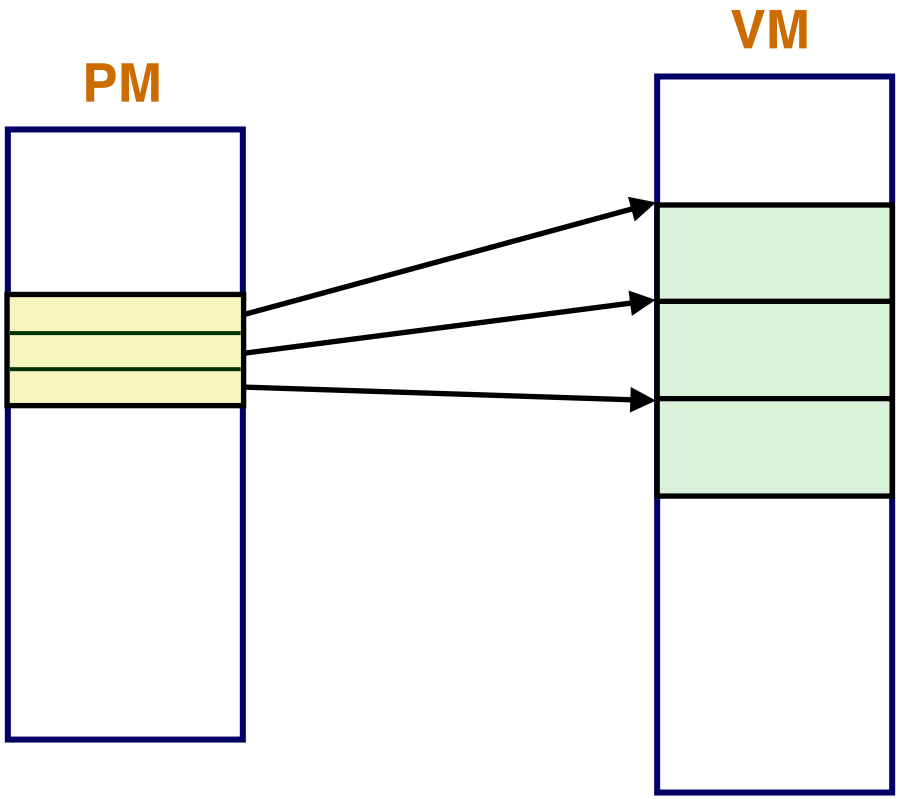

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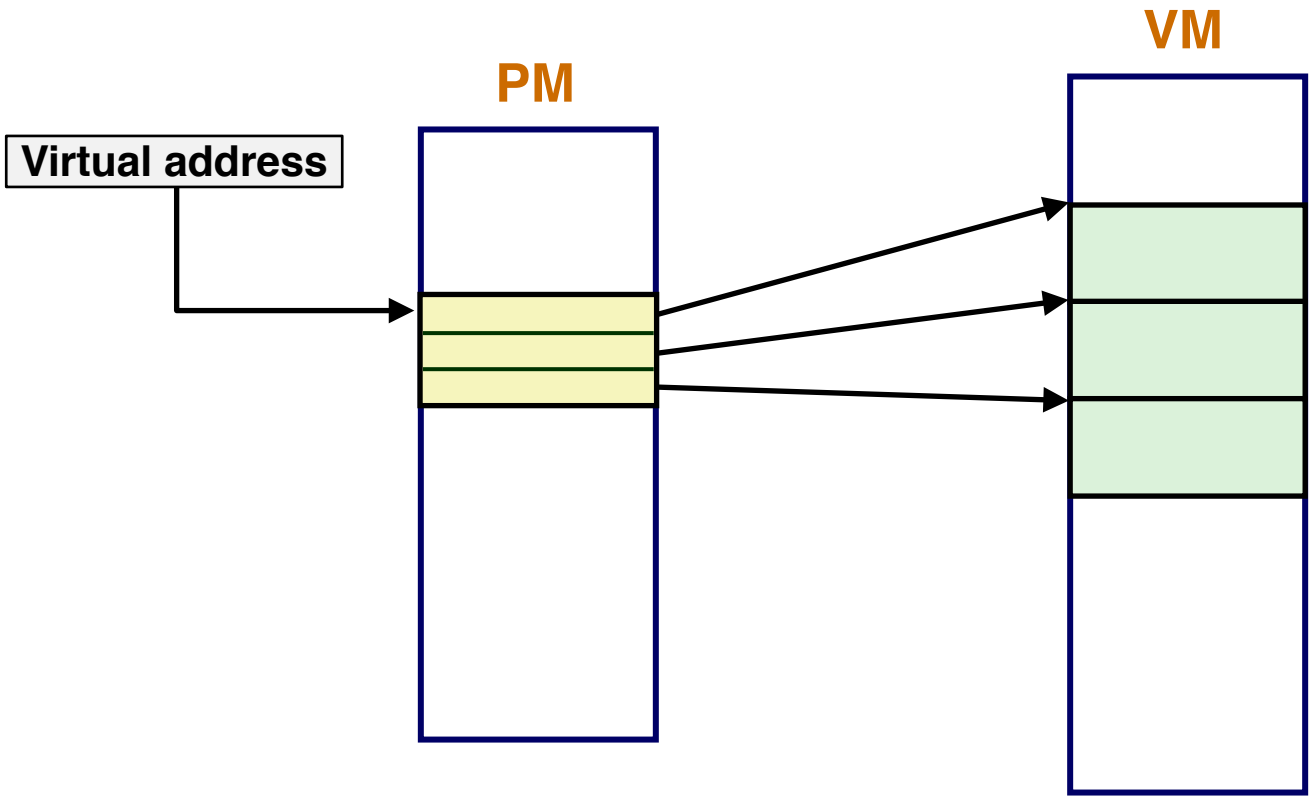

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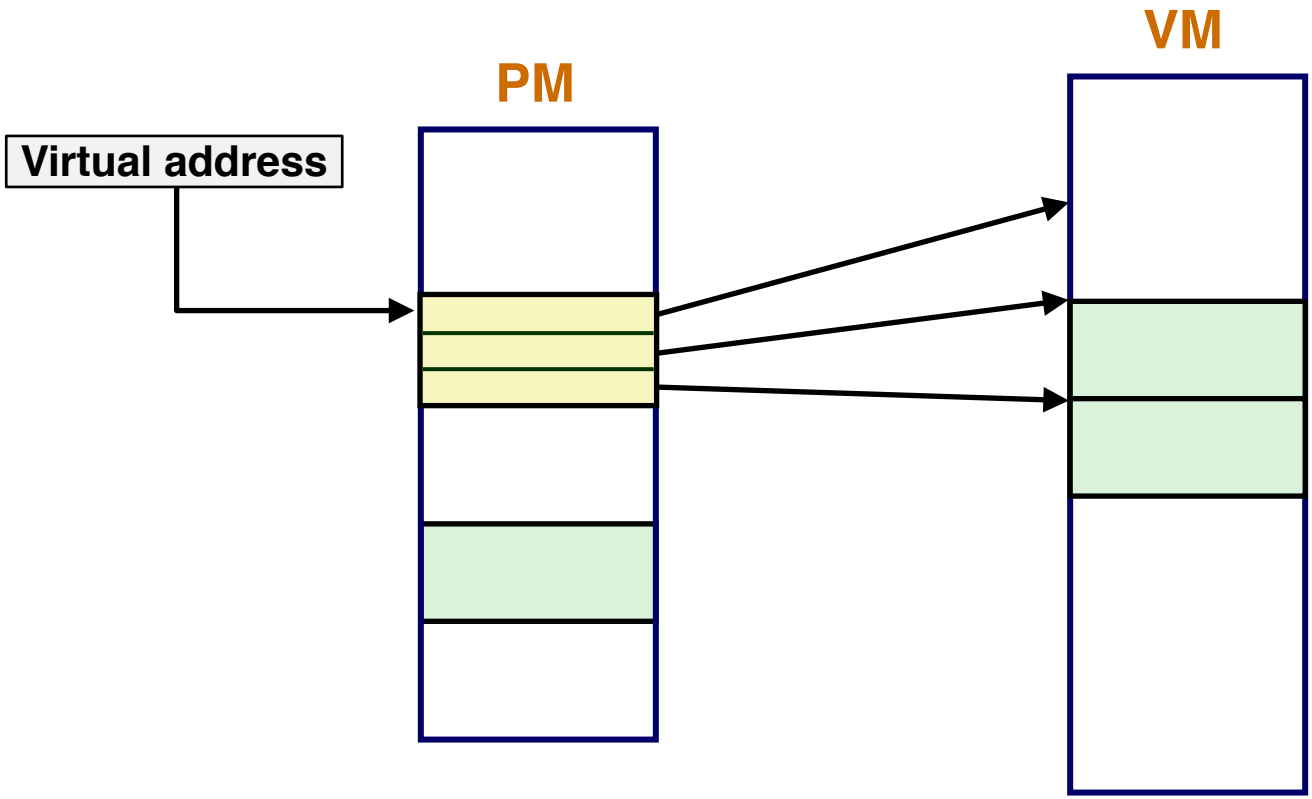

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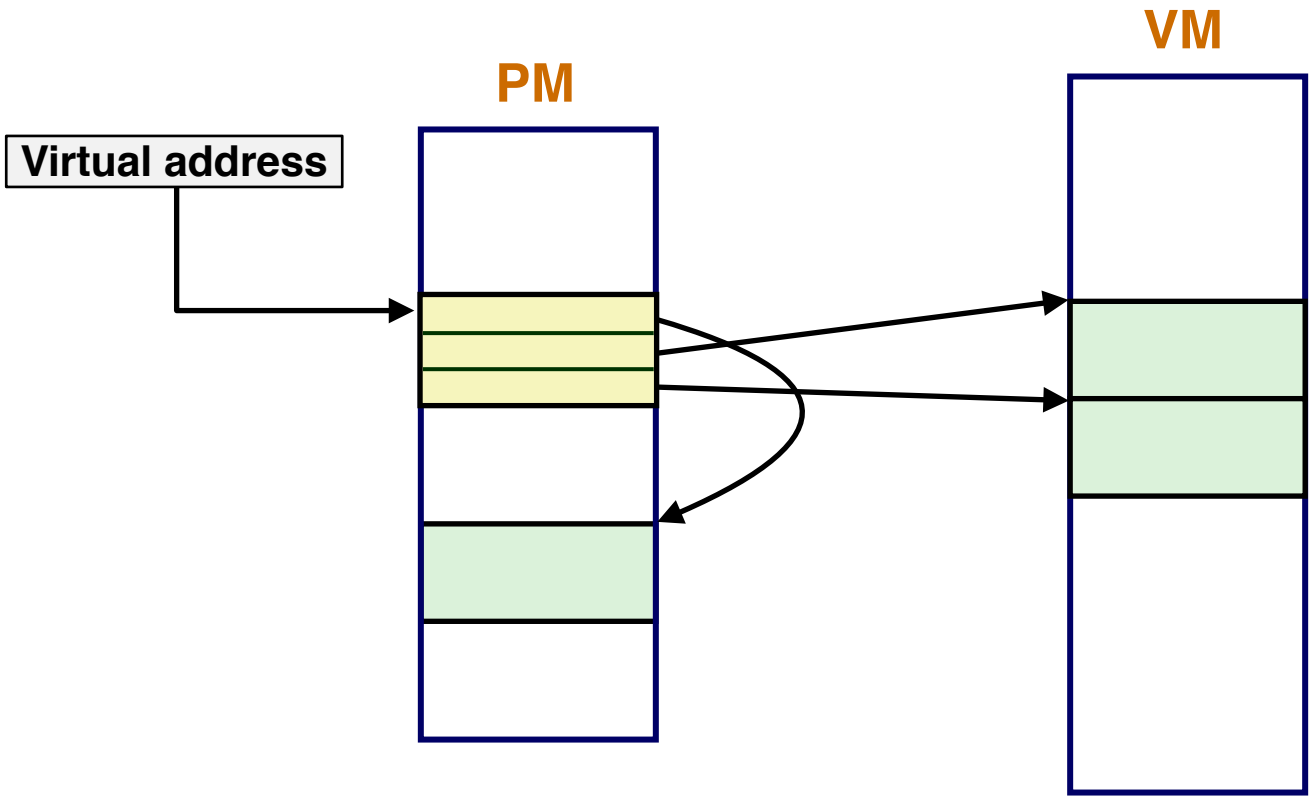
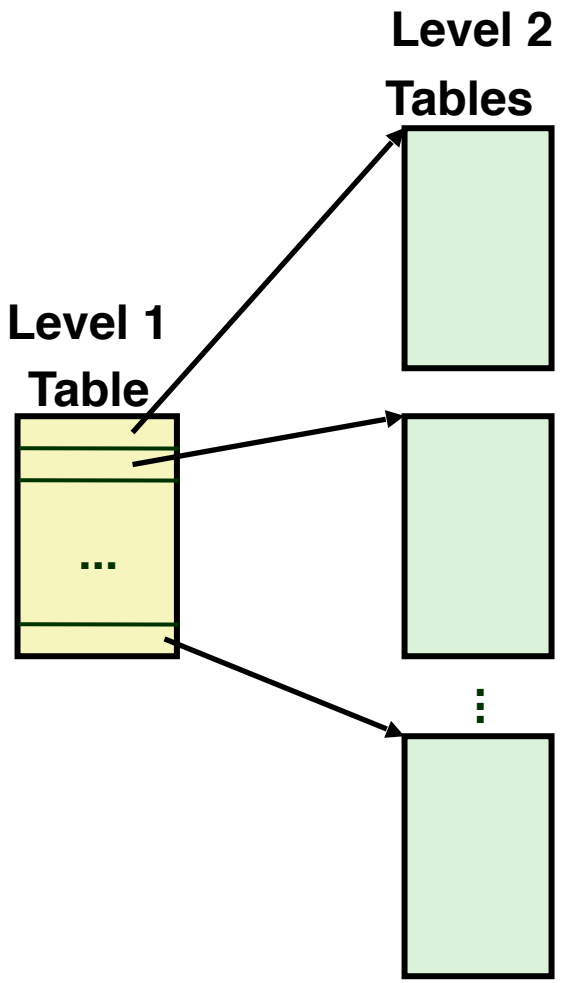
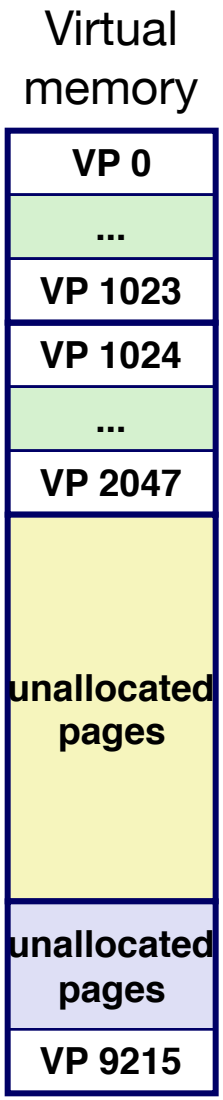


Effectively: A 2-Level Page Table

- Level 1 table:
  - Always in memory at a known location.
  - Each L1 PTE points to the start address of a L2 page table.
  - Bring that table to memory on-demand.
- Level 2 table:
  - Each PTE points to an actual data page



A Two-Level Page Table Hierarchy



32 bit addresses, 4KB pages, 4-byte PTEs

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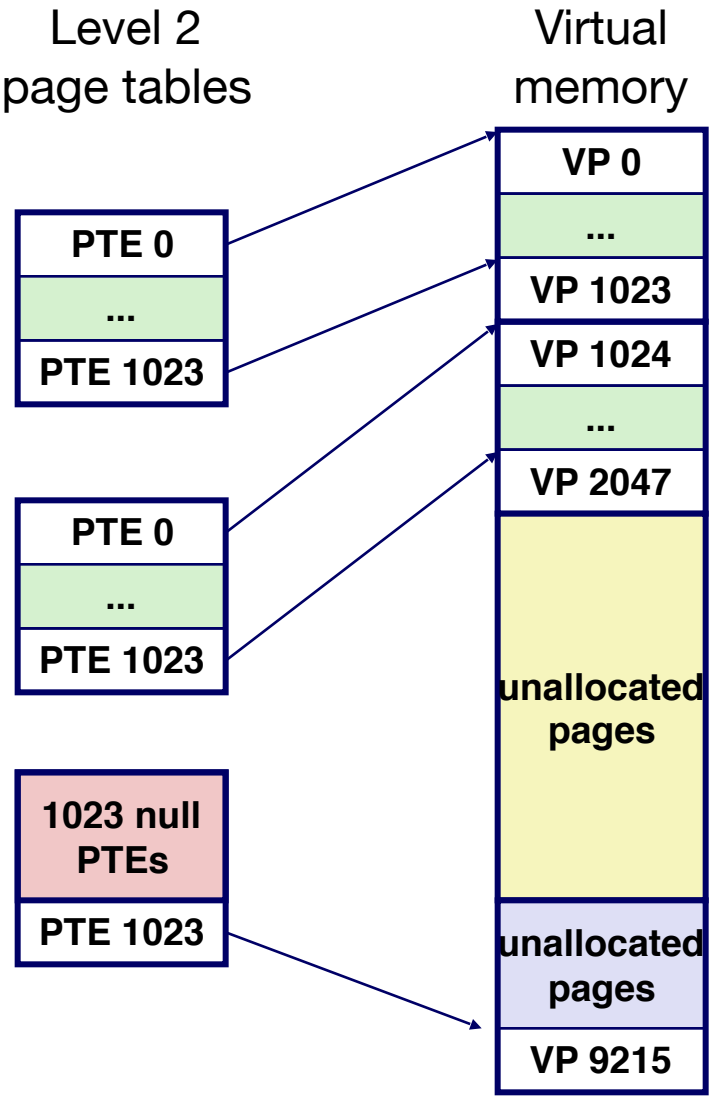

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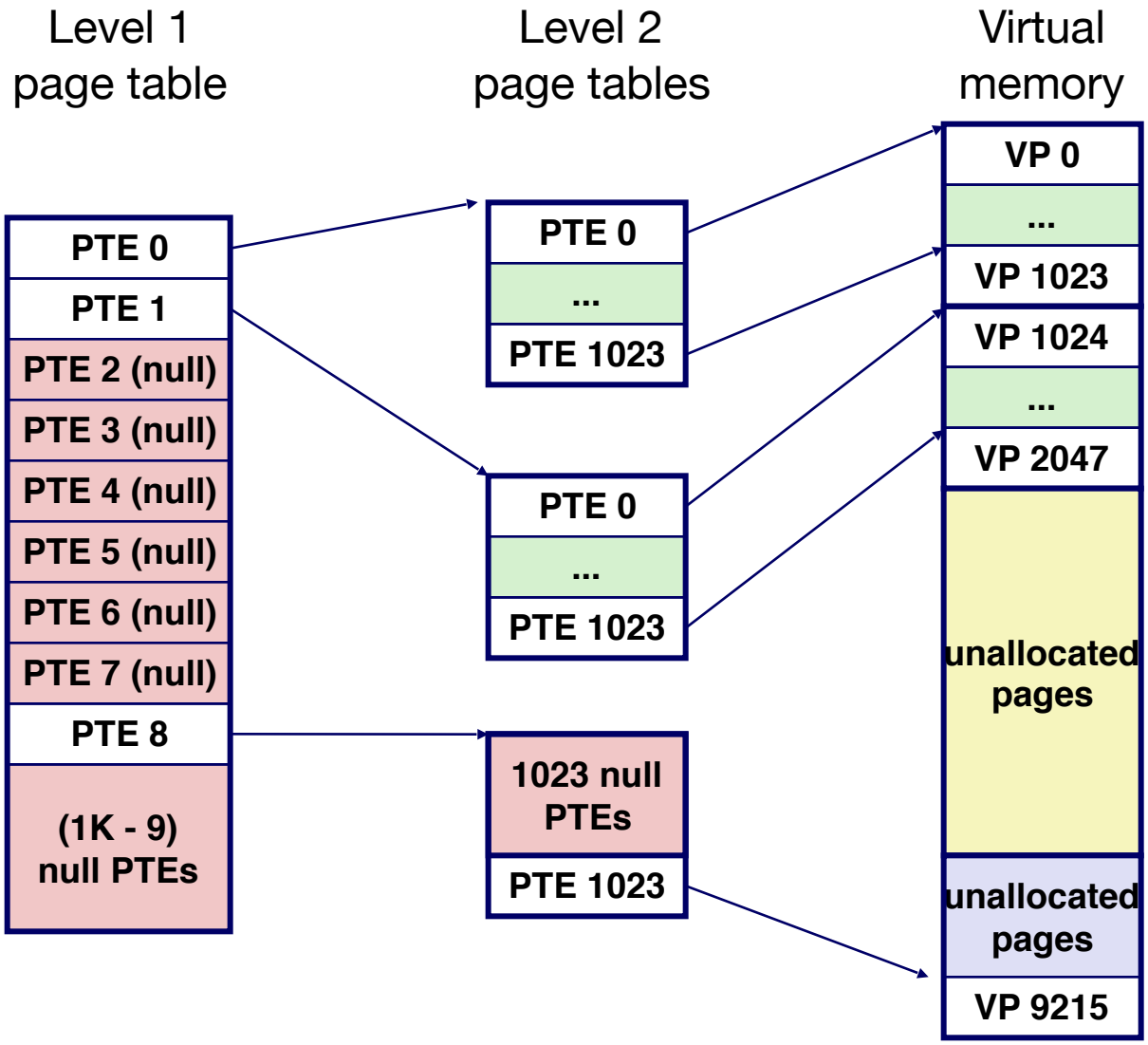

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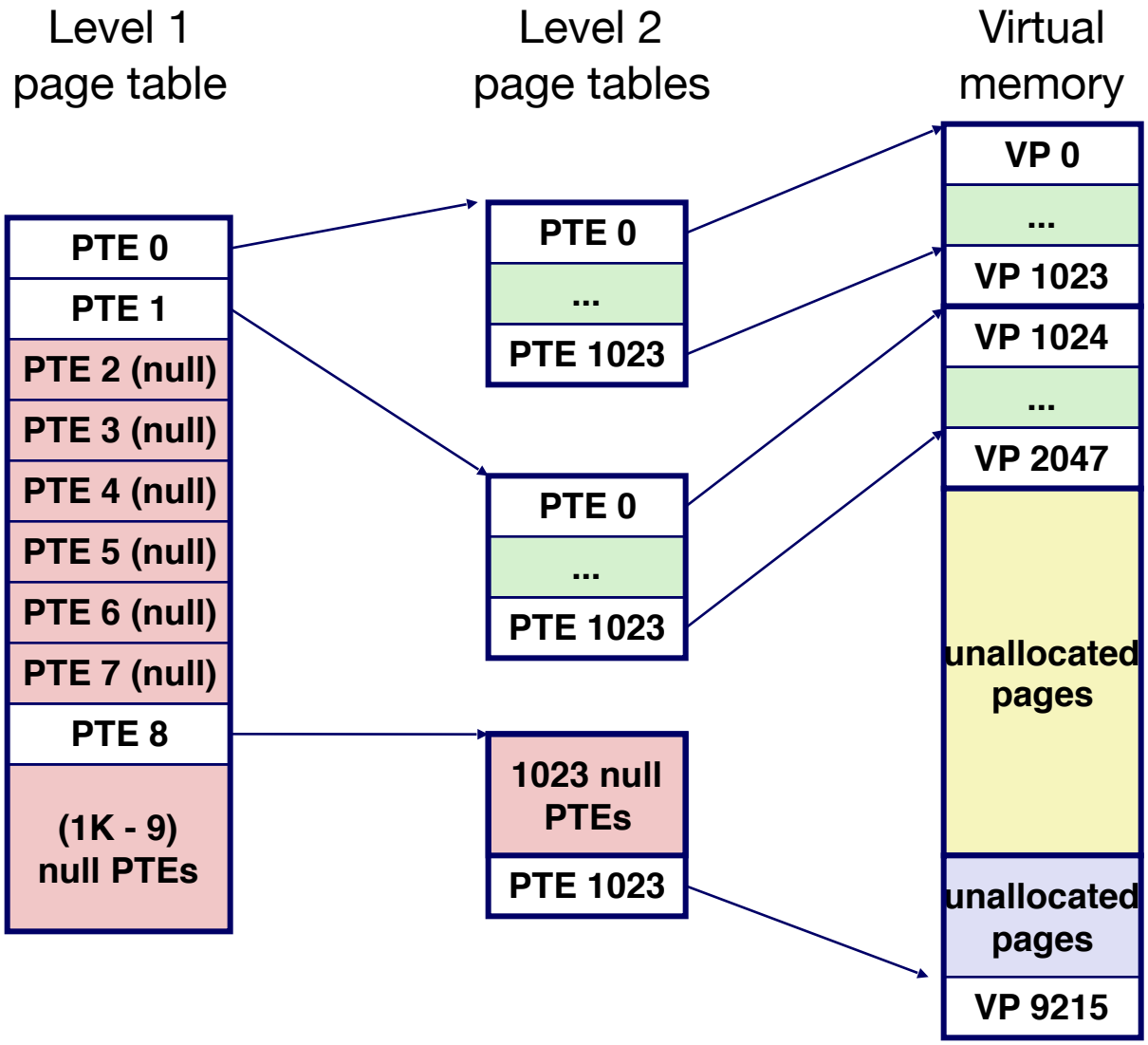

- Level 2 page table size:
  - $2^{32} / 2^{12} * 4 = 4$ MB
- Level 1 page table size:
  - $(2^{32} / 2^{12} * 4) / 2^{12} * 4 = 4$ KB

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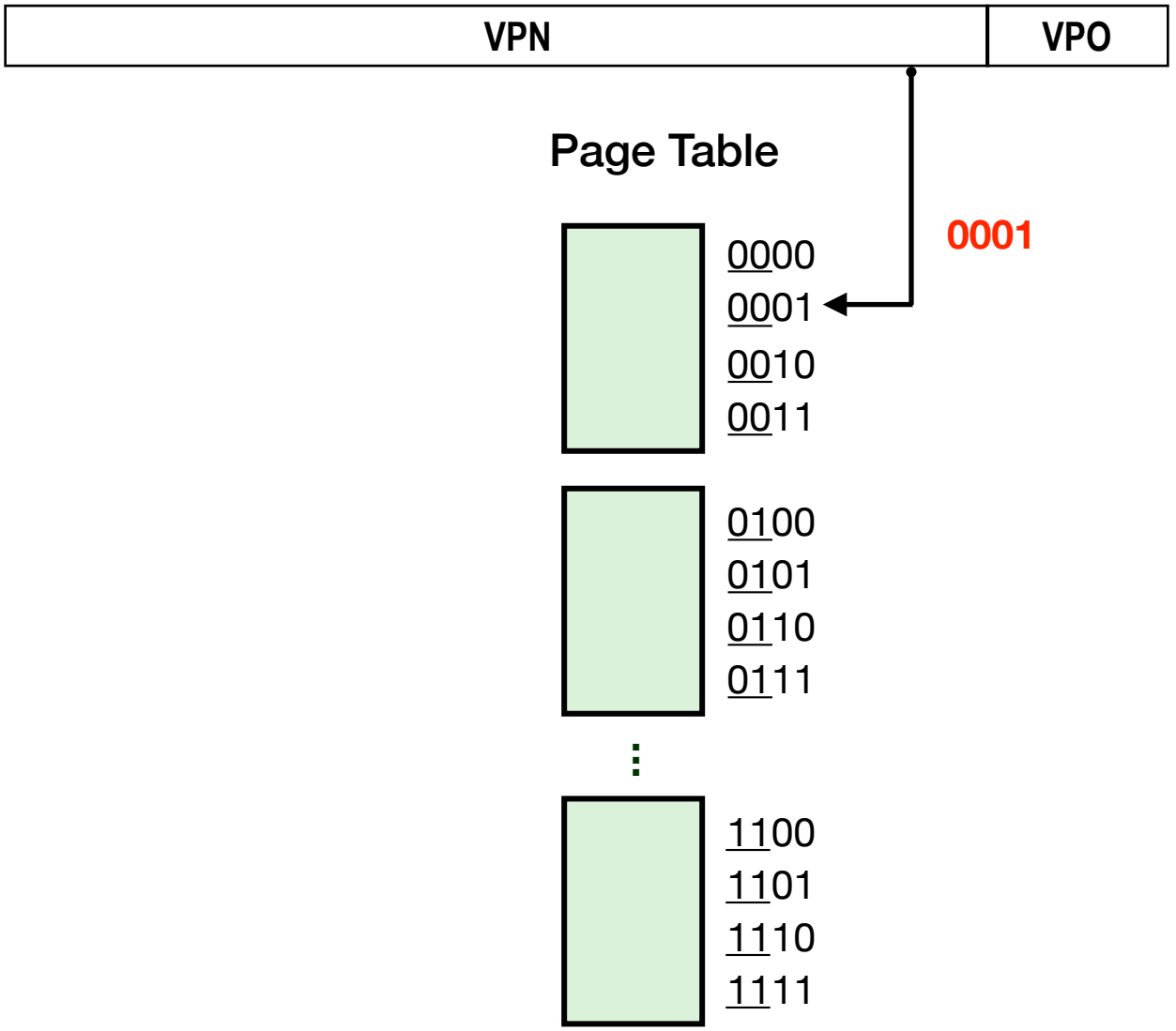

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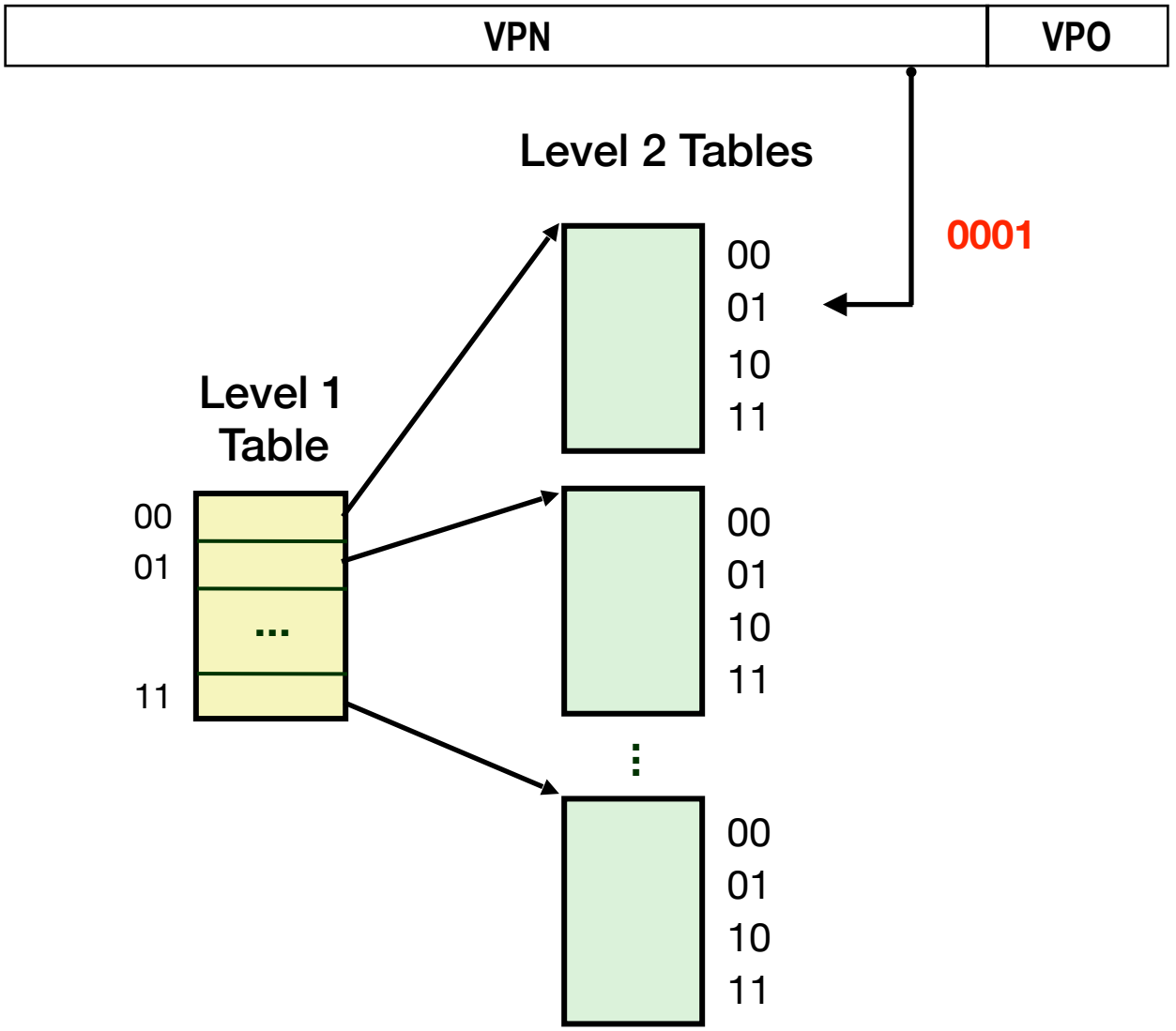

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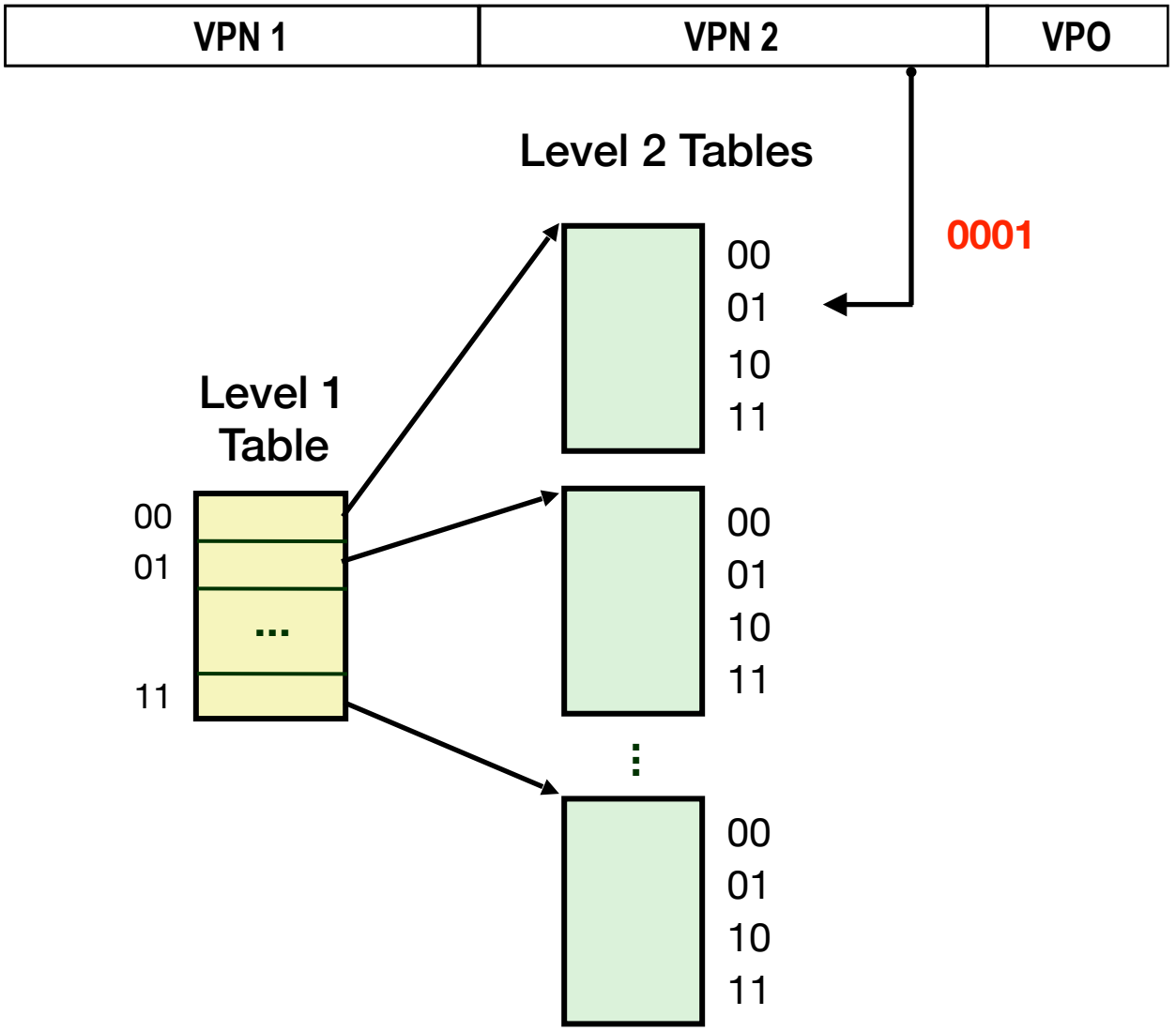

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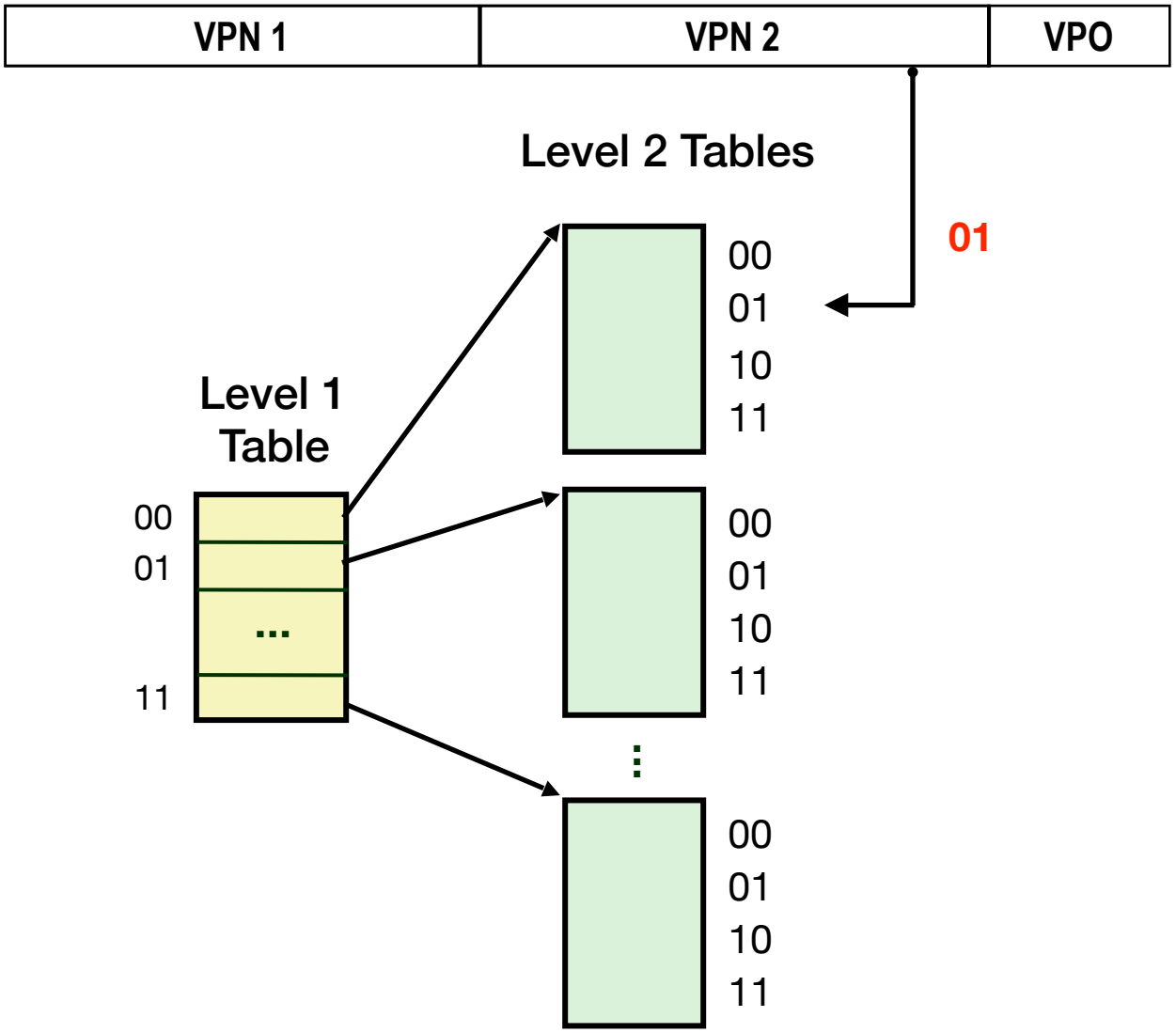

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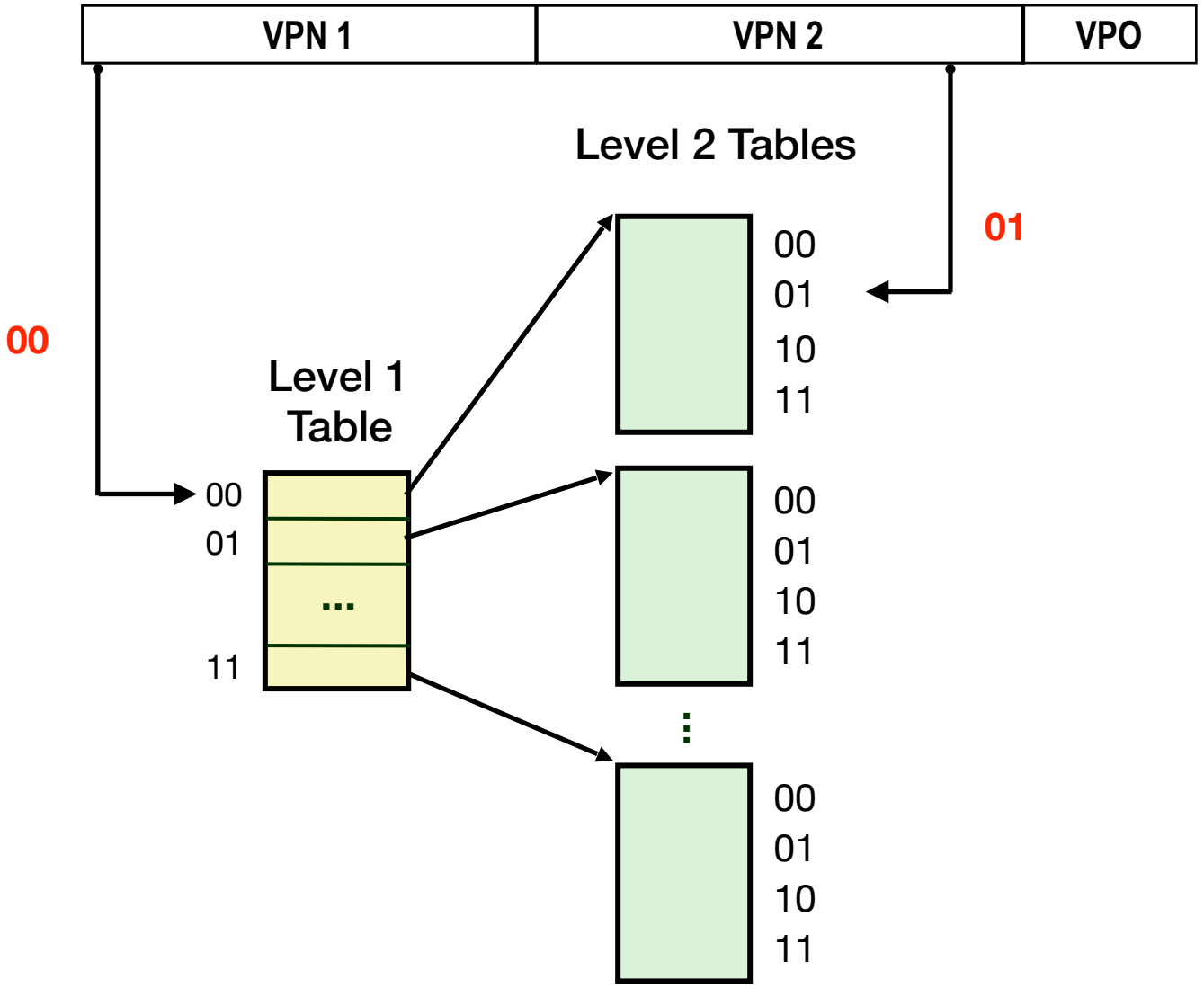

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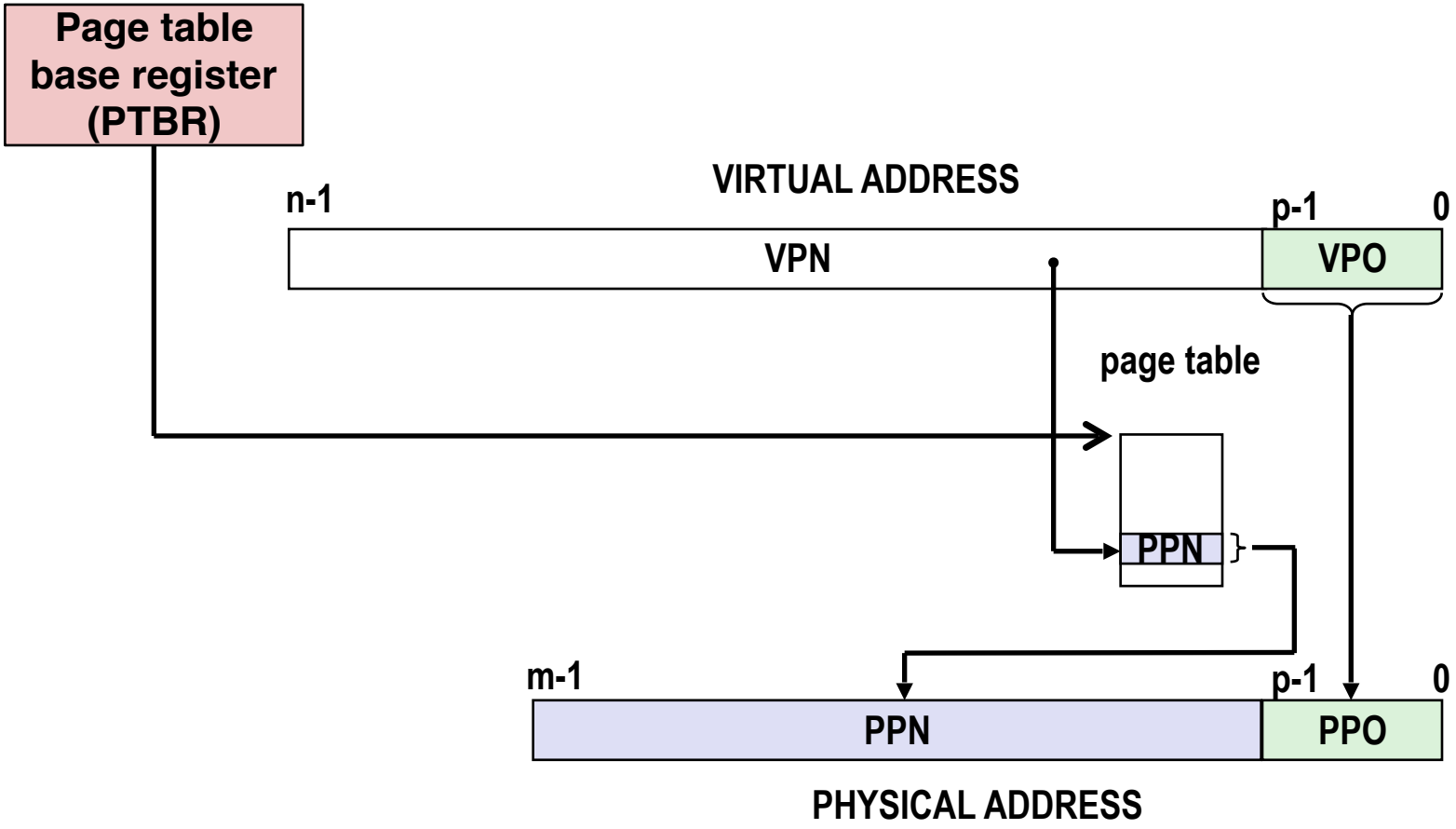

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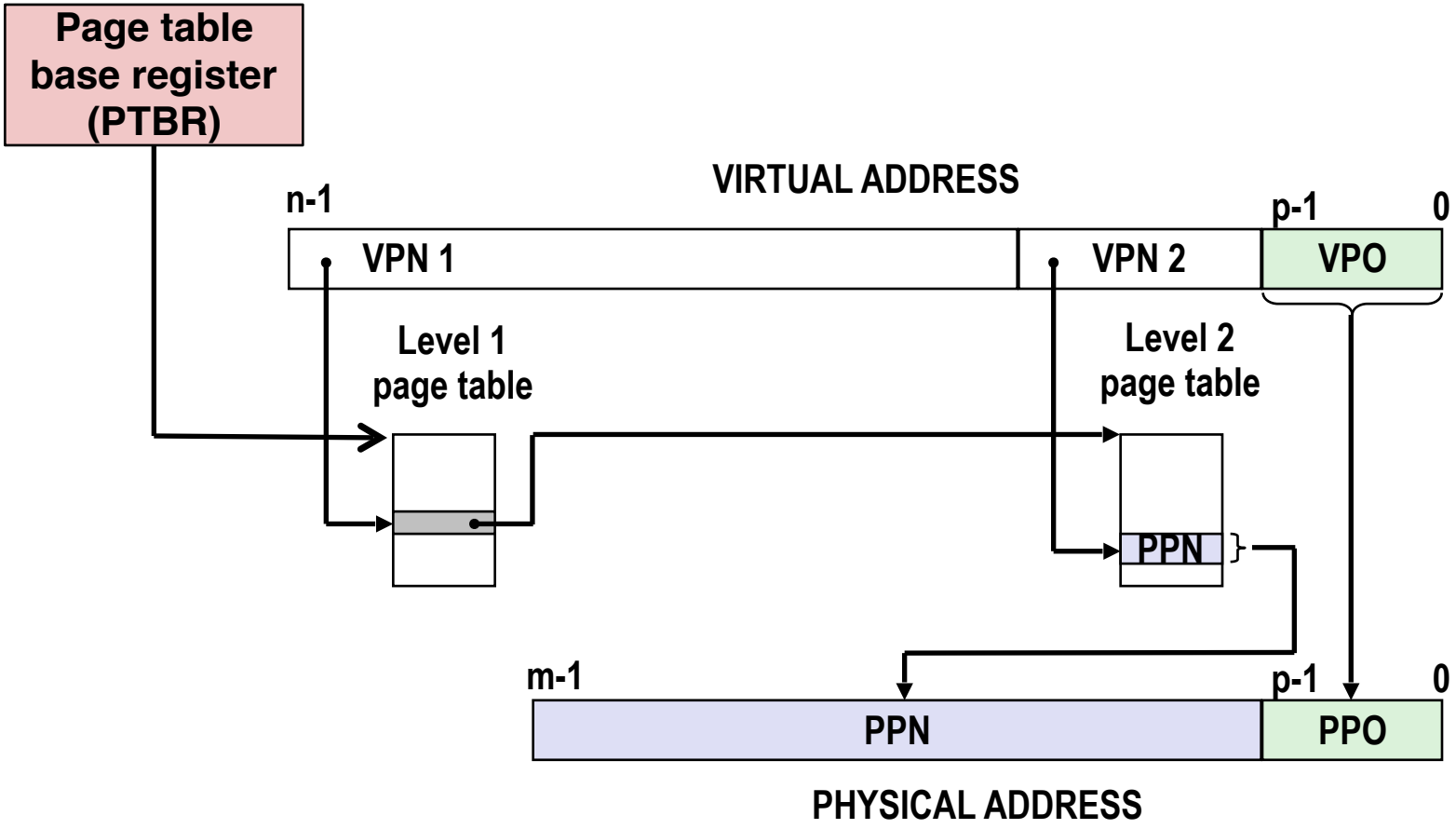
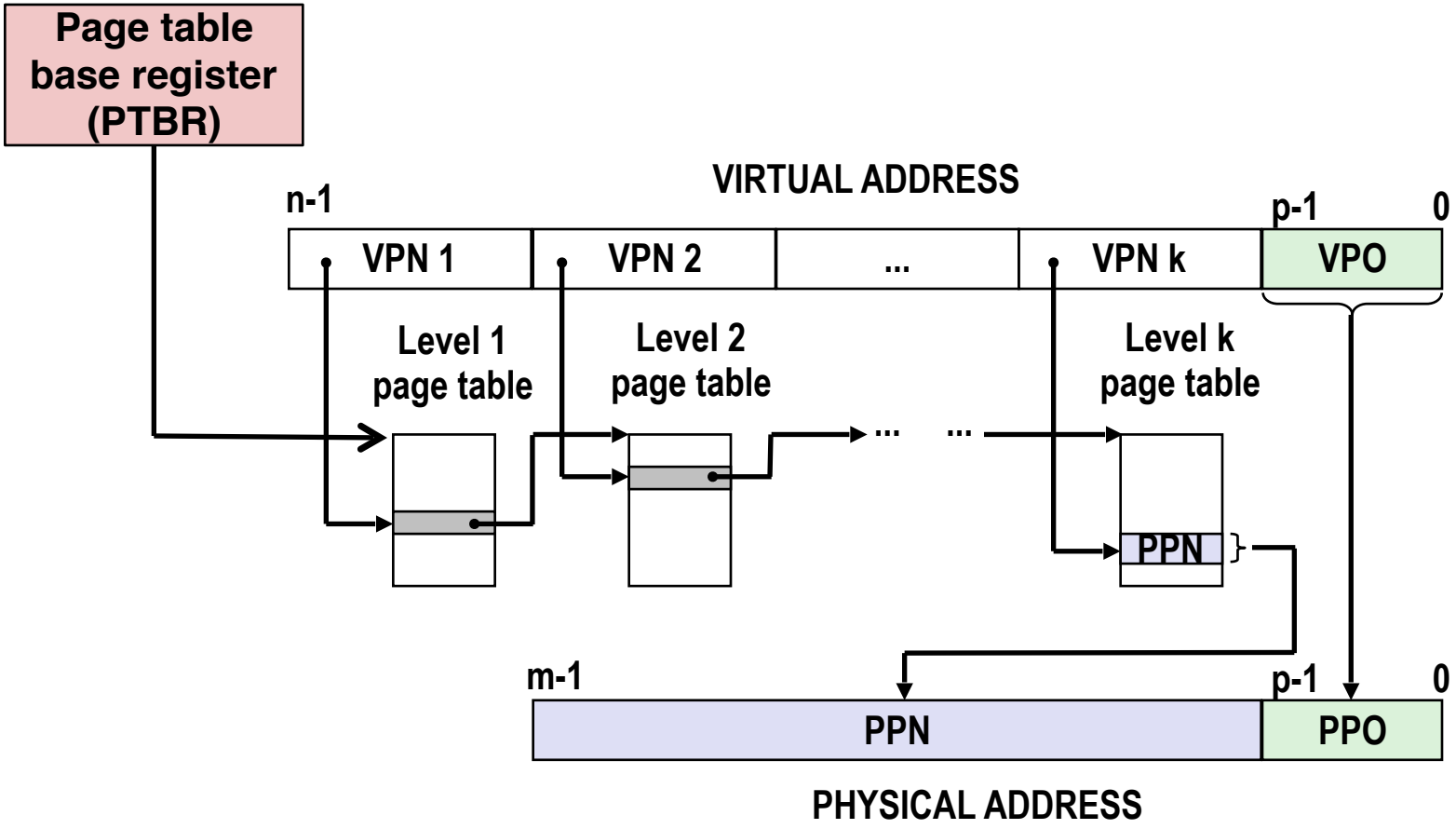


Translating with a k-level Page Table



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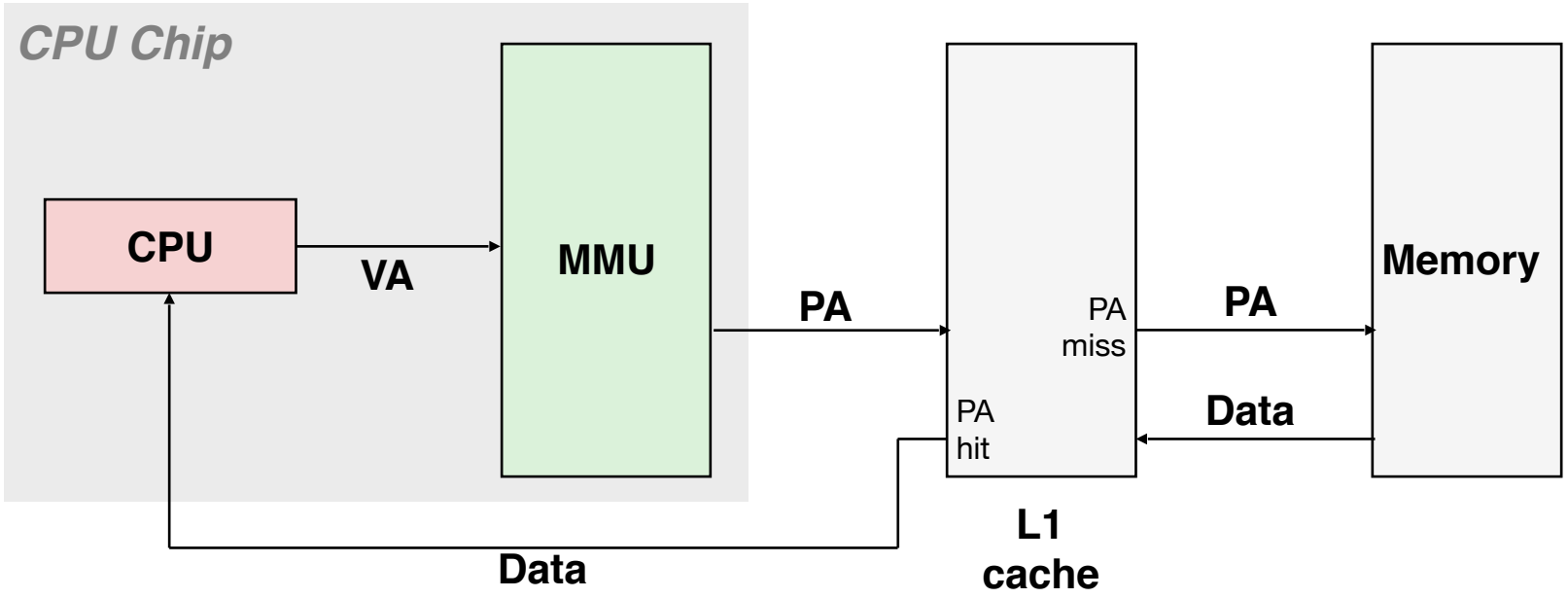
Performance Issue in VM

- Address translation and cache accesses are serialized
  - First translate from VA to PA
  - Then use PA to access cache
  - Slow! Can we speed it up?



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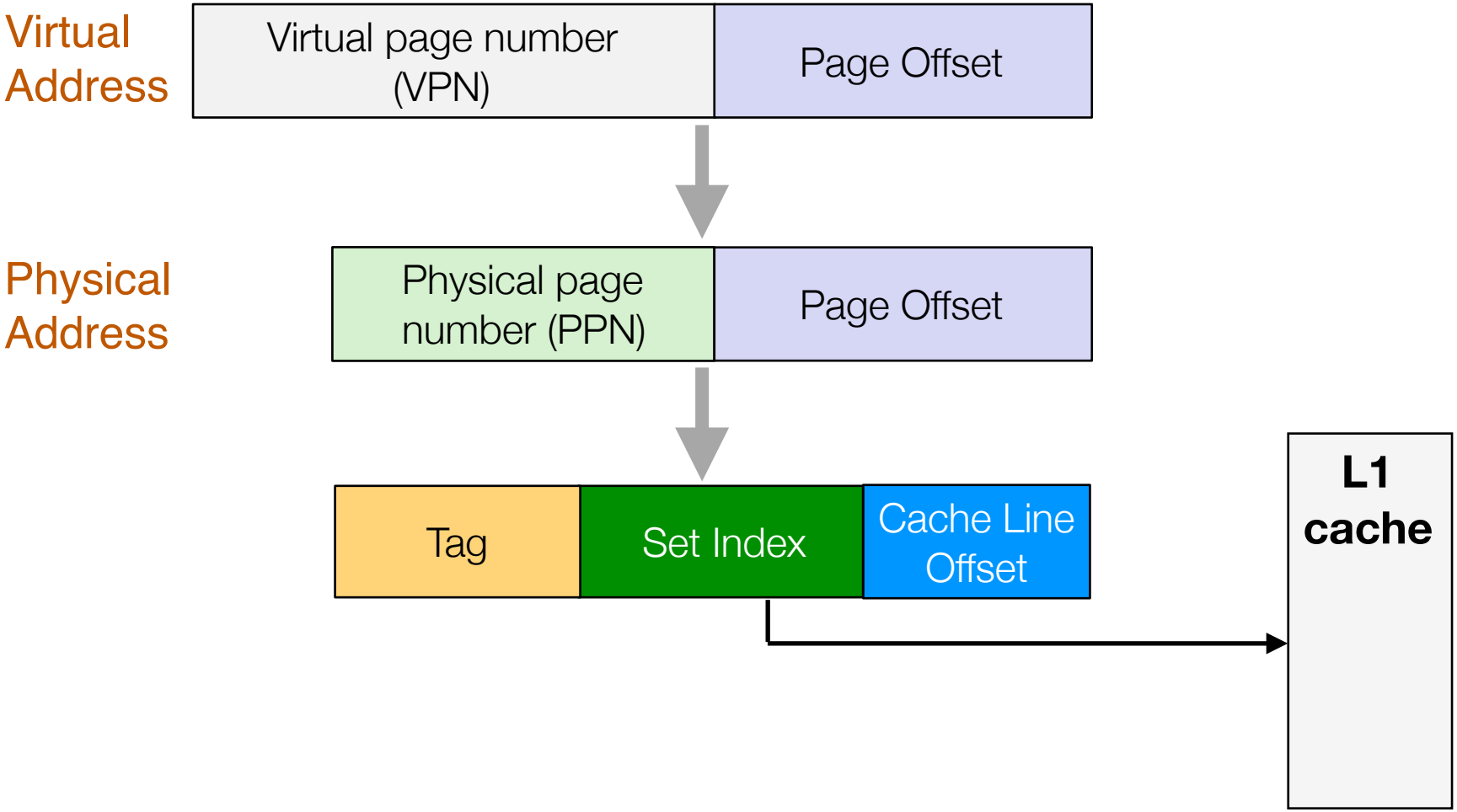

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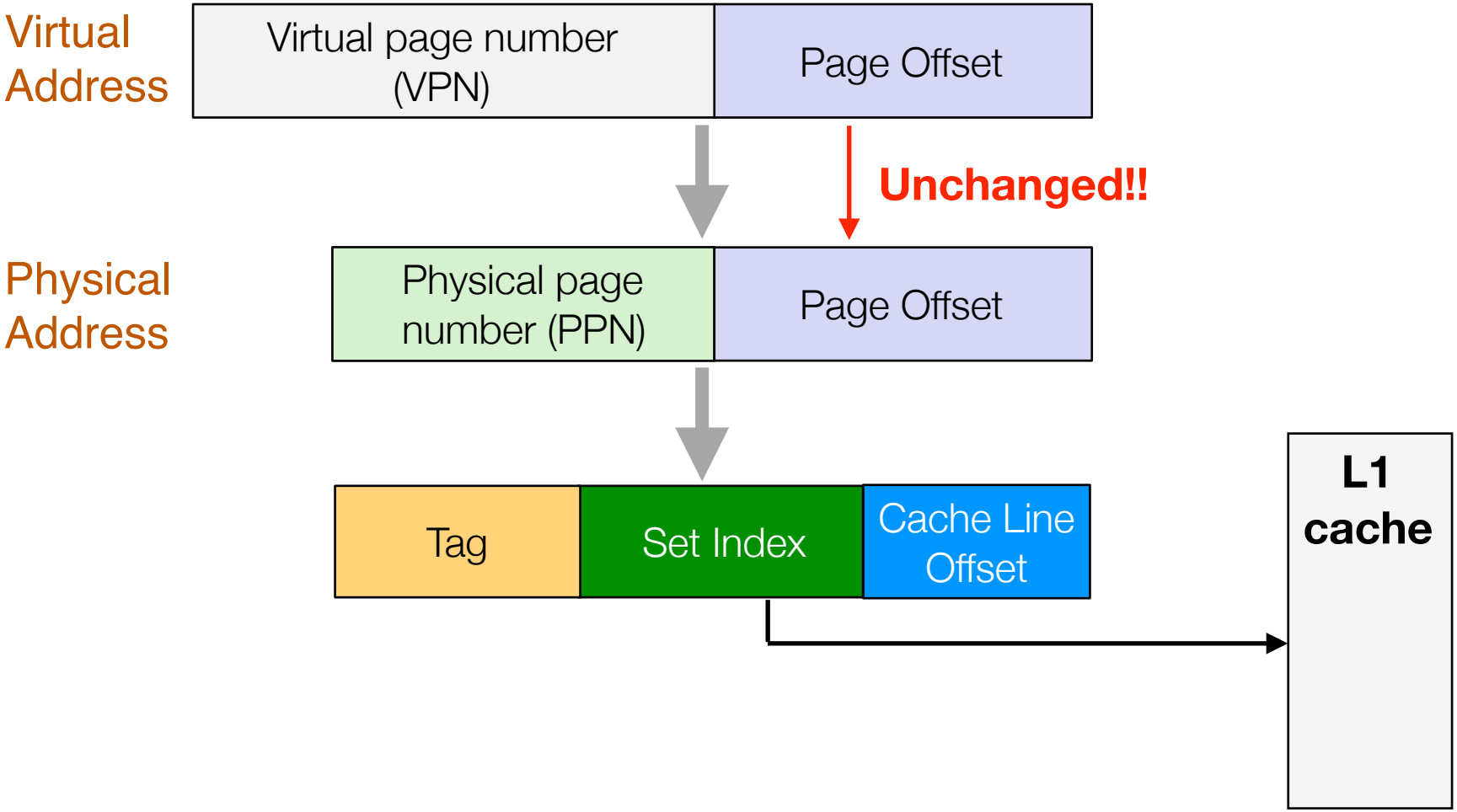

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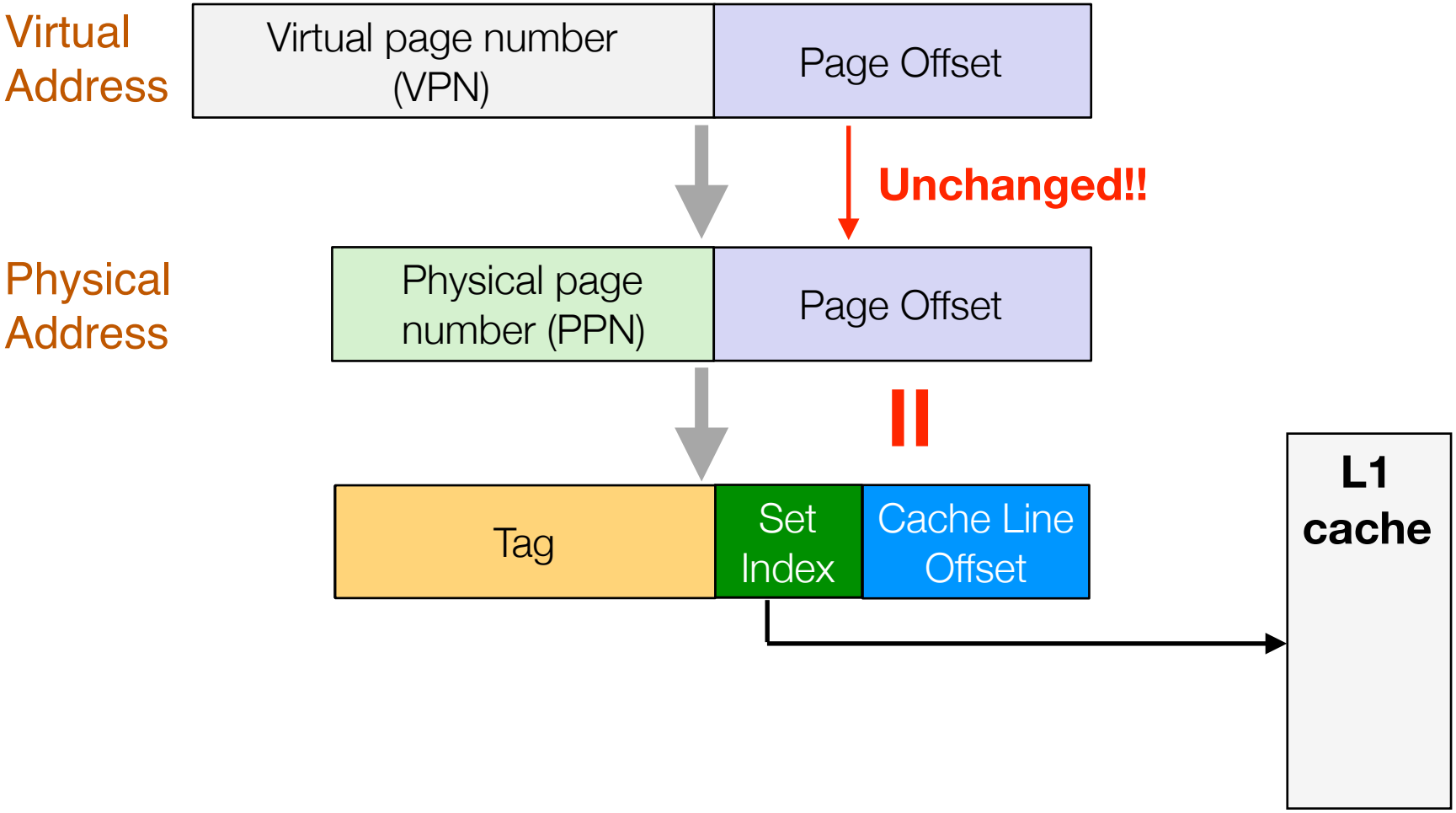

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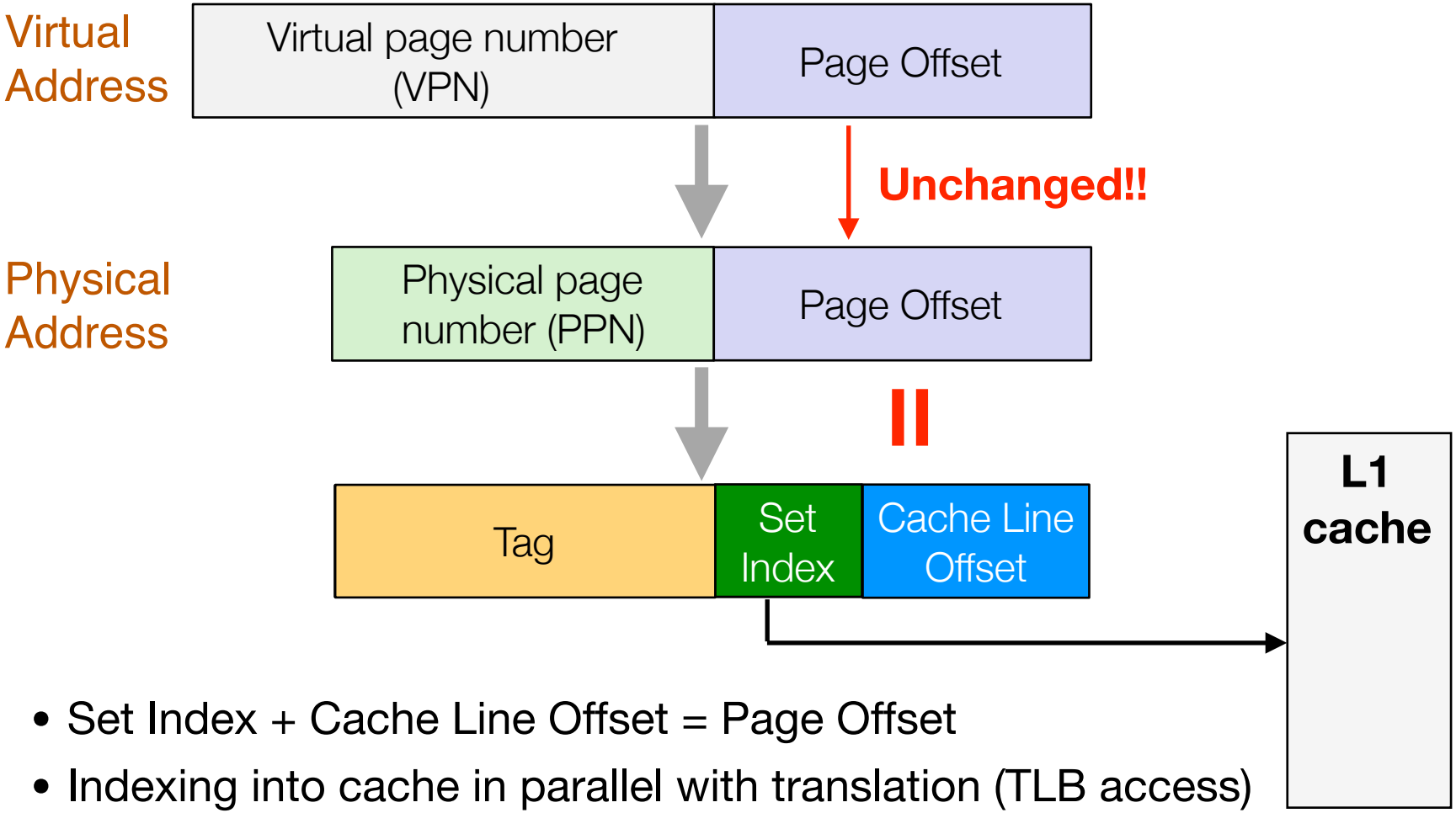

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- Indexing into cache in parallel with translation (TLB access)
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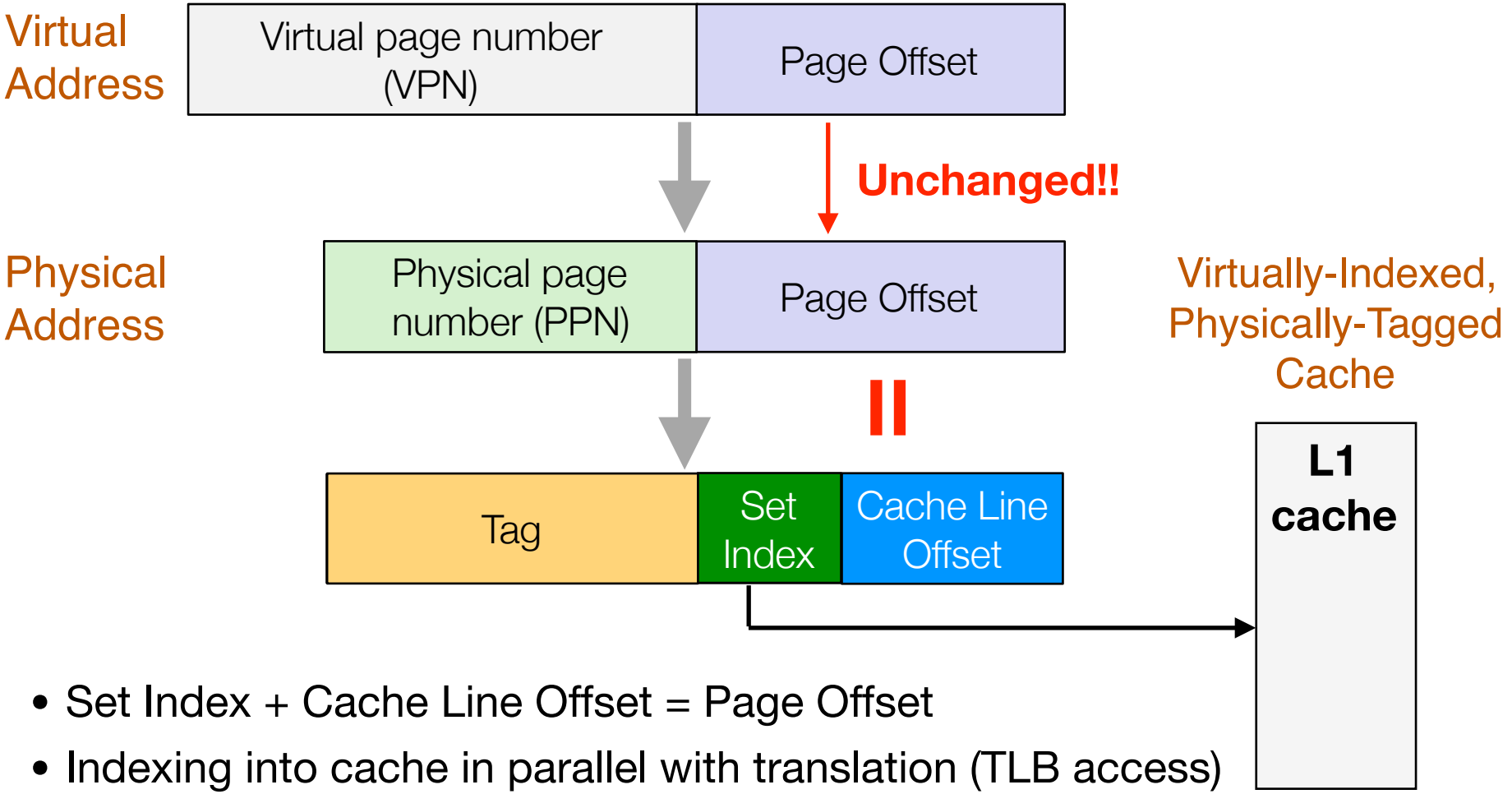

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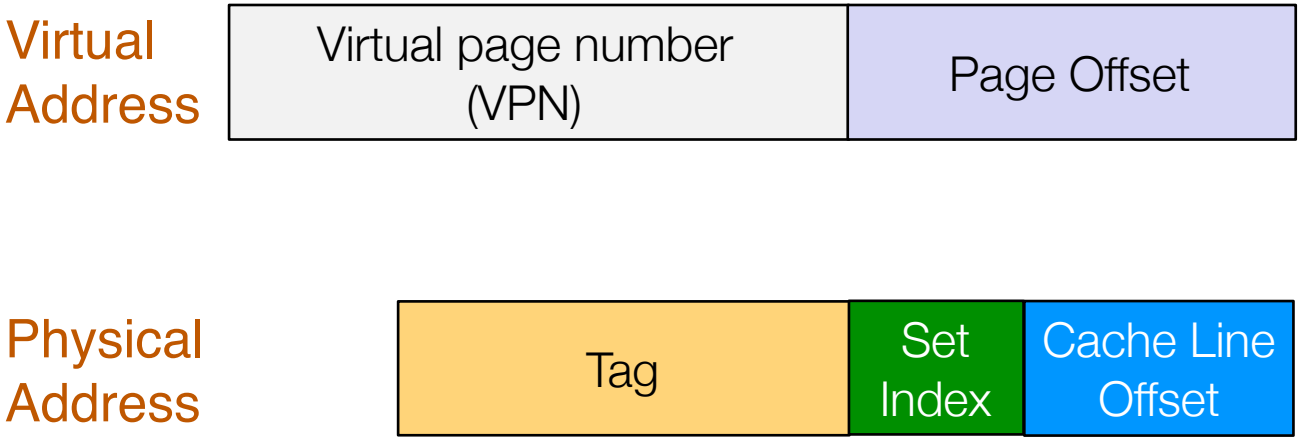

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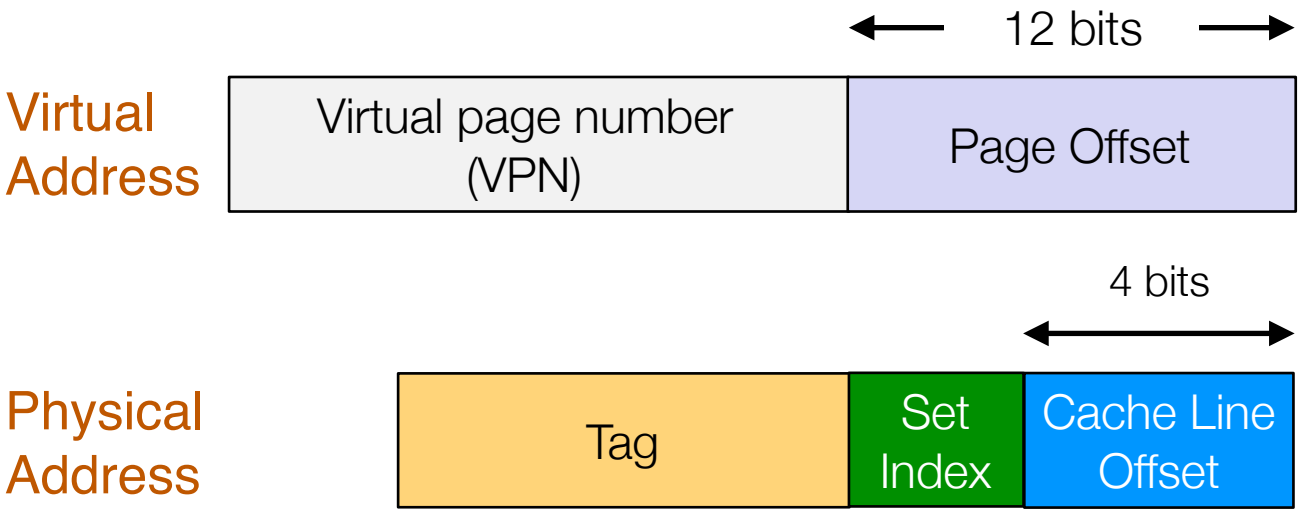

- Assuming 4K page size, cache line size is 16 bytes.

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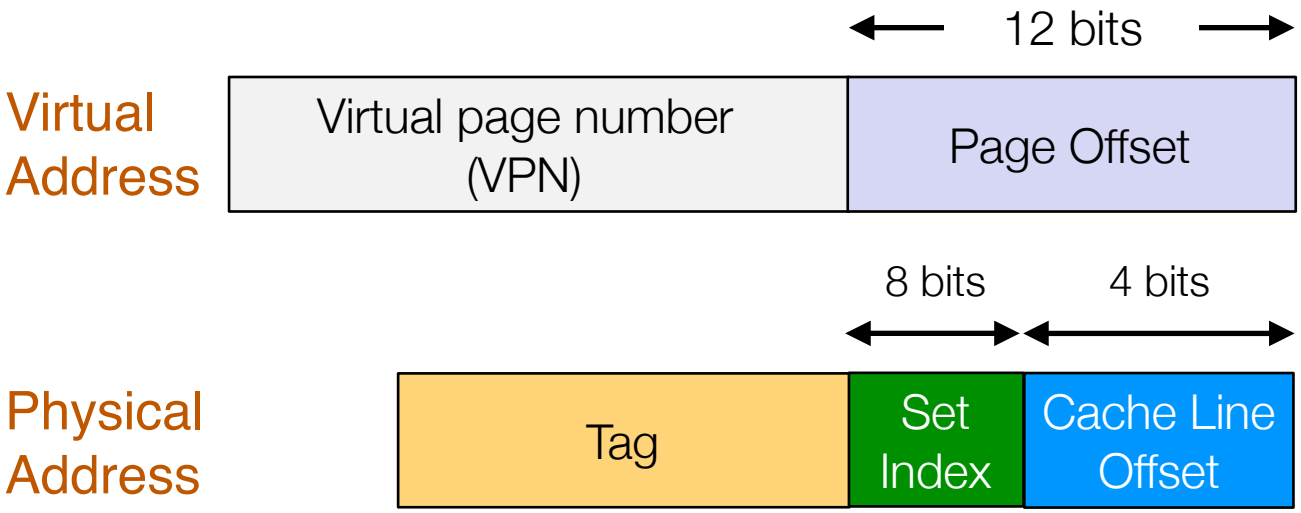

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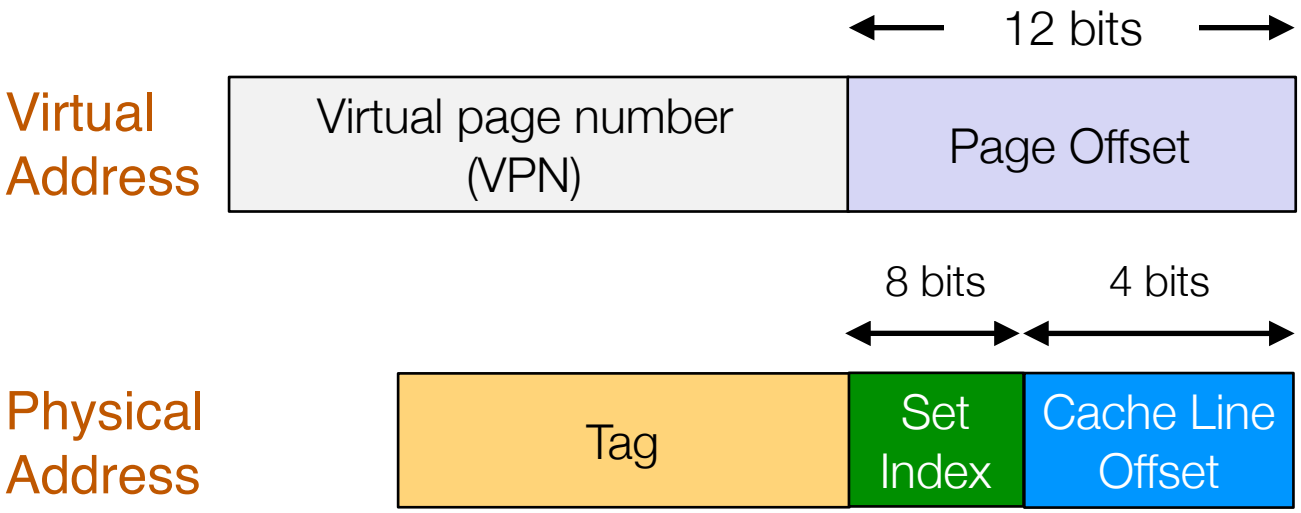

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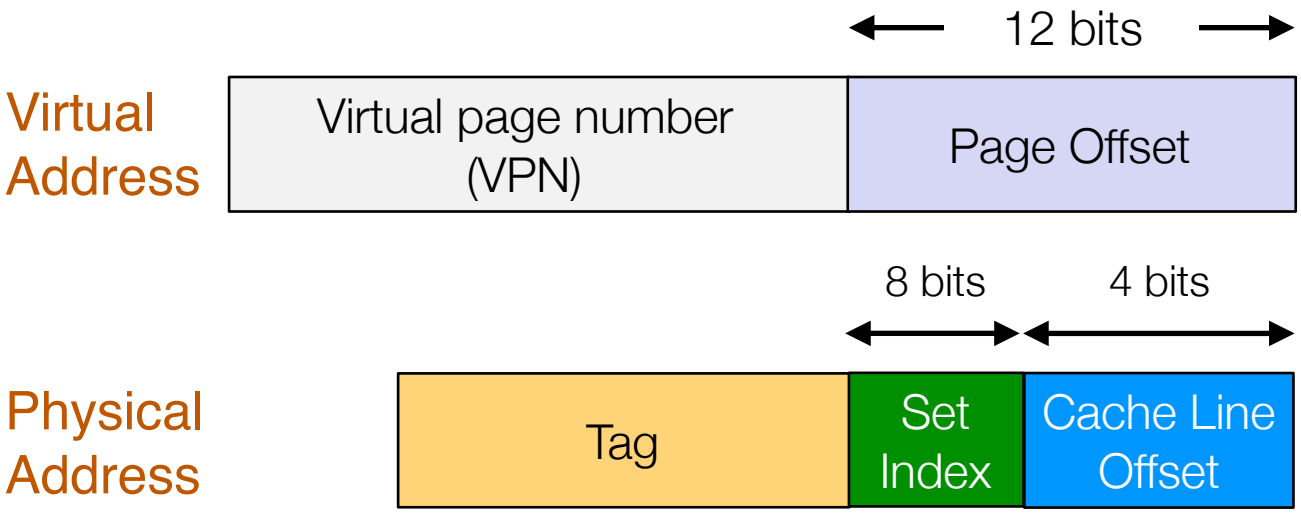

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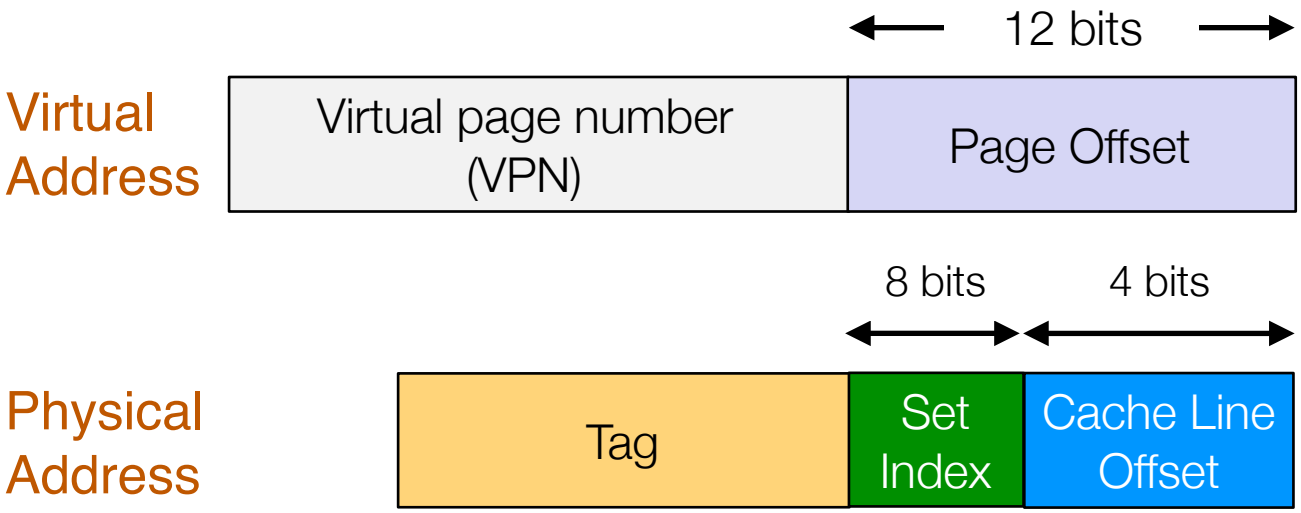

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- Solutions?

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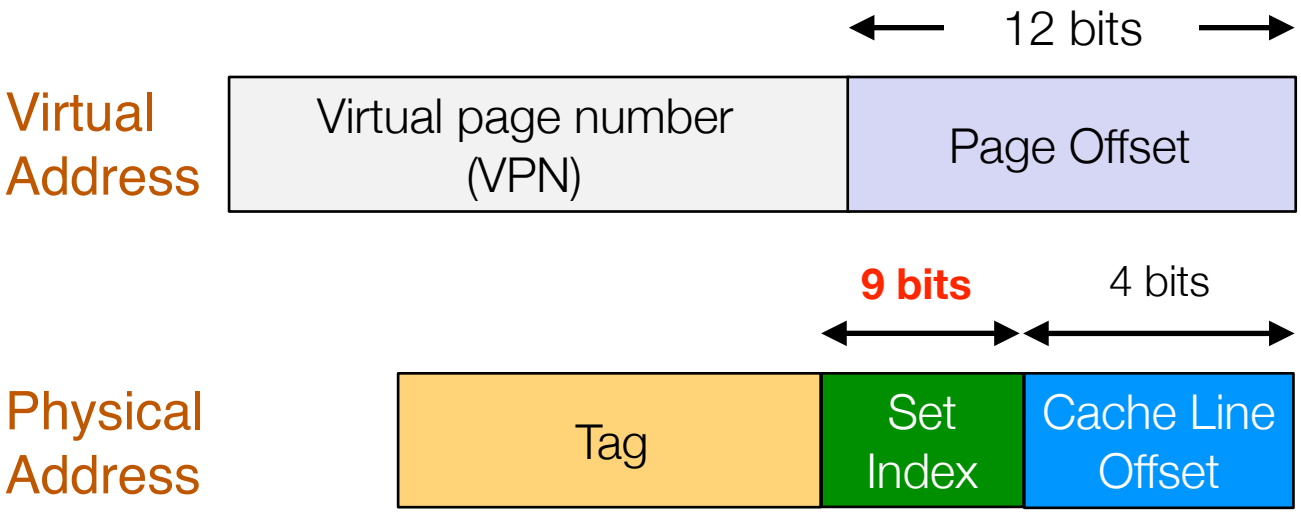

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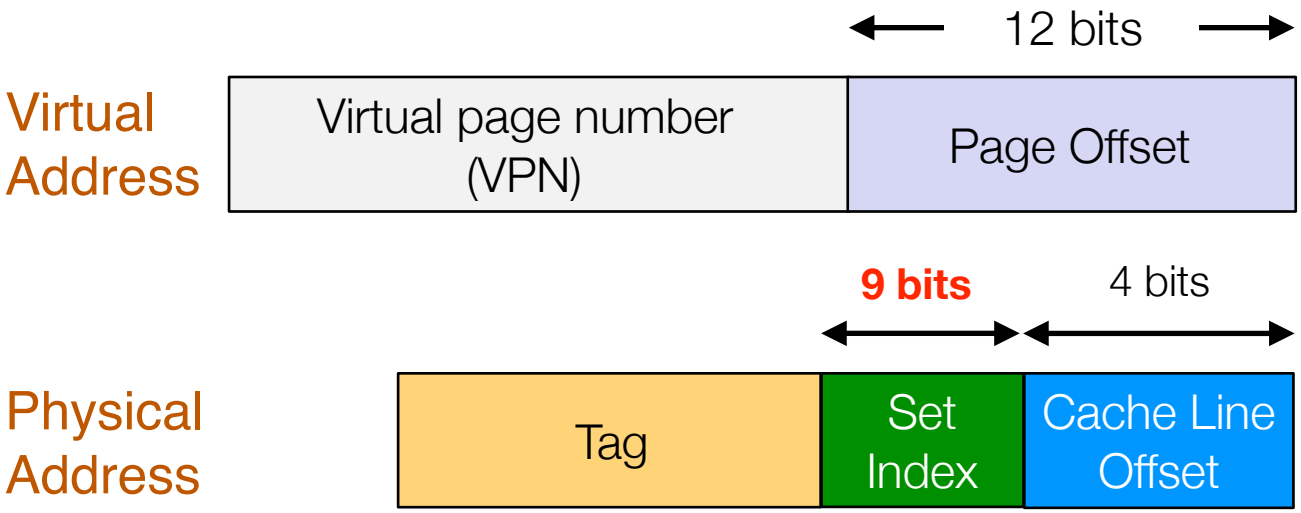

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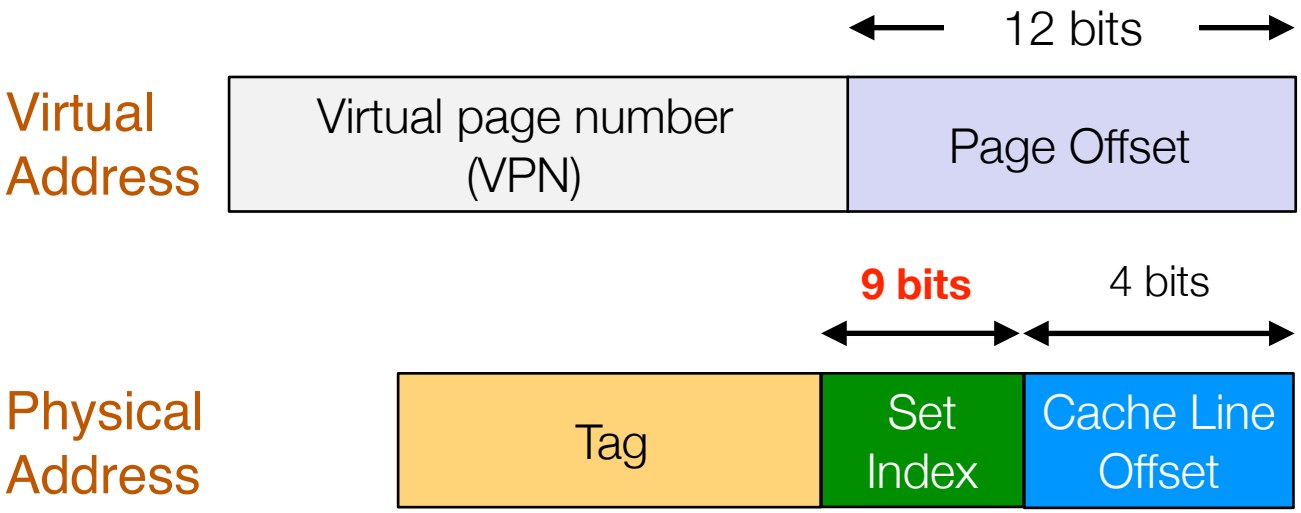

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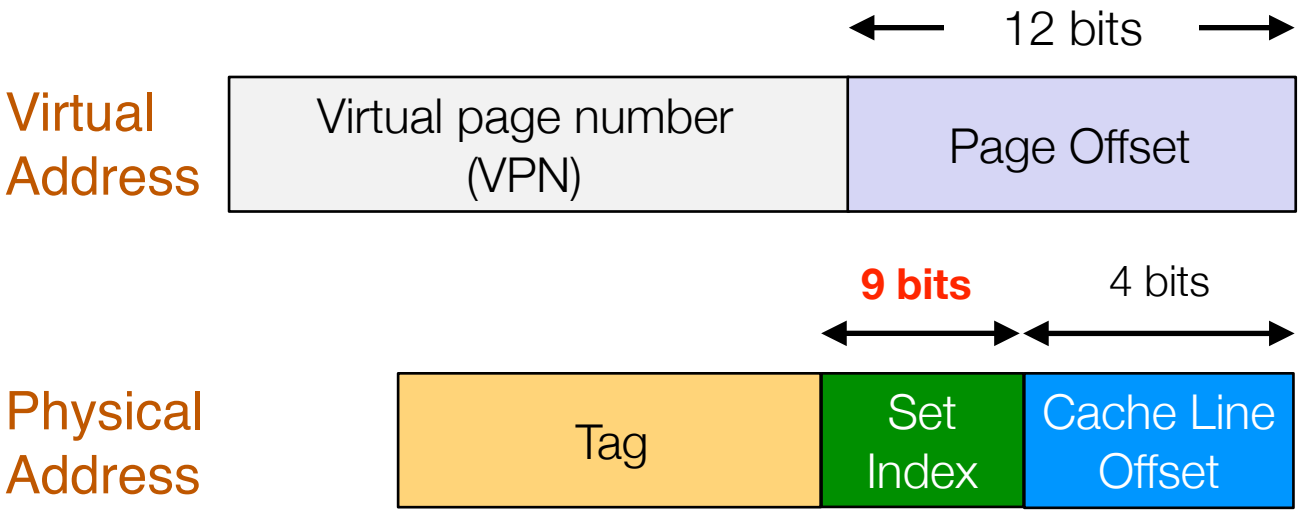

- What if we use 9 bits for Set Index? More Sets now.
- How can this still work???
- The least significant bit in VPN and PPN must be the same
- That is: an even VA must be mapped to an even PA, and an odd VA must be mapped to an odd PA