CSC 252: Computer Organization
Spring 2021: Lecture 11

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Announcement

- Programming assignment 3 is out
  - Details: https://www.cs.rochester.edu/courses/252/spring2021/labs/assignment3.html
  - Due on **March 23**, 11:59 PM
  - You (may still) have 3 slip days

7	8	9	10	11	12	13
		Today				
14	15	16	17	18	19	20
21	22	23	24	25	26	27
		Due		**Mid-term**		

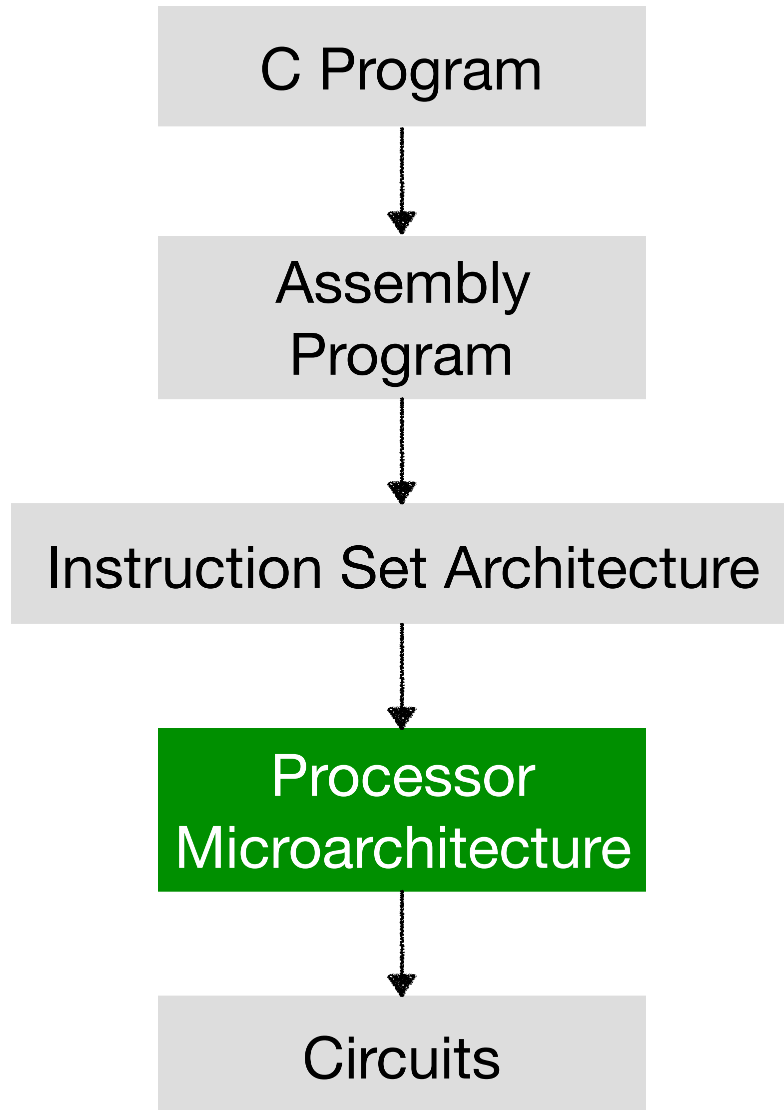
Announcement

- Grades for Lab 1 are posted.
- If you think there are some problems
  - Take a deep breath
  - Tell yourself that the teaching staff like you, not the opposite
  - Email Grad TAs and explain to them why you should get more points

Announcement

- Programming assignment 3 is in x86 assembly language. Seek help from TAs.
- TAs are best positioned to answer your questions about programming assignments!!!
- Programming assignments do NOT repeat the lecture materials. They ask you to synthesize what you have learned from the lectures and work out something new.

So far in 252…

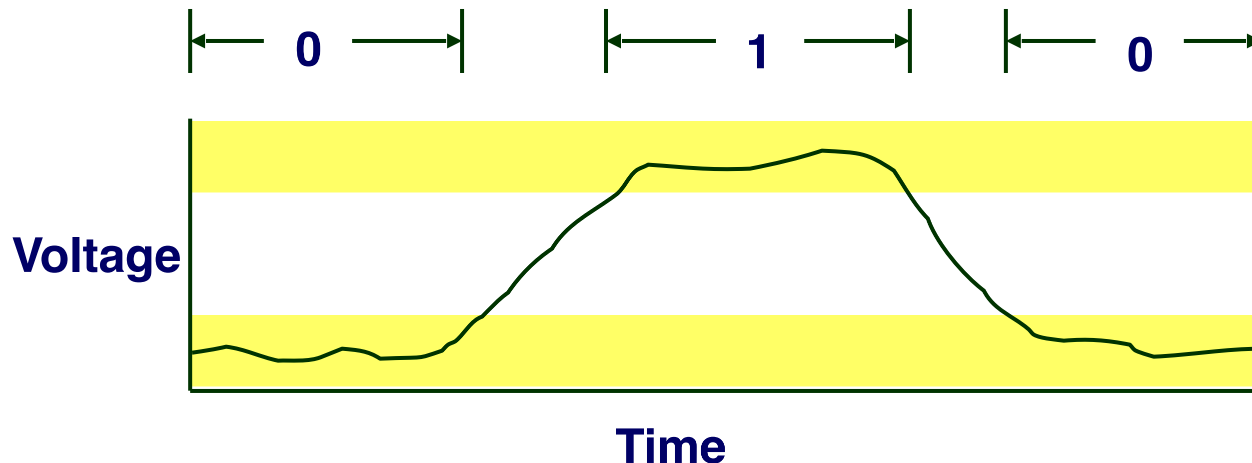


Today: Circuits Basics

- Basics
- Circuits for computations
- Circuits for storing data

Overview of Circuit-Level Design

- Fundamental Hardware Requirements
  - Communication: How to get values from one place to another. Mainly three electrical **wires**.
  - Computation: **transistors**. Combinational logic.
  - Storage: **transistors**. Sequential logic.
- Circuit design is often abstracted as logic design



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- Transistors
- Circuits for computations
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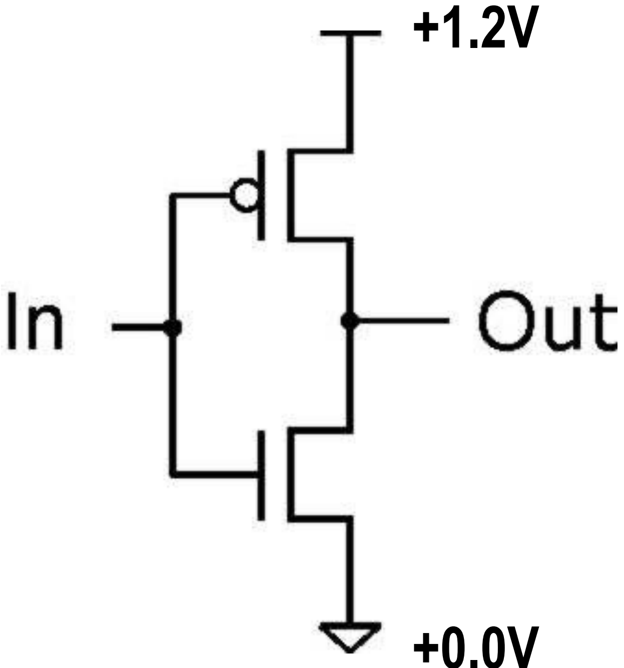
Inverter (NOT Gate)



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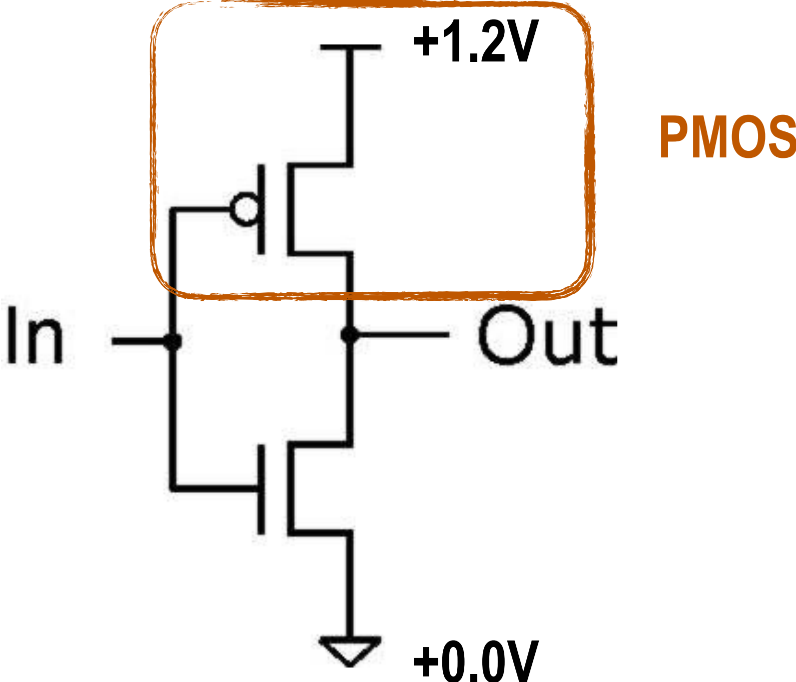

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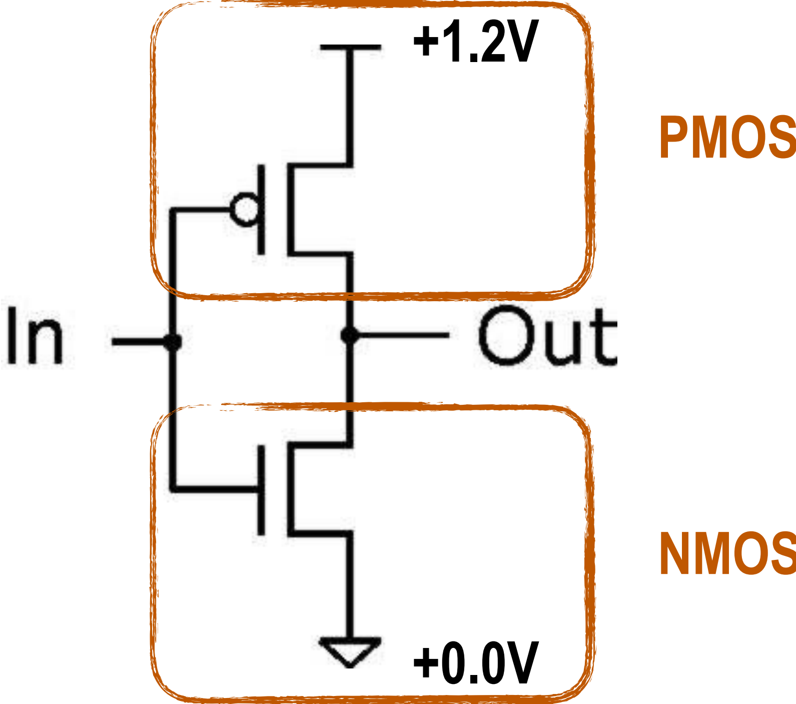
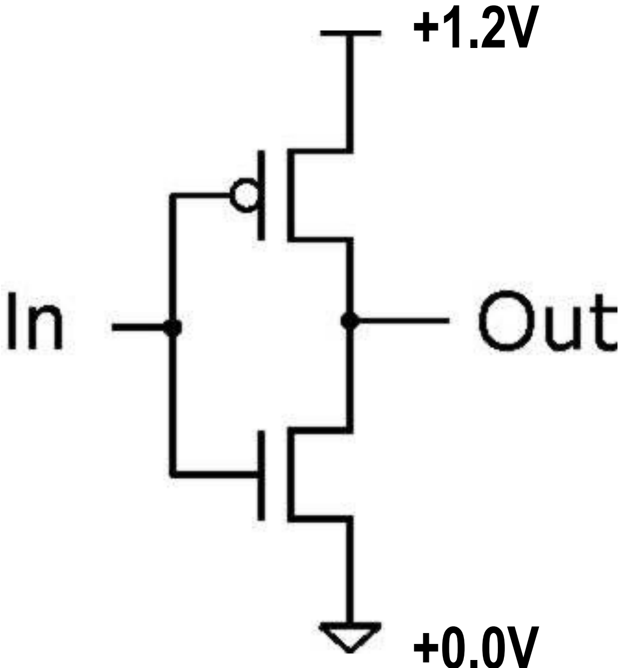
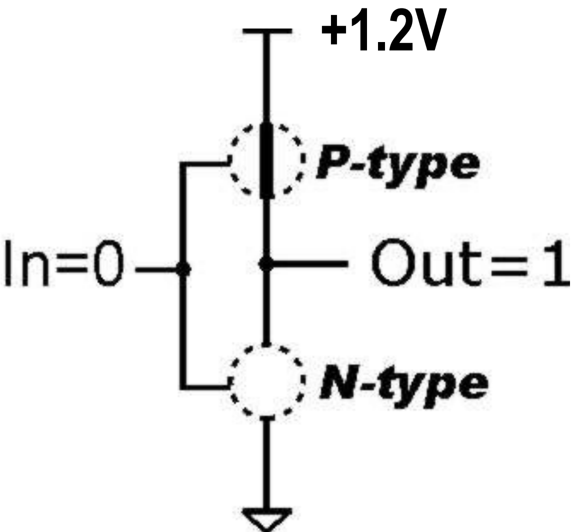


PMOS

NMOS

Inverter (NOT Gate)





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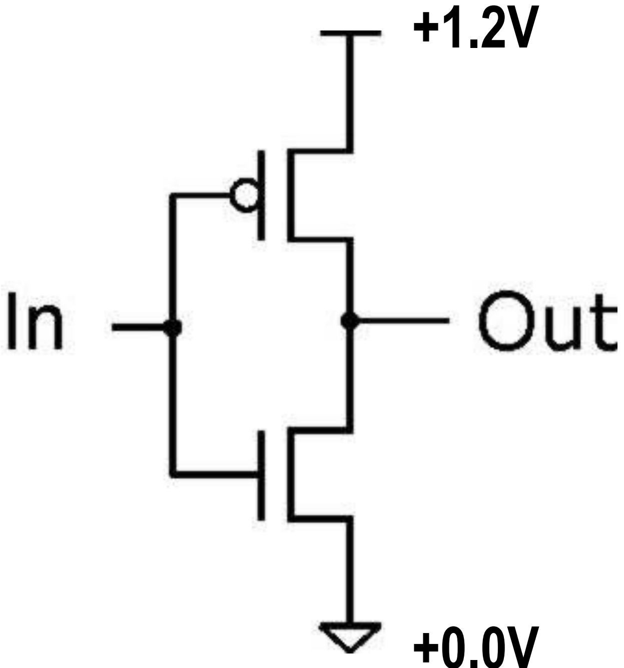

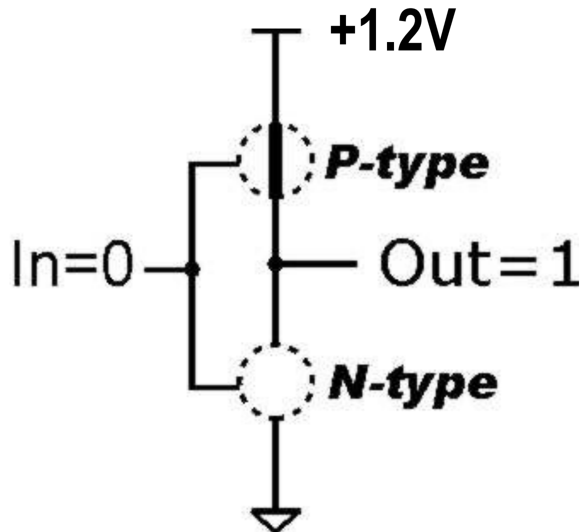

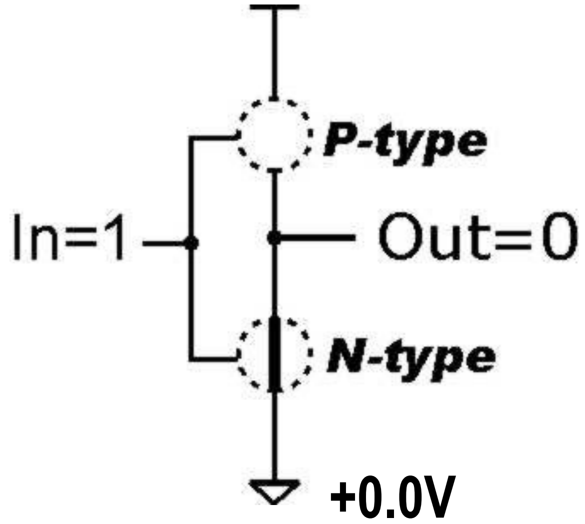

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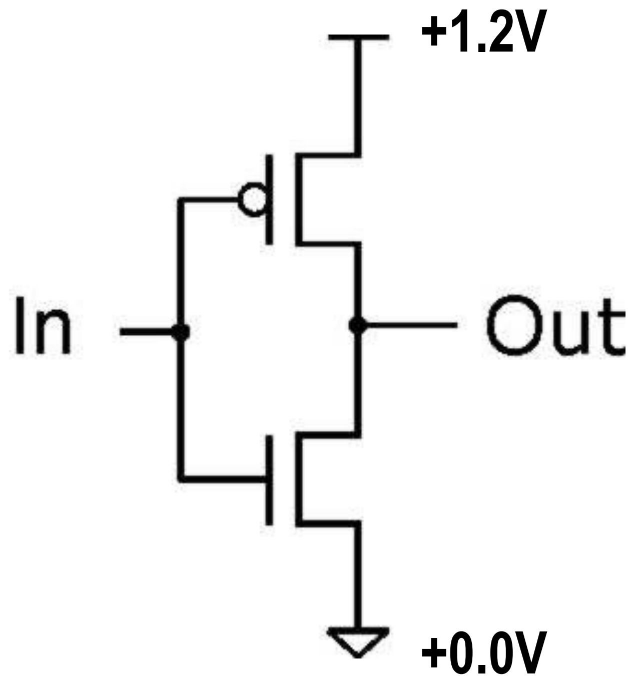
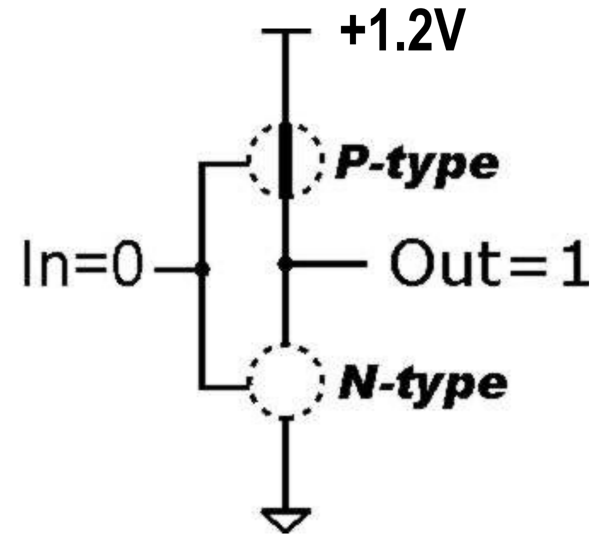
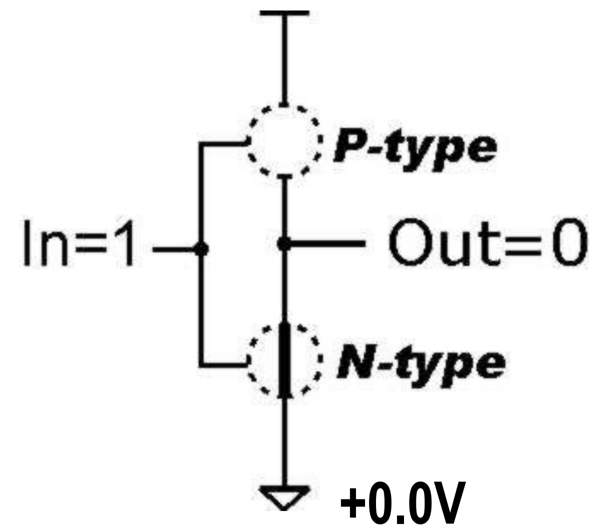
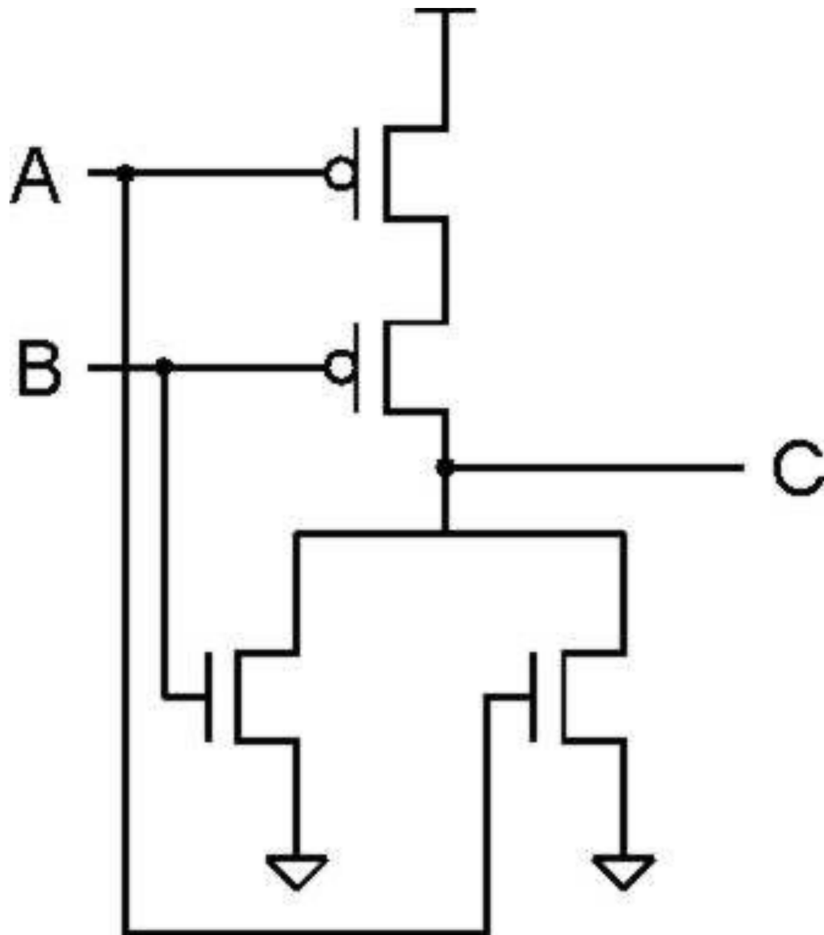


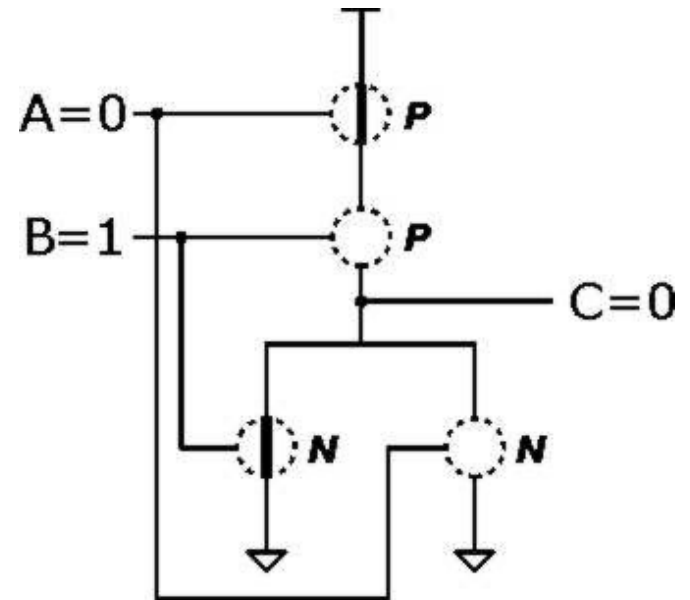


In	Out
0	1
1	0



NOR Gate (NOT + OR)

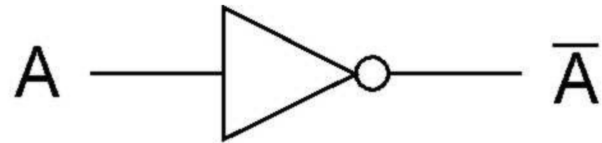


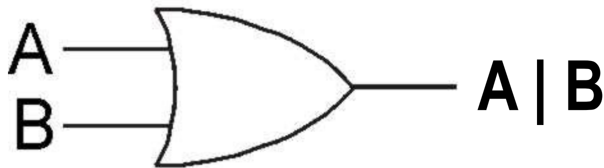


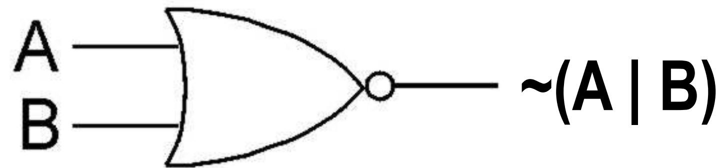
A	B	C
0	0	1
0	1	0
1	0	0
1	1	0

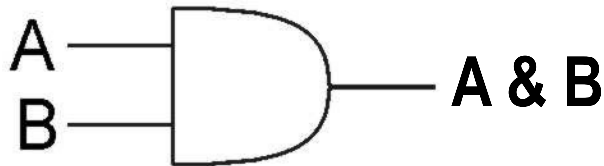
Note: Serial structure on top, parallel on bottom.

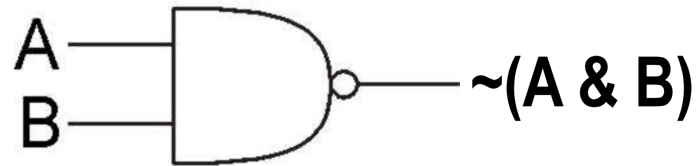
Basic Logic Gates



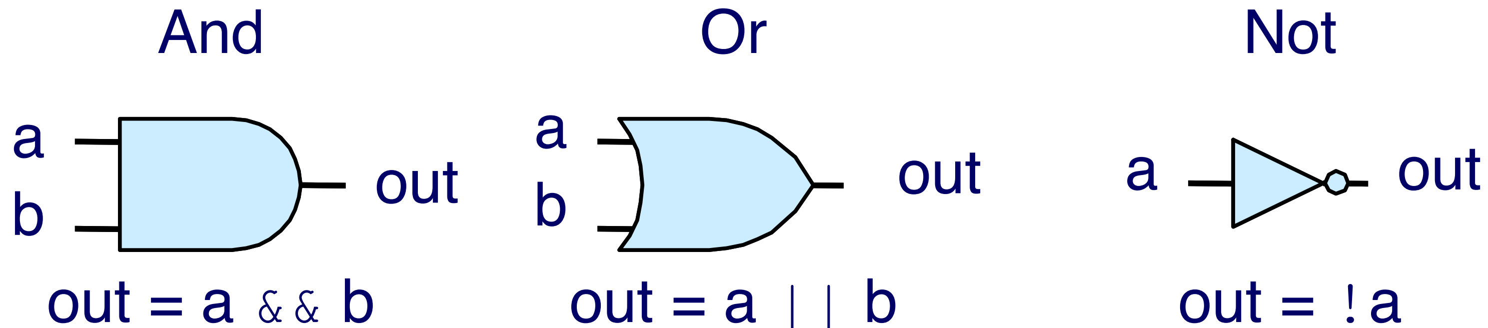




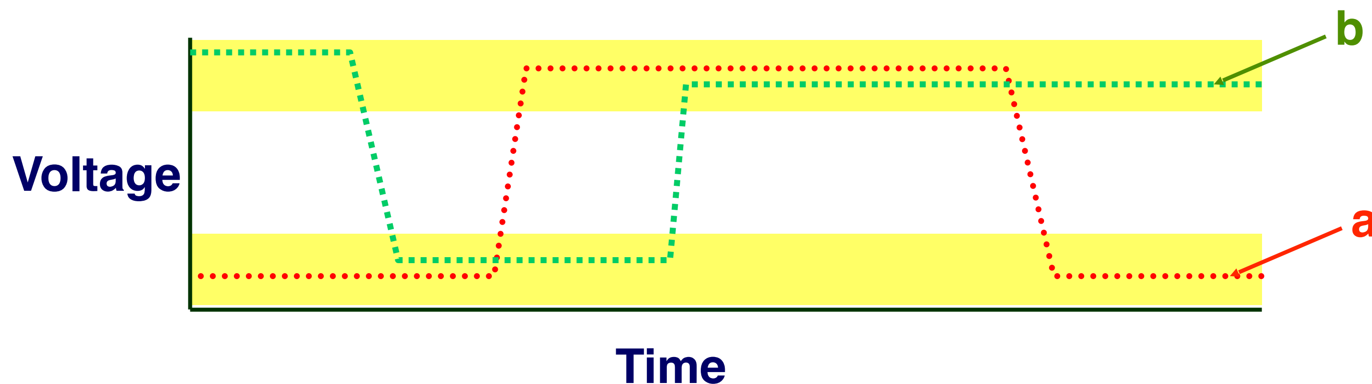




Computing with Logic Gates



- Outputs are Boolean functions of inputs
- Respond continuously to changes in inputs with some small delay
- Different gates have different delays (b/c different transistor combinations)



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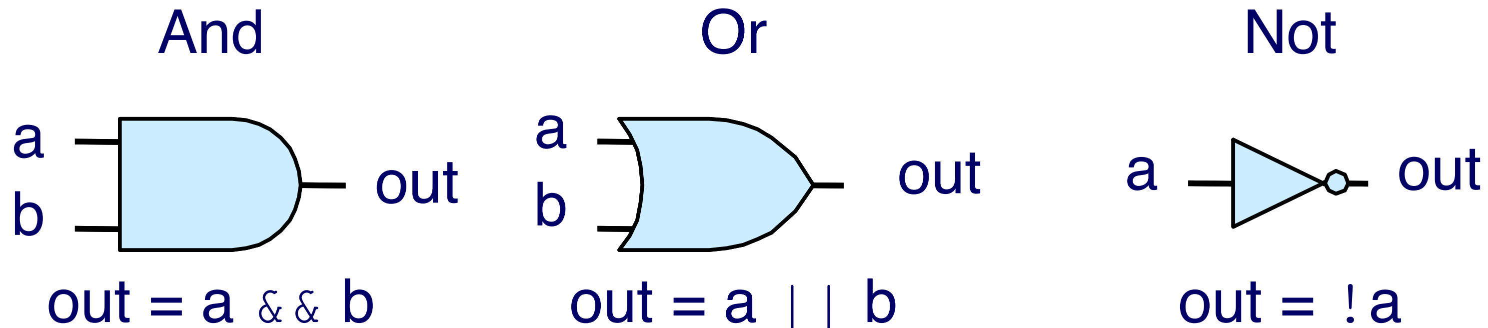

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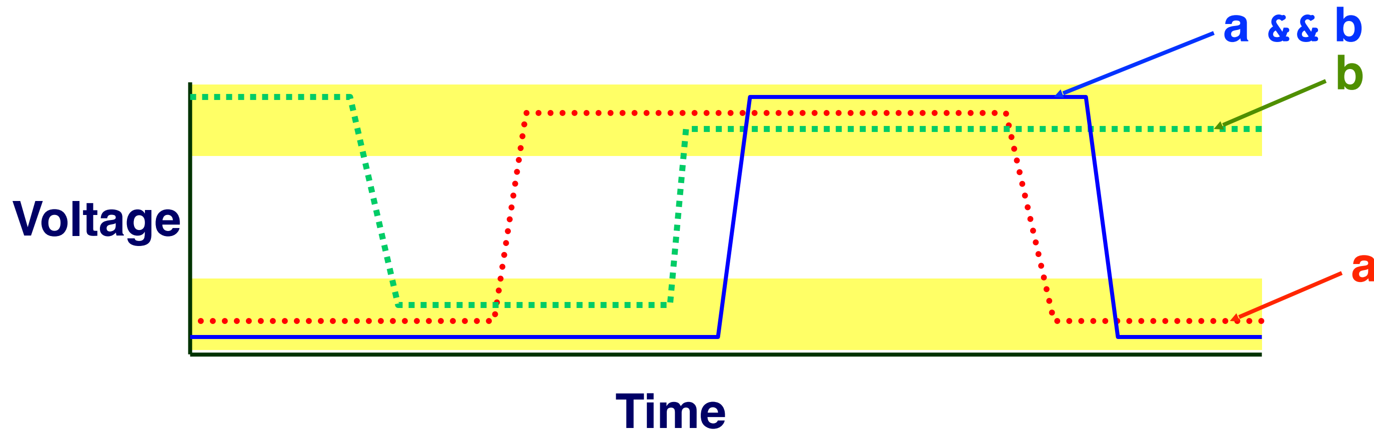

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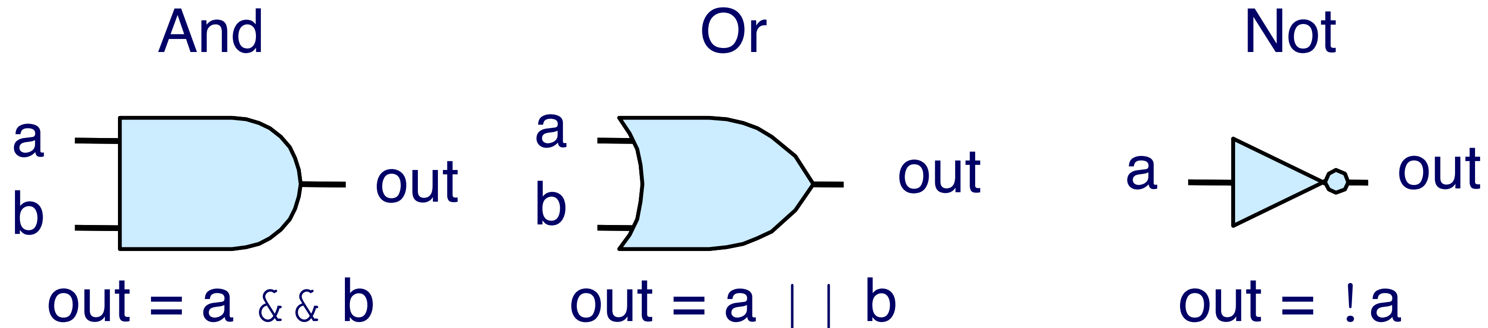

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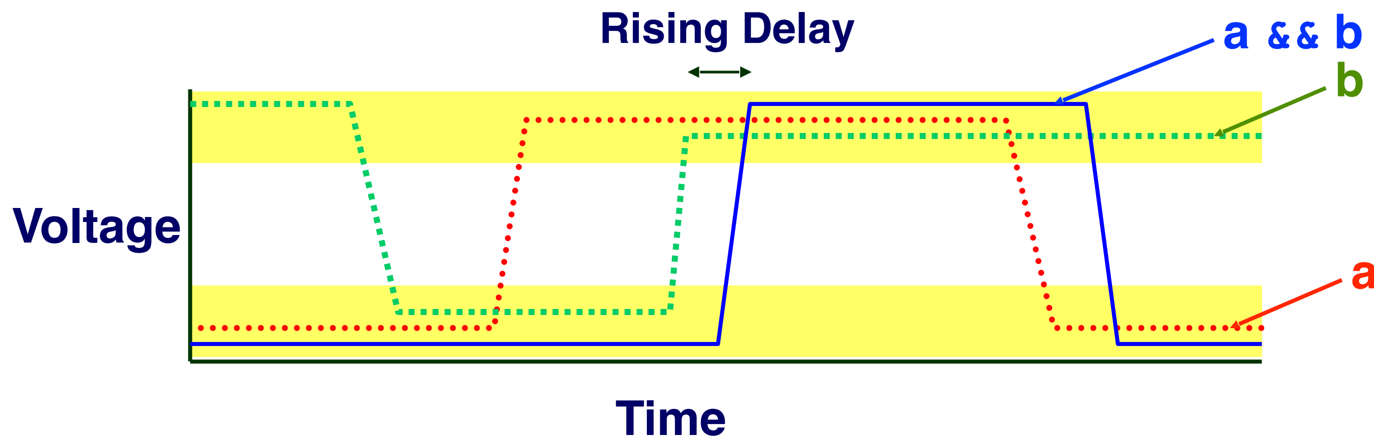

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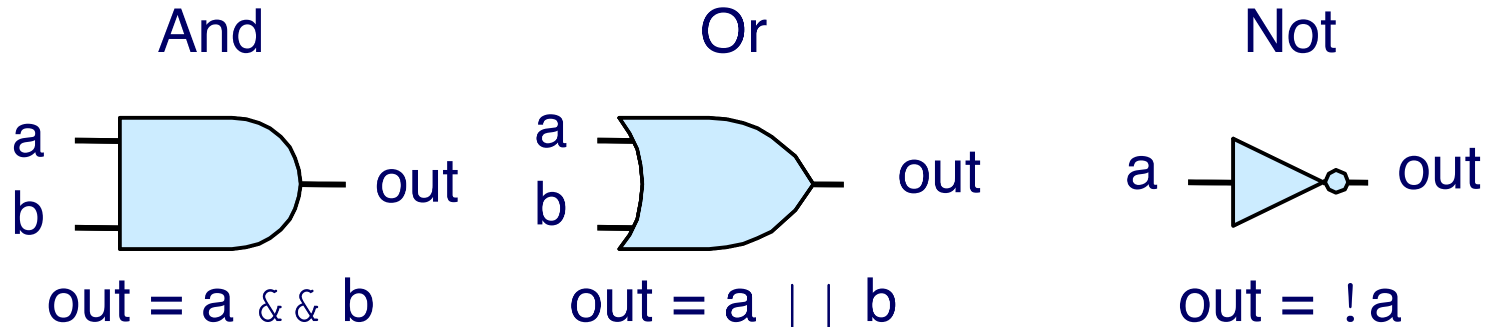

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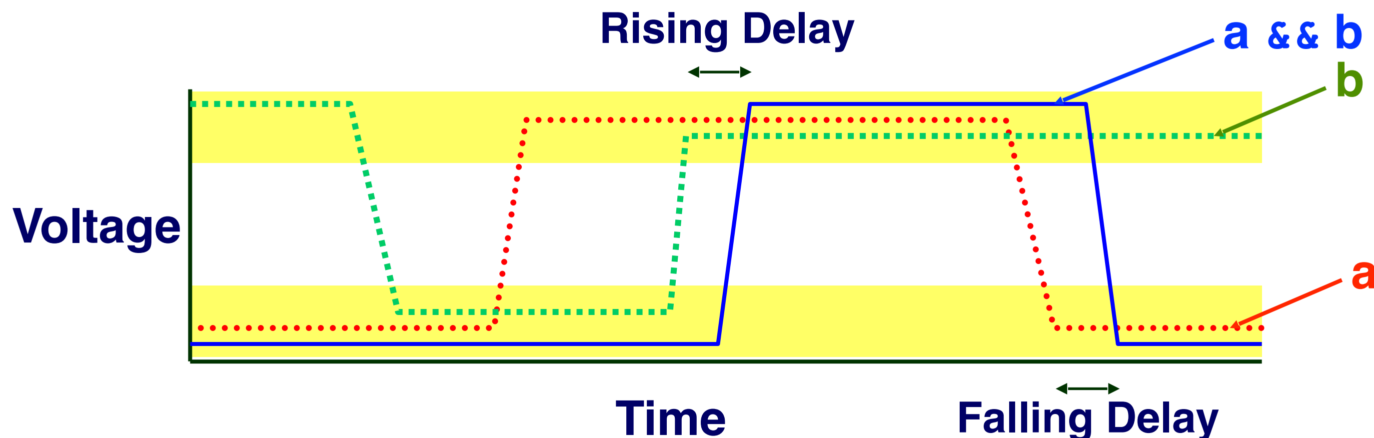
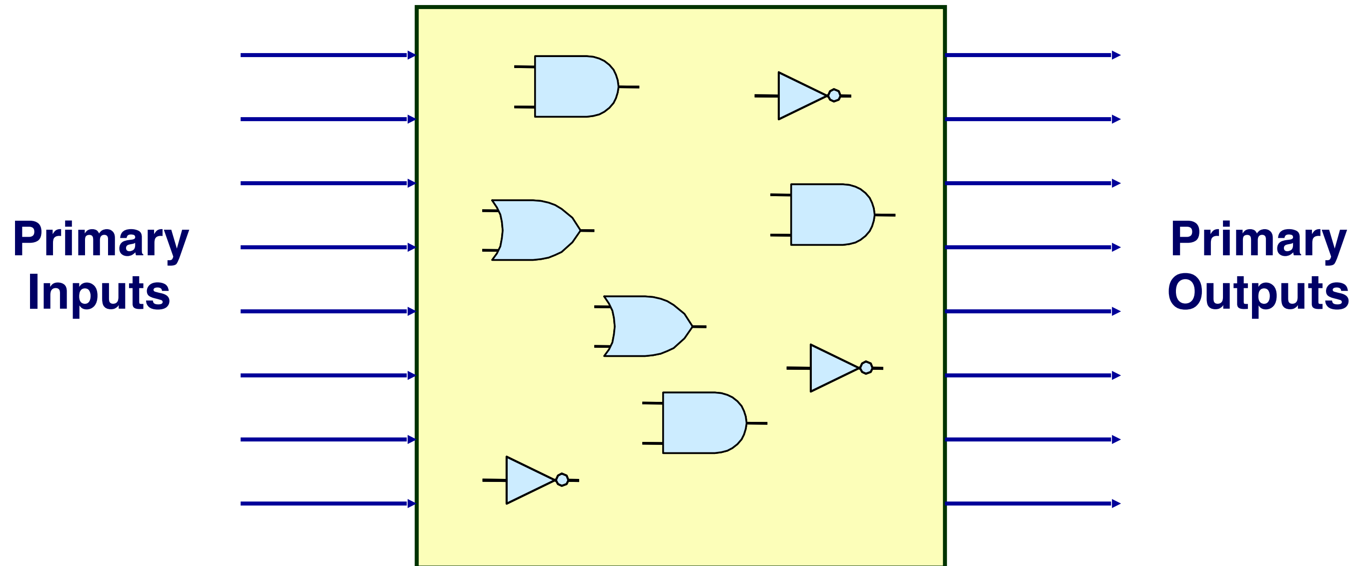


Combinational Circuits



- A Network of Logic Gates
  - Continuously responds to changes on primary inputs
  - Primary outputs become (**after some delay**) Boolean functions of primary inputs

Bit Equality

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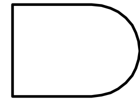

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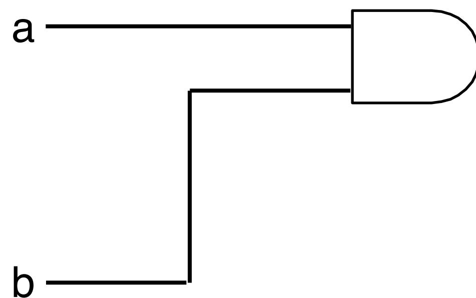

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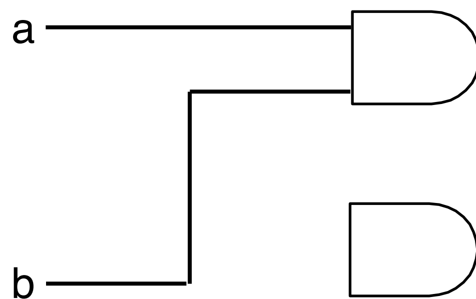

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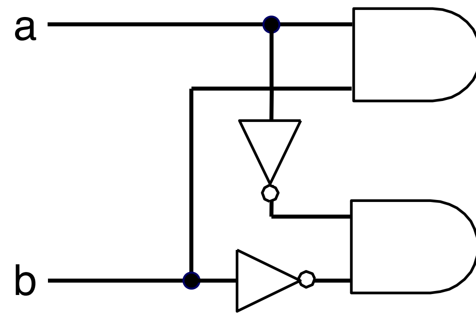

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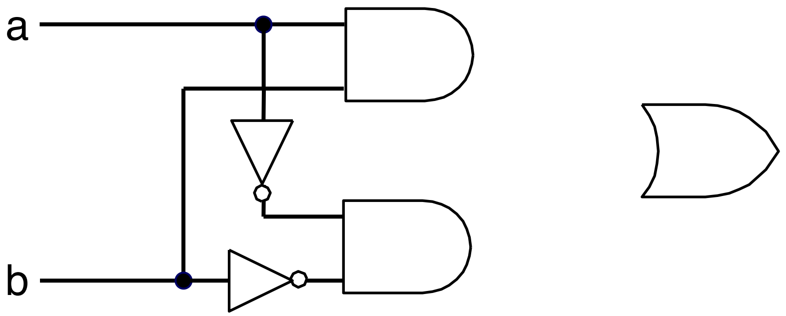

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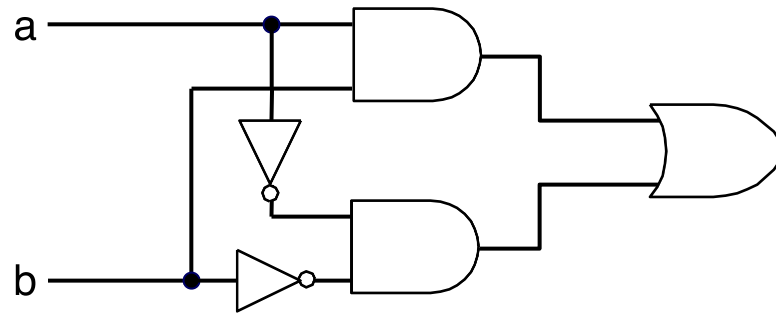

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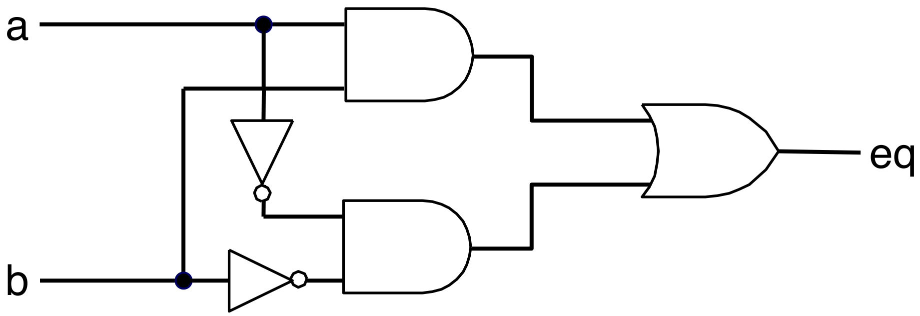

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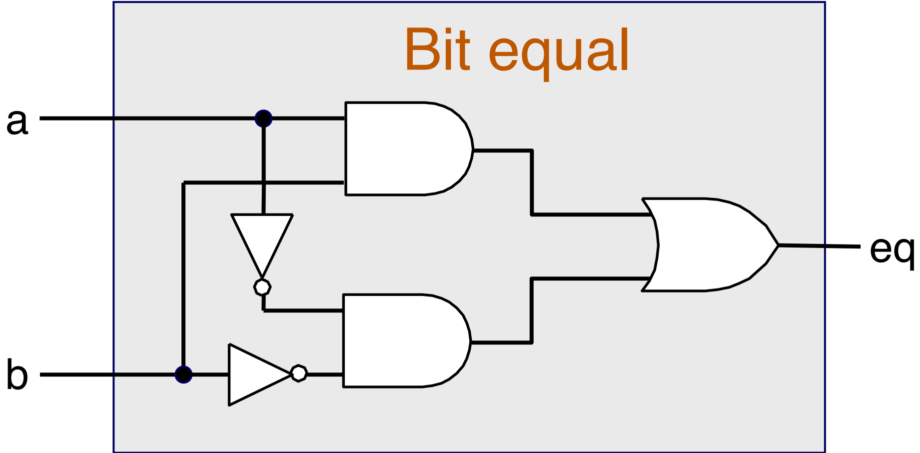
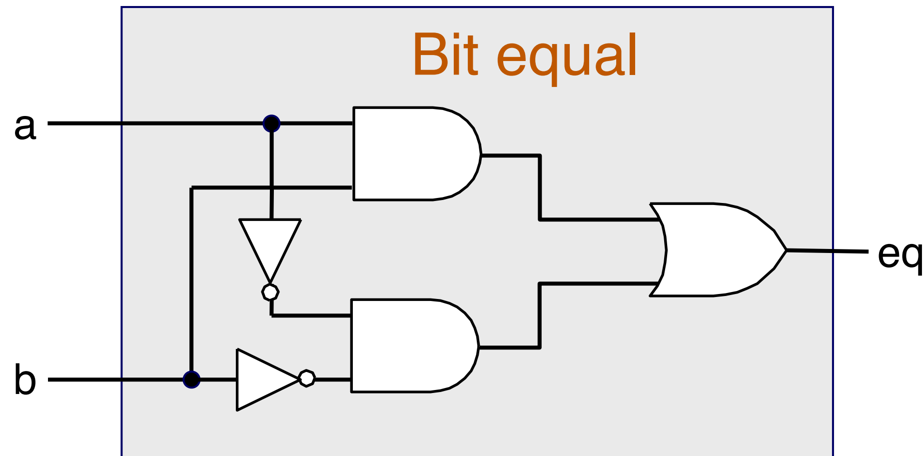


Delay of Bit Equal Circuit



- What’s the delay of this bit equal circuit?
    - Assuming 1-input NOT takes 1 unit of time, 2-input AND takes 4.3, and 2-input OR takes 4.7

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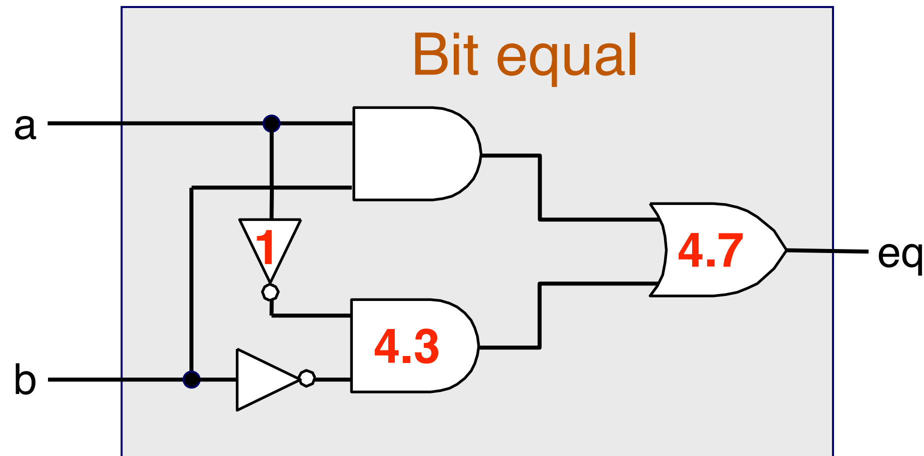

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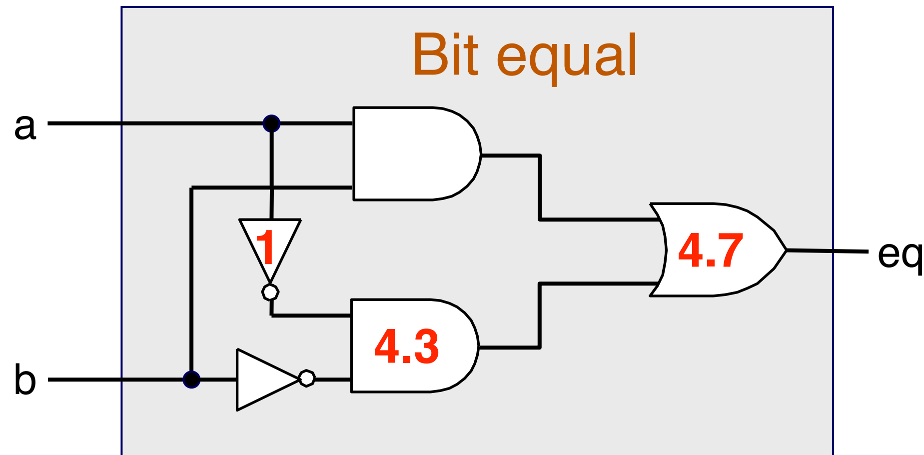

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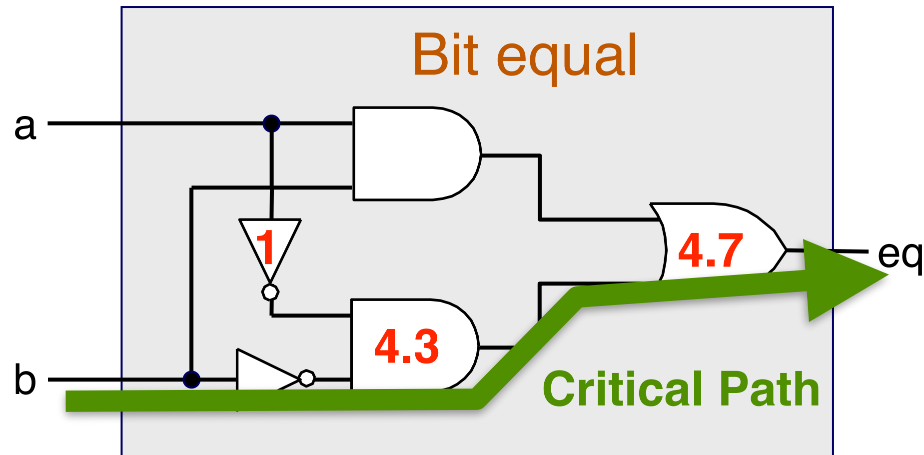

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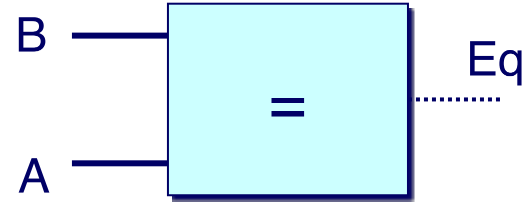
64-bit Equality



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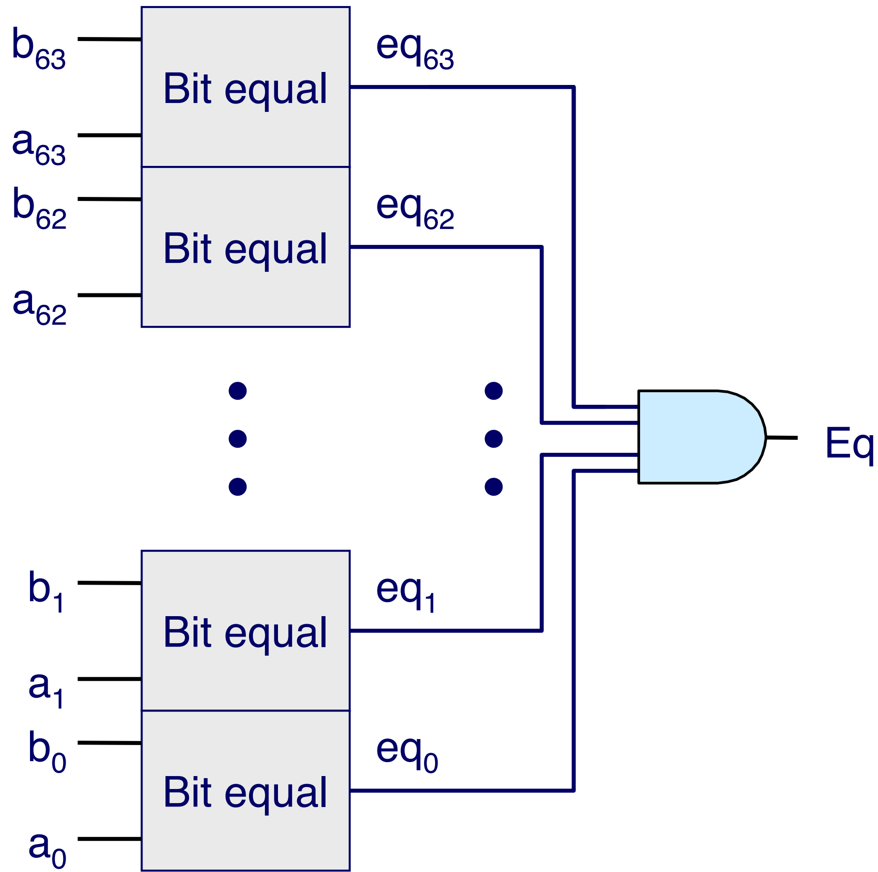
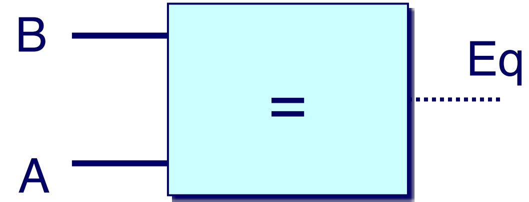
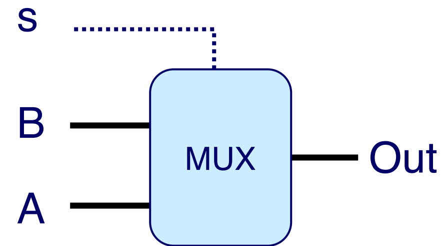




Bit-Level Multiplexor (MUX)

- Control signal s
- Data signals A and B
- Output A when s=1, B when s=0



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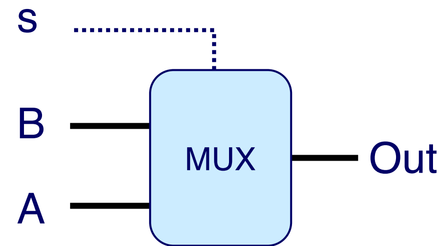


```
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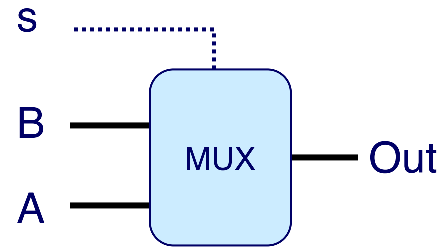


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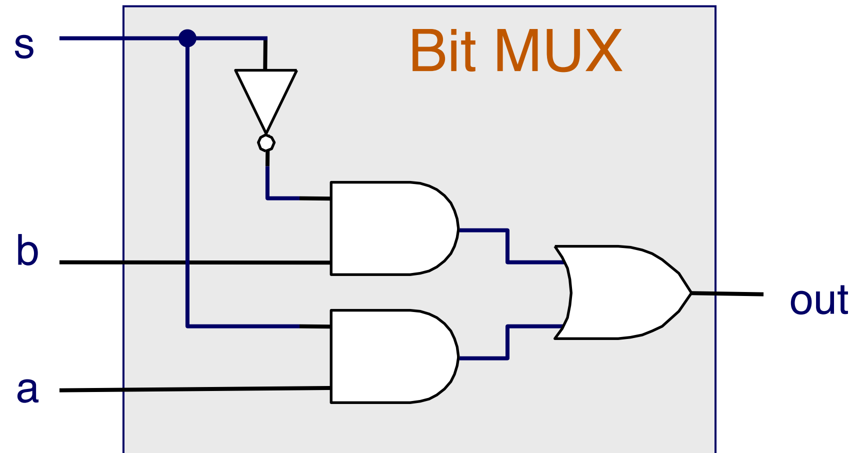

4-Input Multiplexor

- Control signal s; Data signals A, B, C, and D
- Output: A when s = 00, B when s = 01, C when s = 10, D when s = 11

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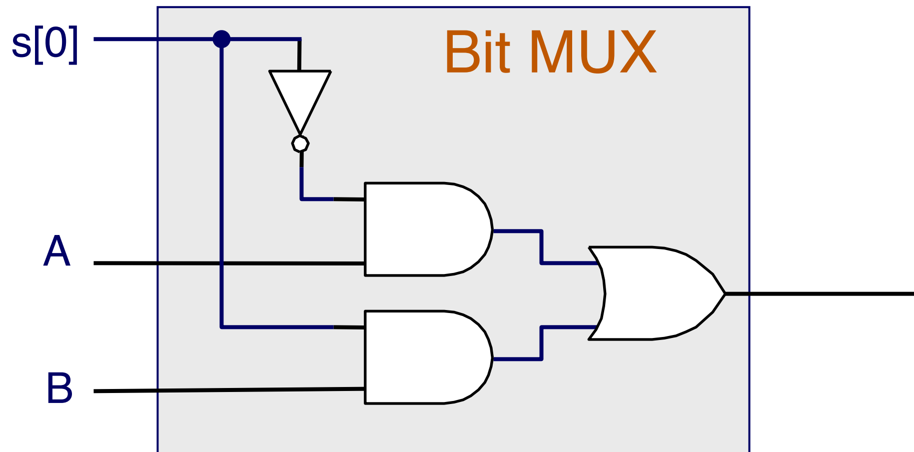

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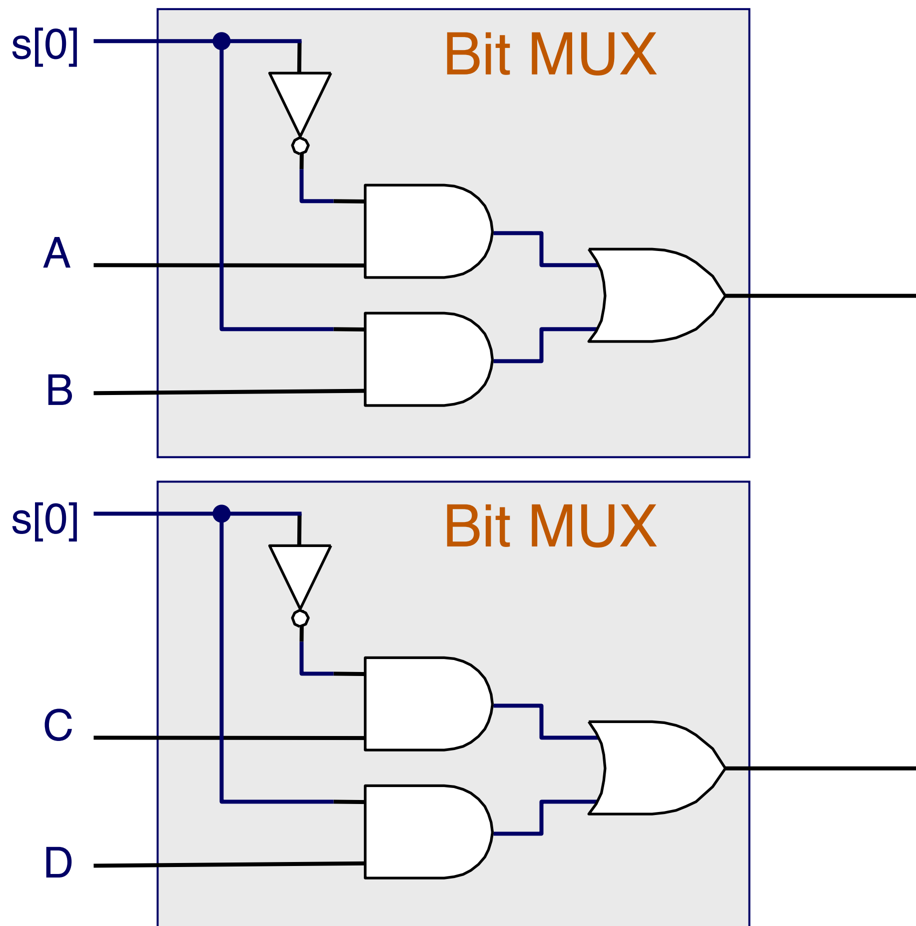

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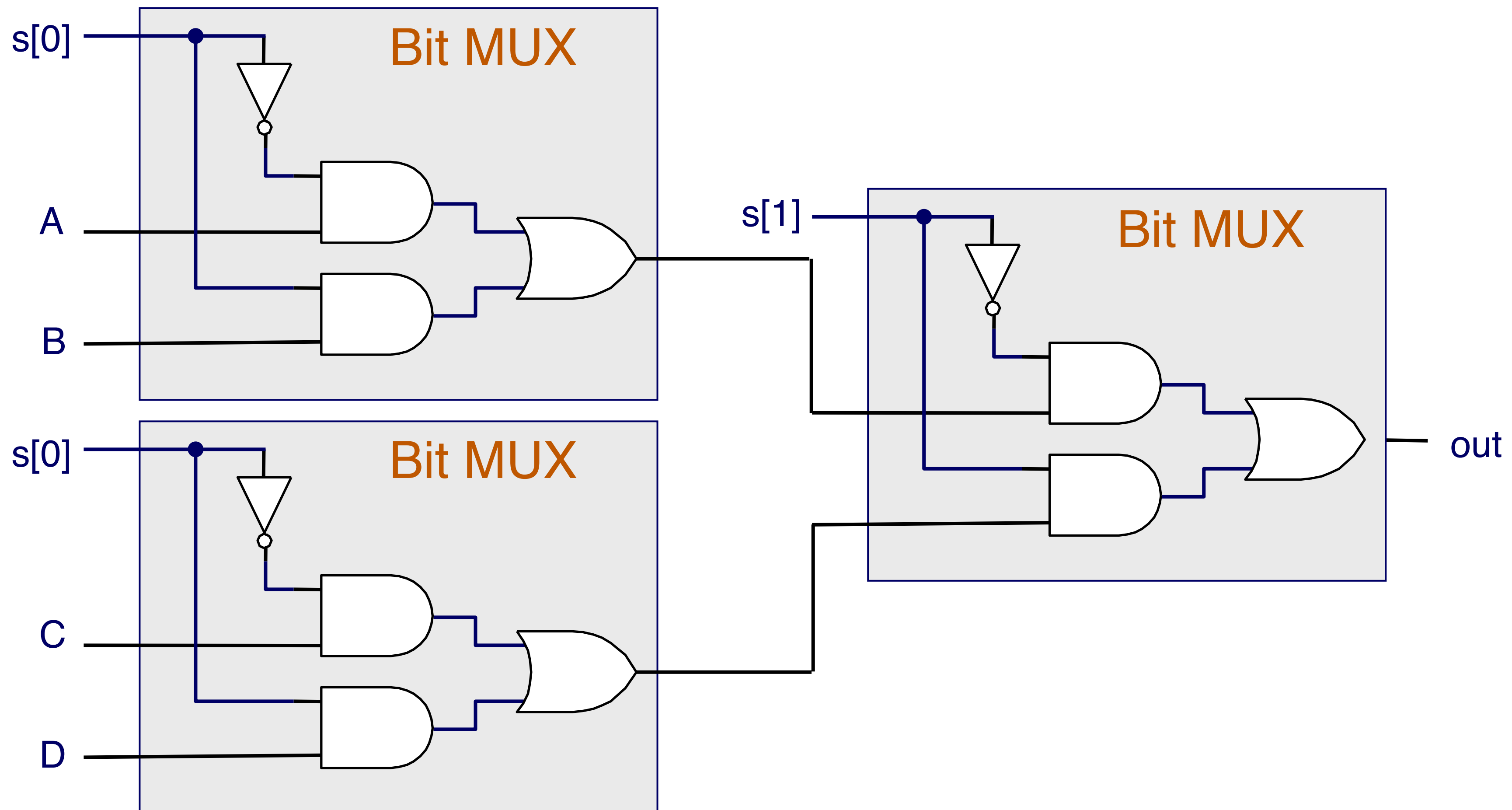

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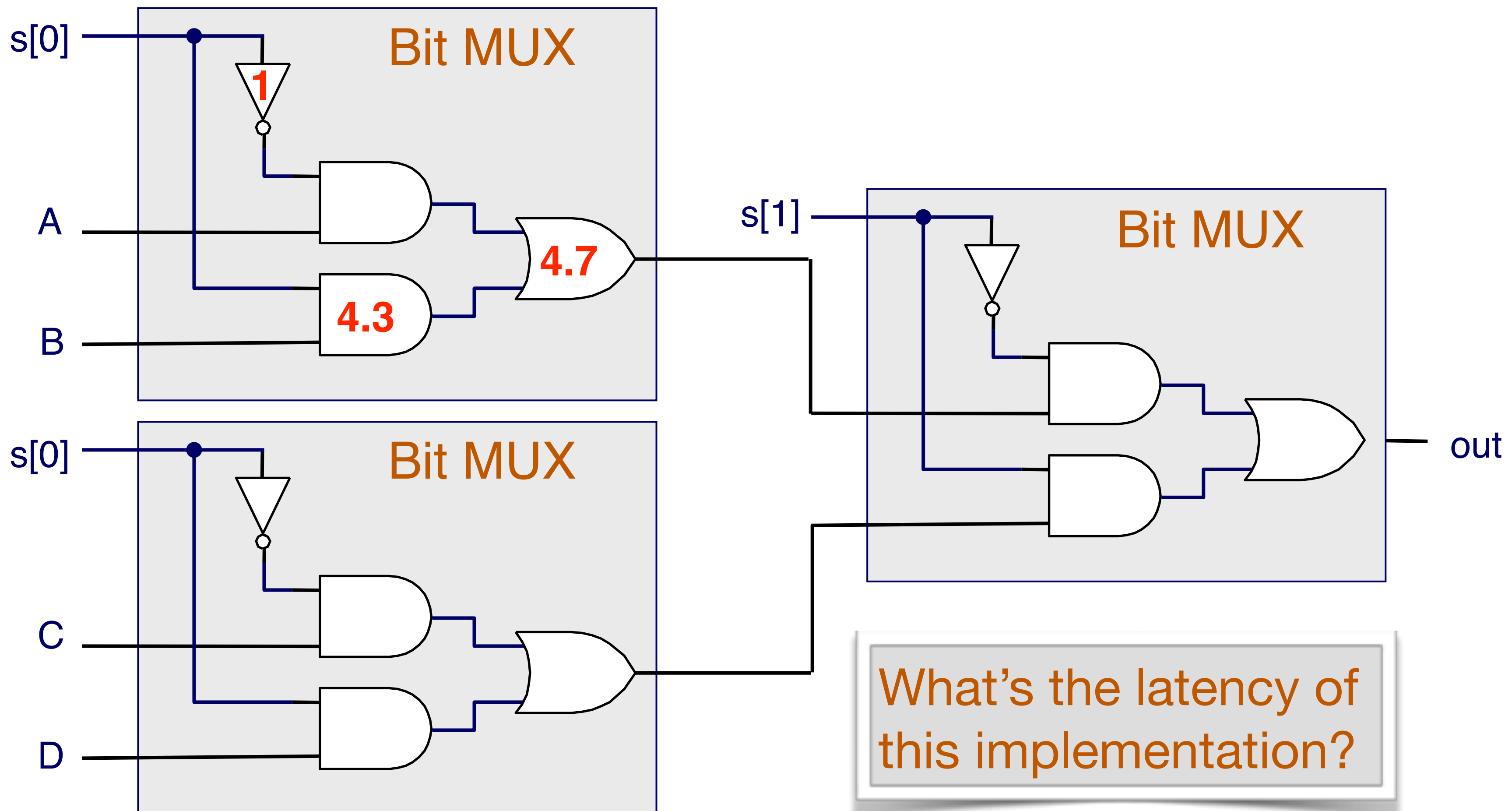

Logic Design and VLSI

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- The *logic synthesis tool* will automatically generate the “best” gate-level implementation of a piece of logic.
- Take a Logic Design or Very Large Scale Integrated-Circuit (VLSI) course if you want to know more about circuit design.
  - Logic design uses the gate-level abstractions
  - VLSI tells you how the gates are implemented at transistor-level

Full (1-bit) Adder

Add two bits and carry-in,
produce one-bit sum and carry-out.

A	B	C_{in}	S	C_{out}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Full (1-bit) Adder

Add two bits and carry-in,
produce one-bit sum and carry-out.

$$S = (\sim A \mathbin{\&} \sim B \mathbin{\&} C_{in}) \mid (\sim A \mathbin{\&} B \mathbin{\&} \sim C_{in}) \mid (A \mathbin{\&} \sim B \mathbin{\&} \sim C_{in}) \mid (A \mathbin{\&} B \mathbin{\&} C_{in})$$

$$C_{ou} = (\sim A \mathbin{\&} B \mathbin{\&} C_{in}) \mid (A \mathbin{\&} \sim B \mathbin{\&} C_{in}) \mid (A \mathbin{\&} B \mathbin{\&} \sim C_{in}) \mid (A \mathbin{\&} B \mathbin{\&} C_{in})$$

A	B	C_{in}	S	C_{out}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

1-bit Full Adder

Add two bits and carry-in,
produce one-bit sum and carry-out.

$$
\begin{aligned}
C_{ou} = &(\sim A \ \& \ B \ \& \ C_{in}) \\
| &(A \ \& \ \sim B \ \& \ C_{in}) \\
| &(A \ \& \ B \ \& \ \sim C_{in}) \\
| &(A \ \& \ B \ \& \ C_{in})
\end{aligned}
$$

1-bit Full Adder

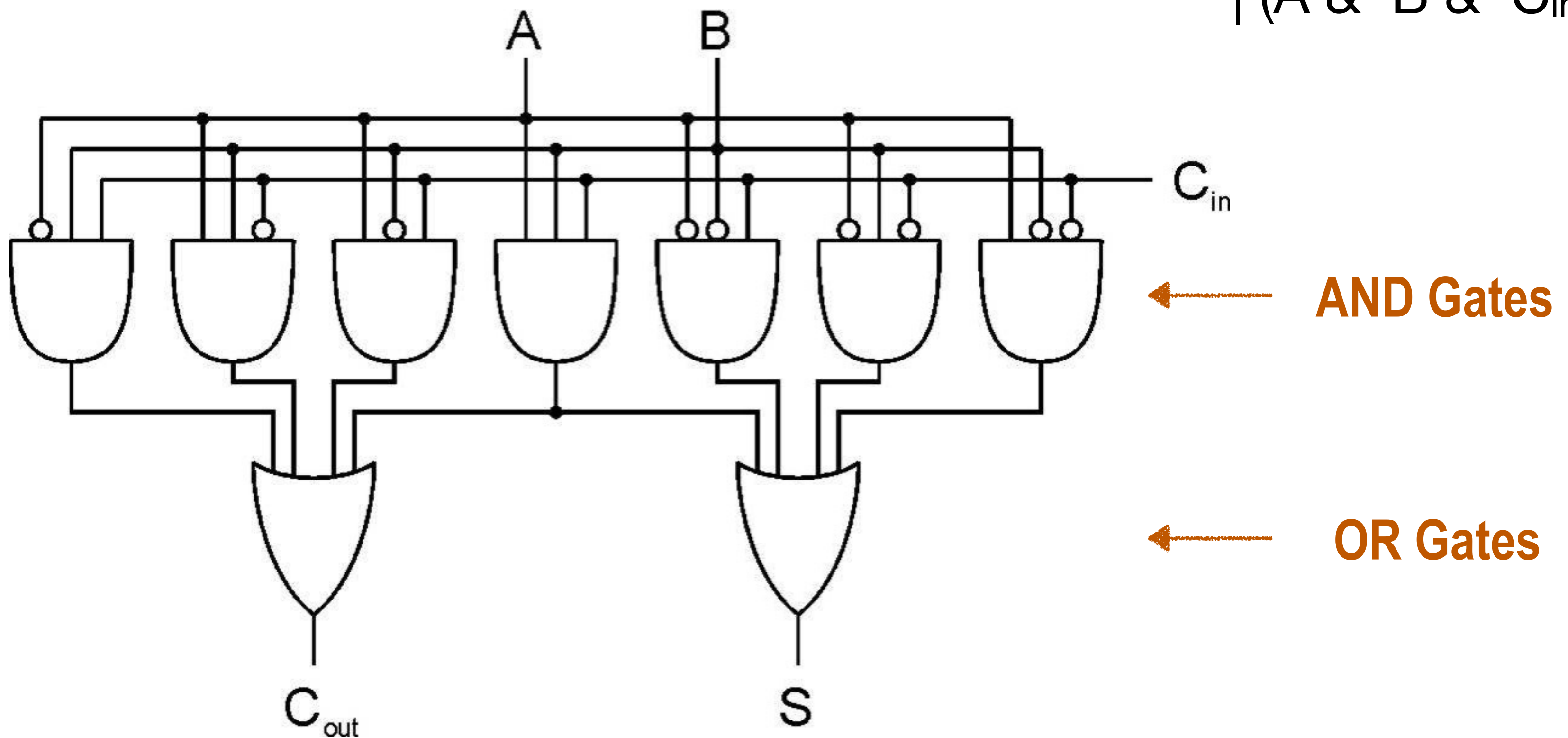
Add two bits and carry-in,
produce one-bit sum and carry-out.

C_{ou} = (~A & B & C_{in})

| (A & ~B & C_{in})

| (A & B & ~C_{in})

| (A & B & C_{in})



1-bit Full Adder

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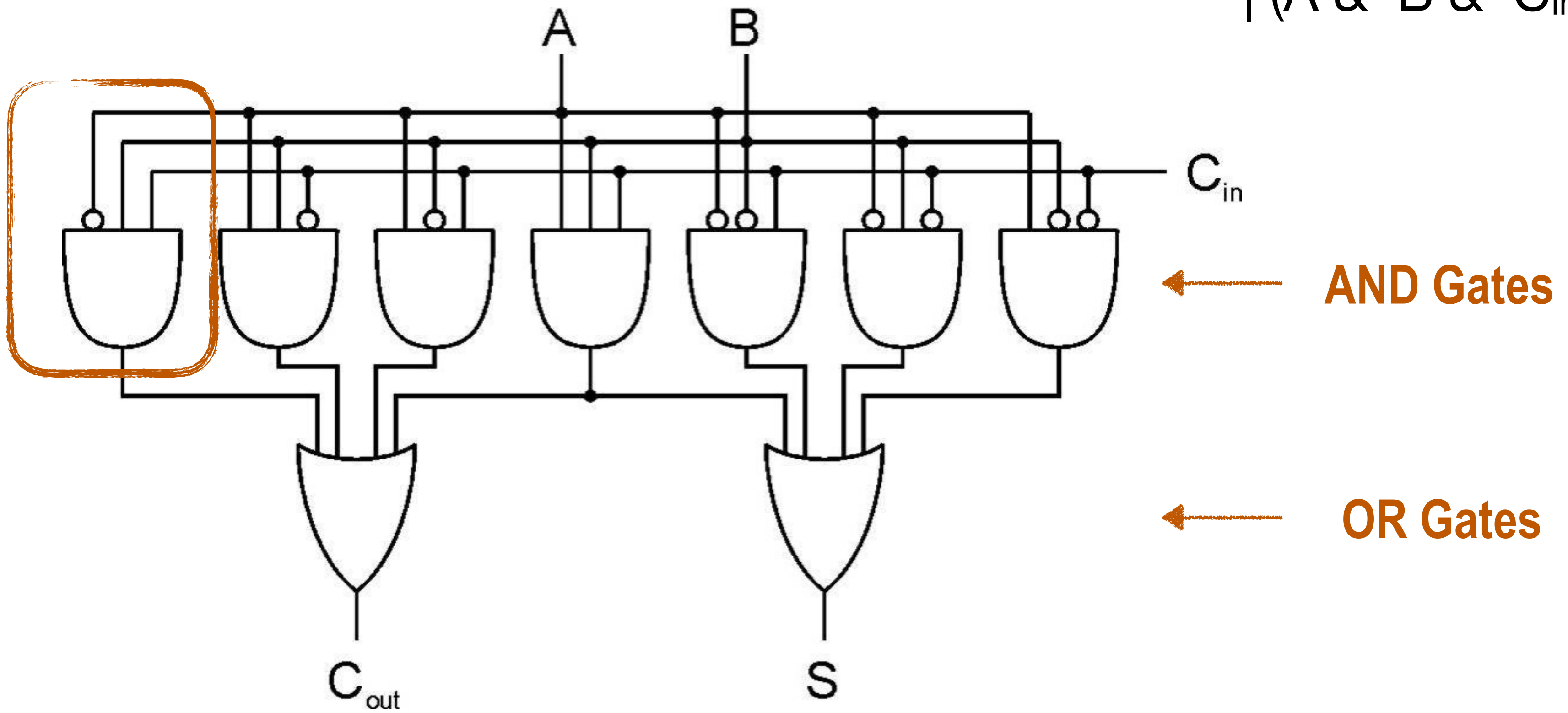
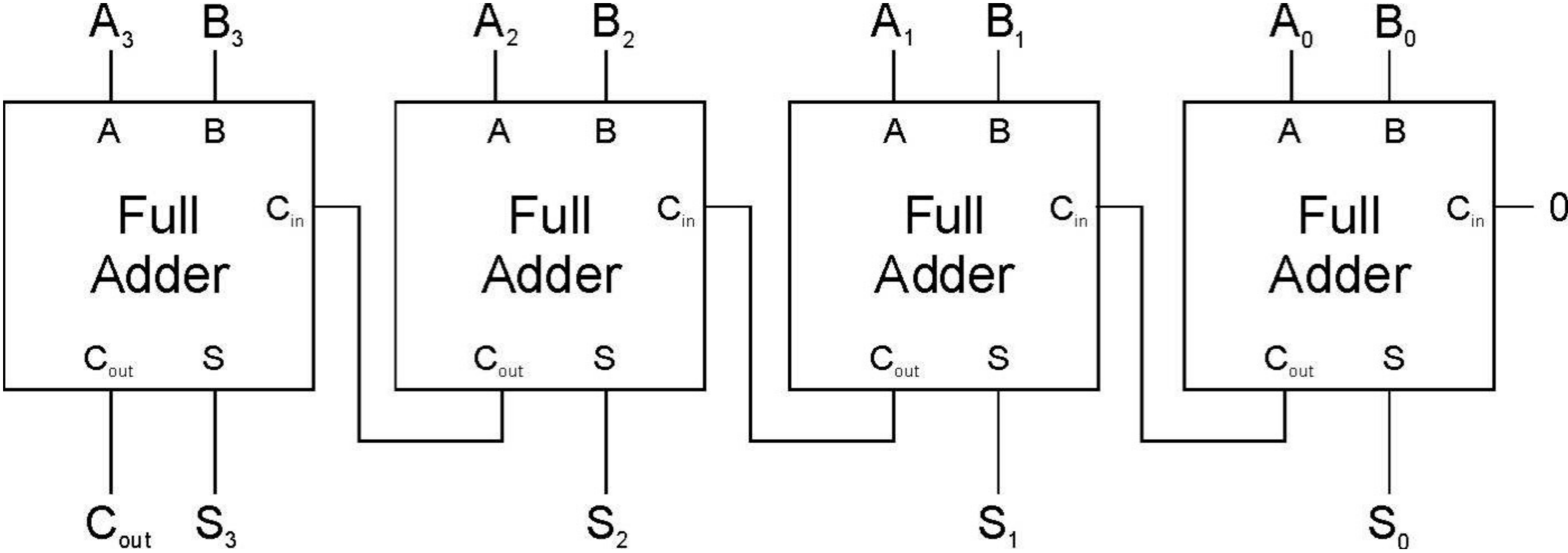
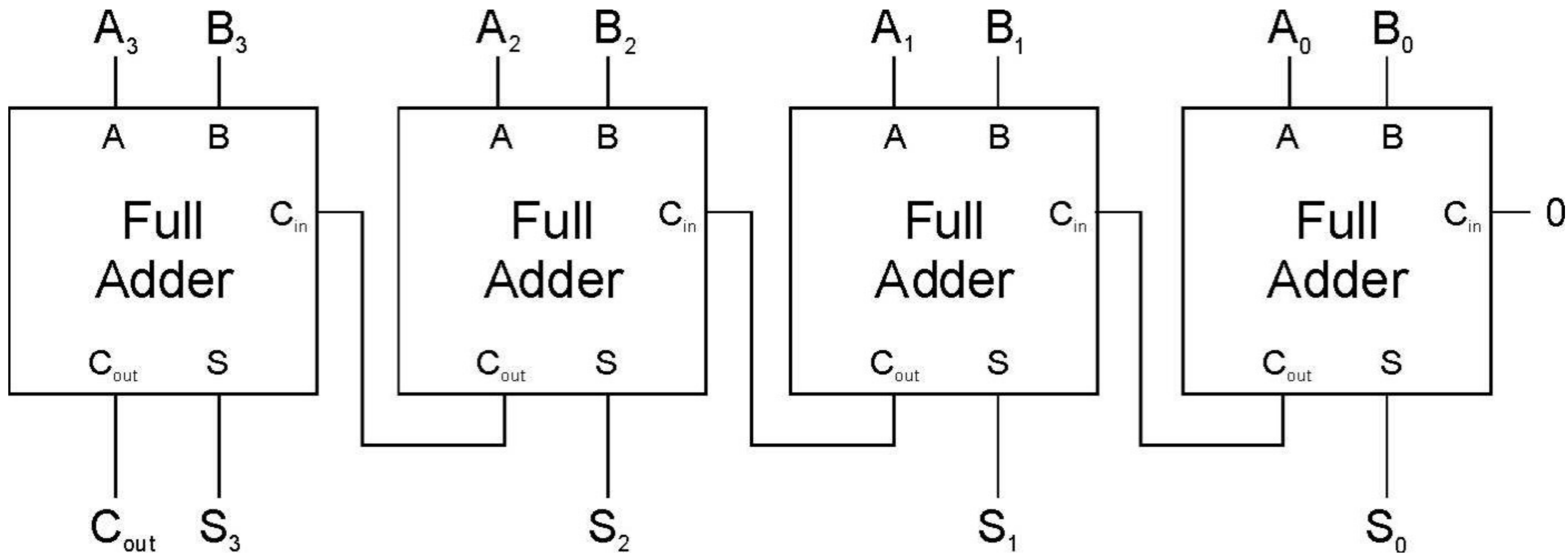


Four-bit Adder



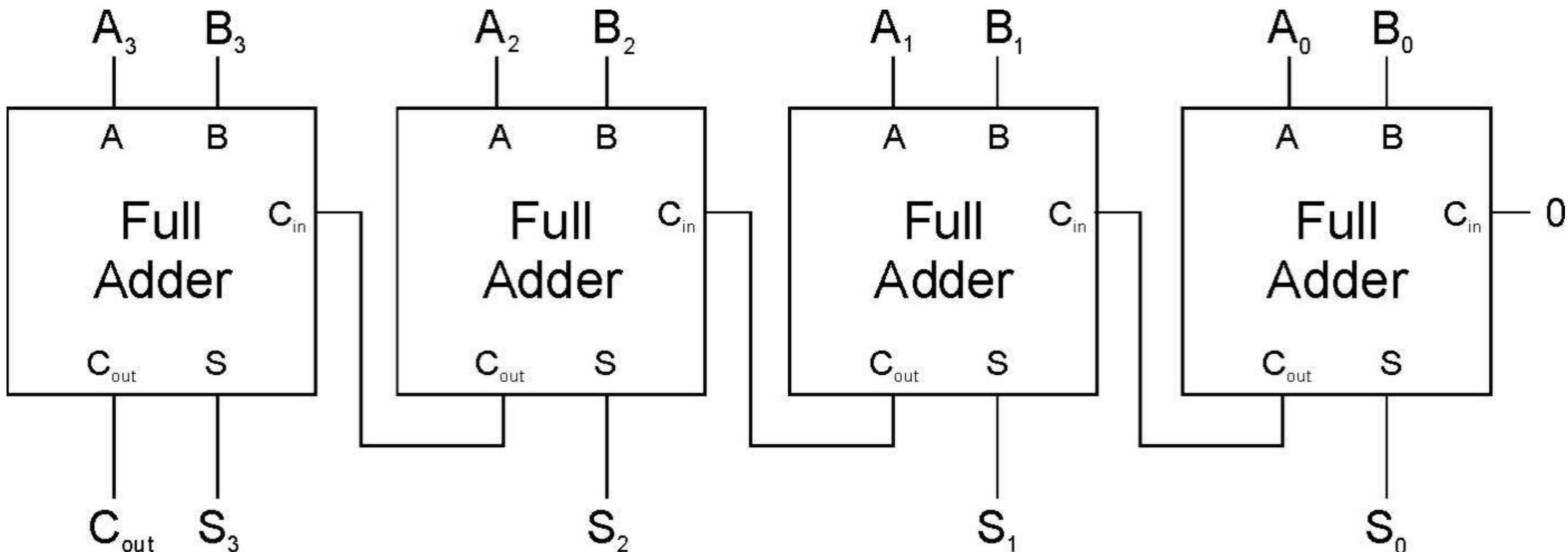
Four-bit Adder

- Ripple-carry Adder
  - Simple, but performance linear to bit width

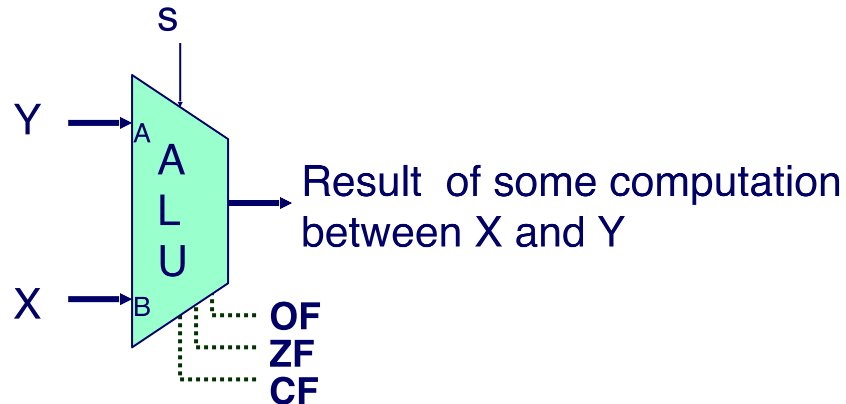


Four-bit Adder

- Ripple-carry Adder
  - Simple, but performance linear to bit width
- Carry look-ahead adder (CLA)
  - Generate all carriers simultaneously



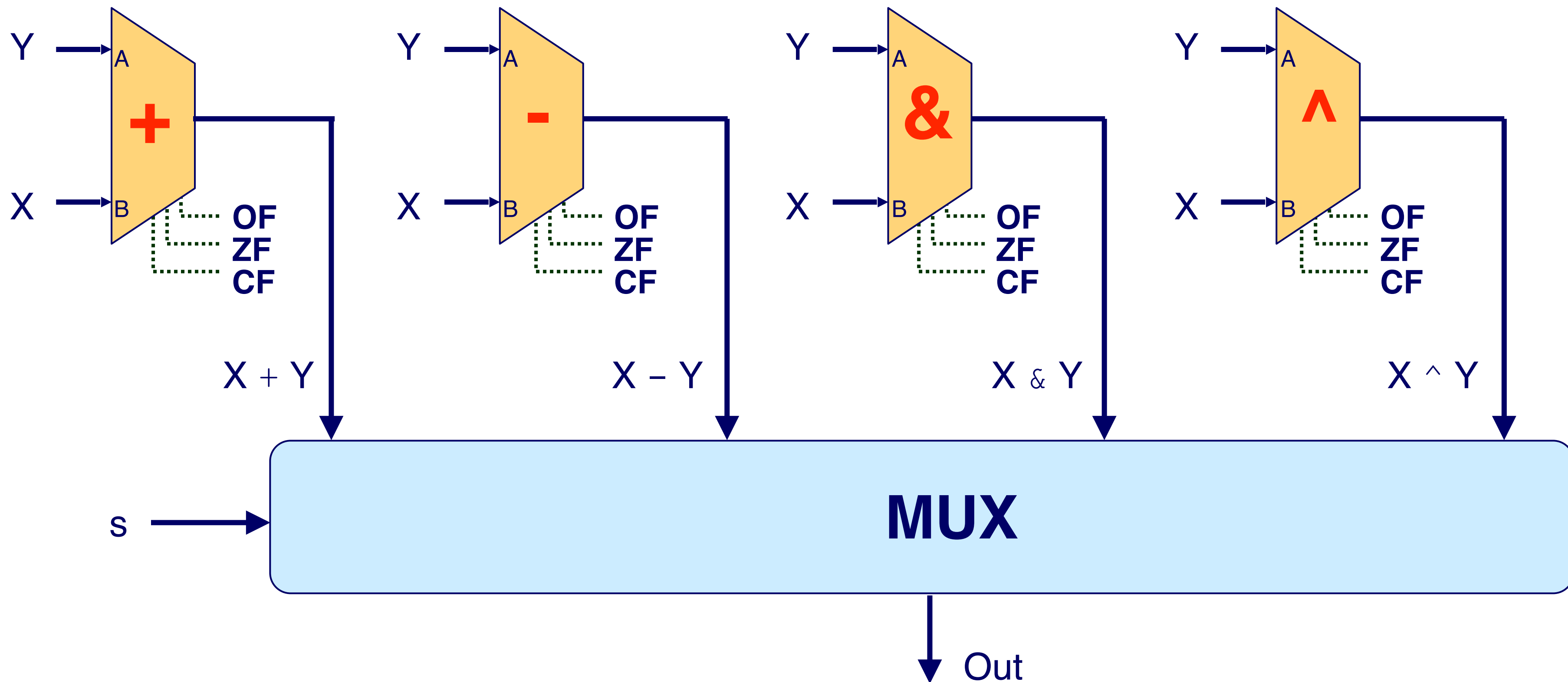
Arithmetic Logic Unit



- An ALU performs multiple kinds of computations.
- The actual computation depends on the selection signal s.
- Also sets the condition codes (status flags)
- For instance:
    - X + Y when s == 00
    - X - Y when s == 01
    - X & Y when s == 10
    - X ^ Y when s == 11
- How can this ALU be implemented?

Arithmetic Logic Unit

- Implement 4 different circuits, one for each operation.
- Then use a MUX to select the results



Today: Circuits Basics

- Transistors
- Circuits for computations
- Circuits for storing data

The Need for Storing Bits

- Assembly programs set architecture (processor) states.
    - Register File
    - Status Flags
    - Memory
    - Program Counter

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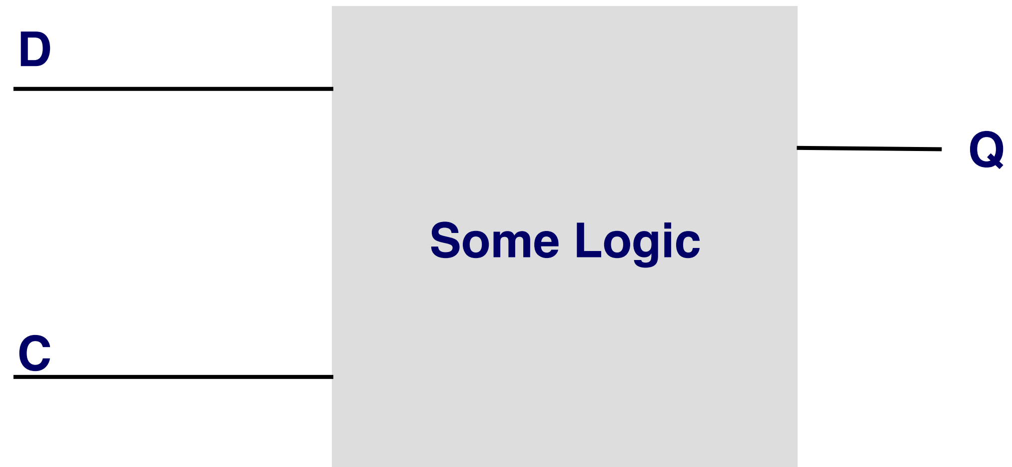
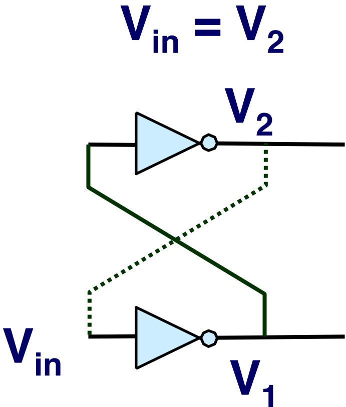
- Every state is essentially some bits that are stored/loaded.
- Think of the program execution as an FSM.
- The hardware must provide mechanisms to load and store bits.
- There are many different ways to store bits. They have trade-offs.

Build a 1-Bit Storage

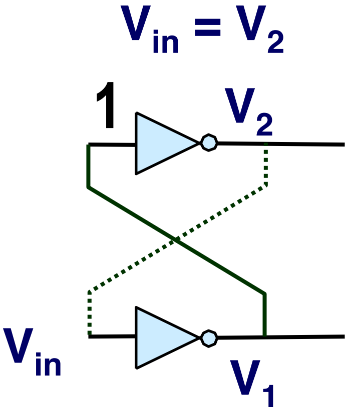


- What I would like:
  - D is the data I want to store (0 or 1)
  - C is the control signal
    - When C is 1, Q becomes D (i.e., storing the data)
    - When C is 0, Q doesn't change with D (data stored)

Bitstable Element



Bitstable Element



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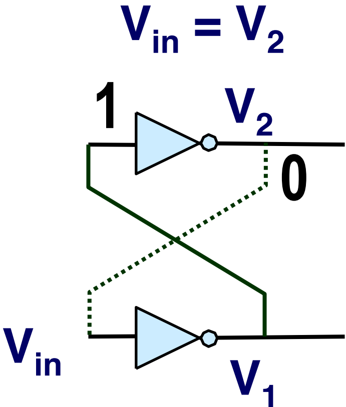

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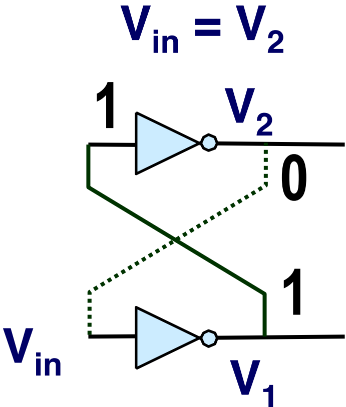

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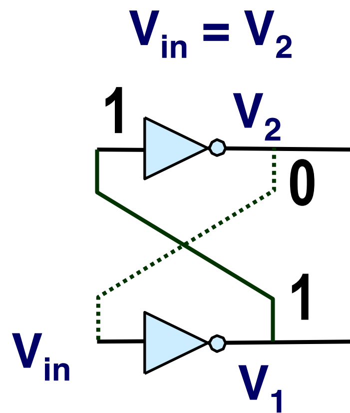

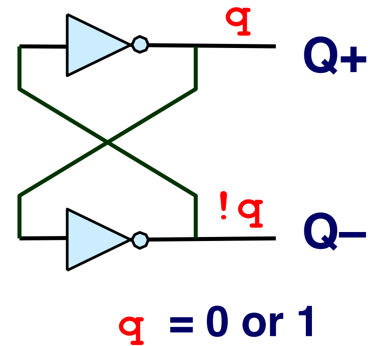

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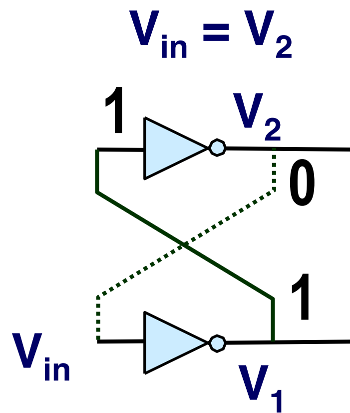
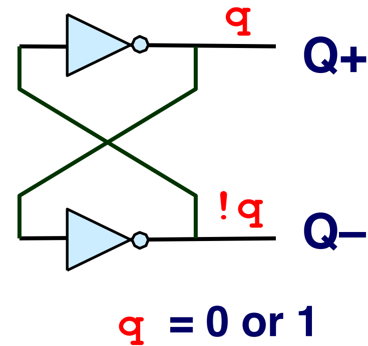


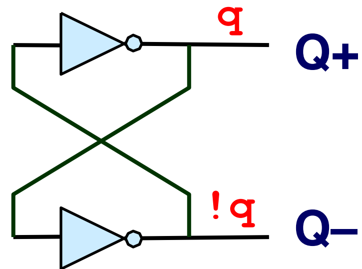
Bistable Element



Q+ ***continuously*** outputs q.

Storing and Accessing 1 Bit

Bistable Element



q = 0 or 1

Storing and Accessing 1 Bit

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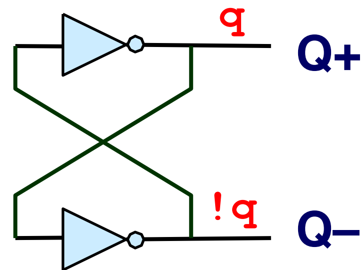

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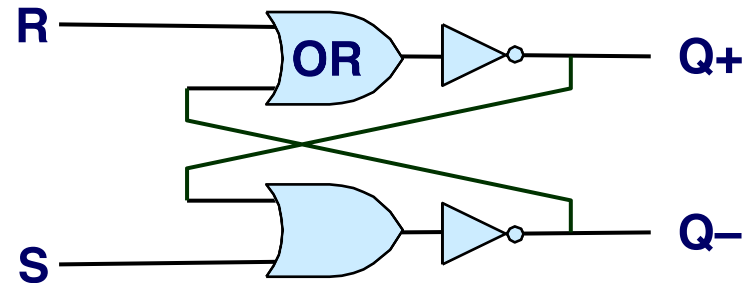

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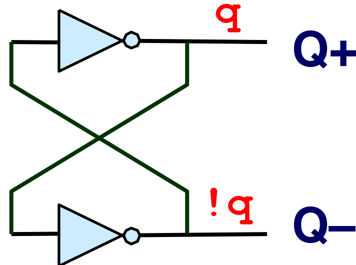

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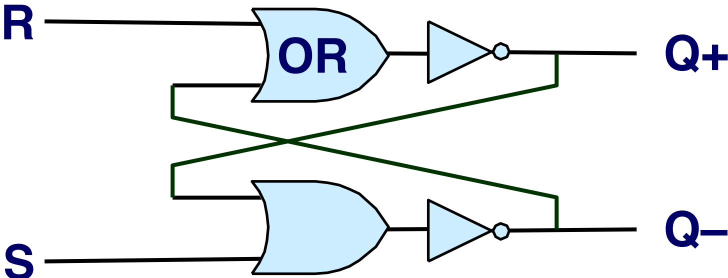

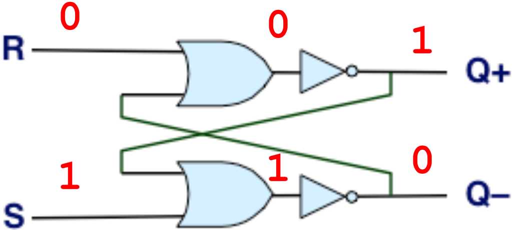

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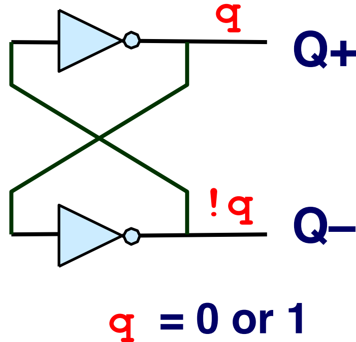
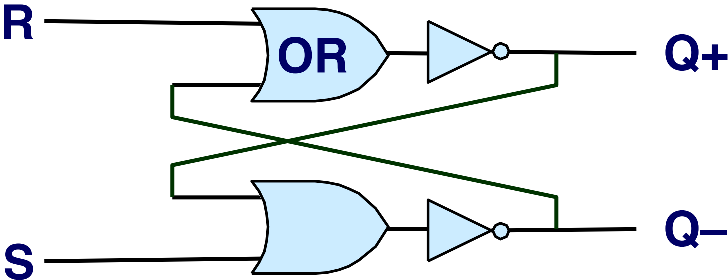
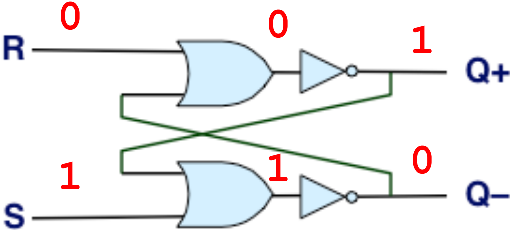




Setting Q+ to 1



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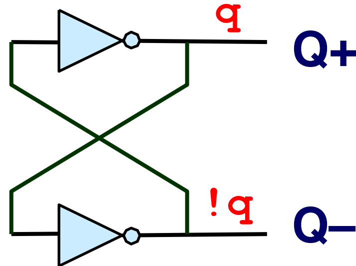

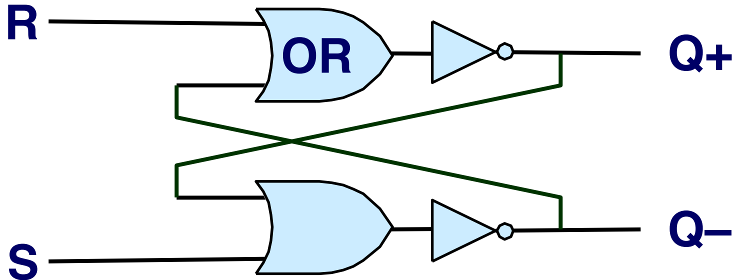

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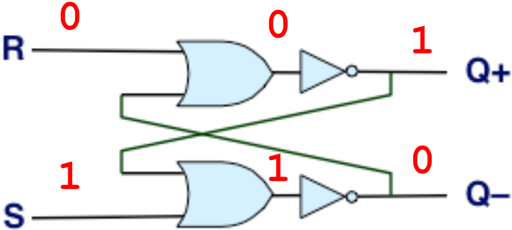

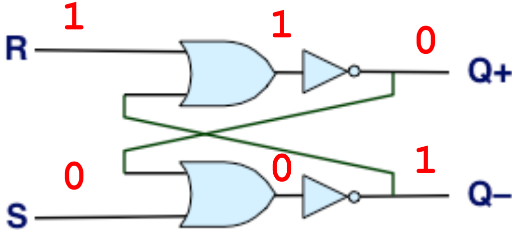

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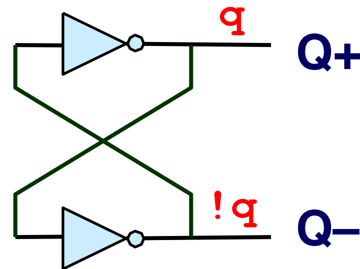
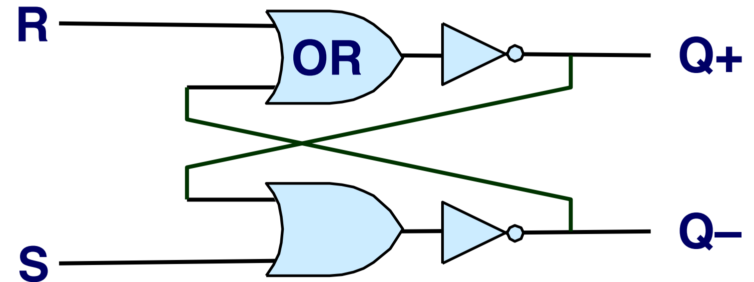


q = 0 or 1



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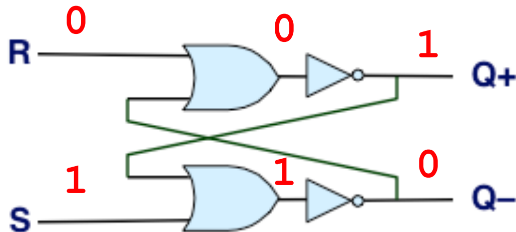
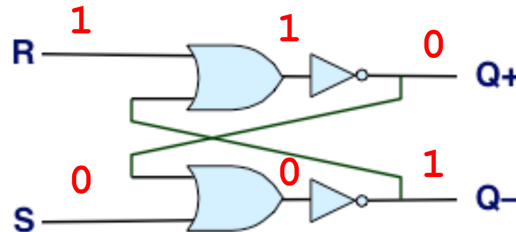


Setting Q+ to 0



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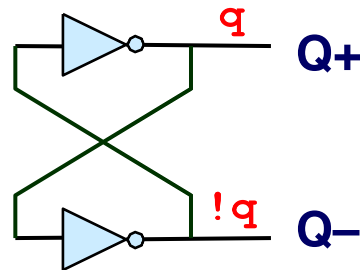
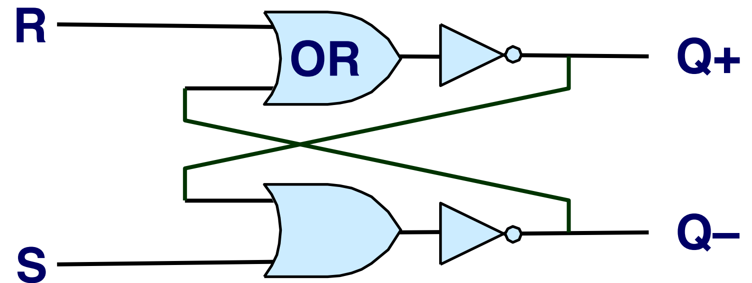
Bistable Element





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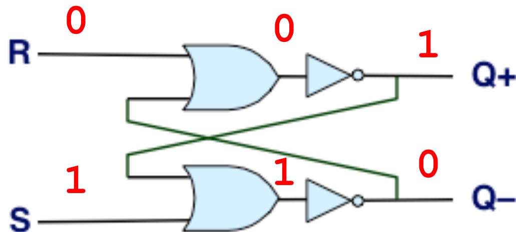

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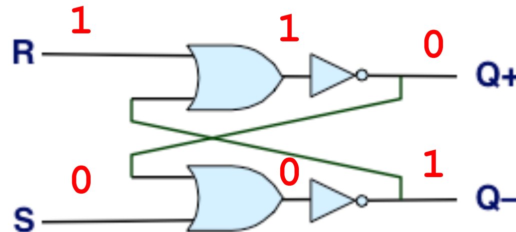

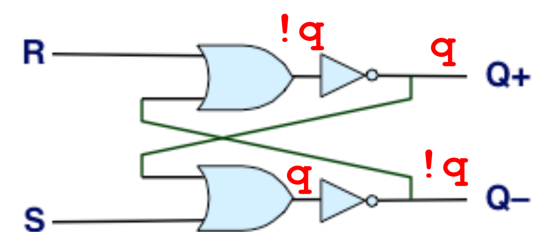

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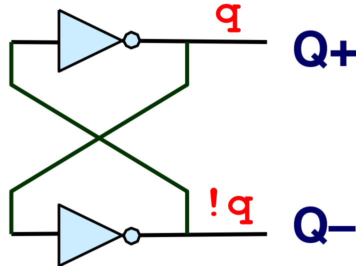
Bistable Element



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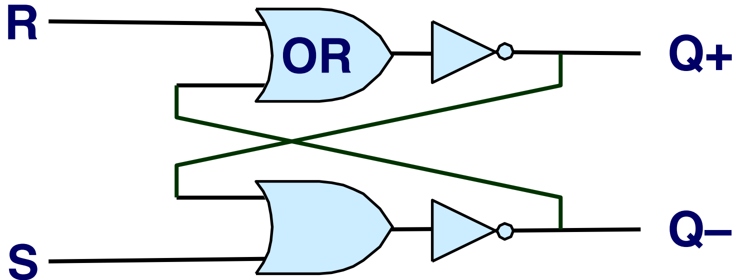

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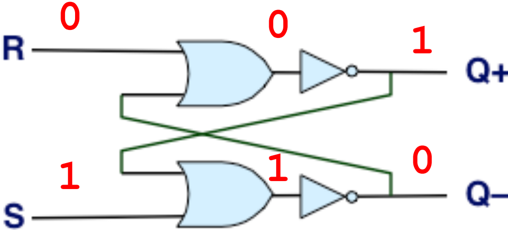

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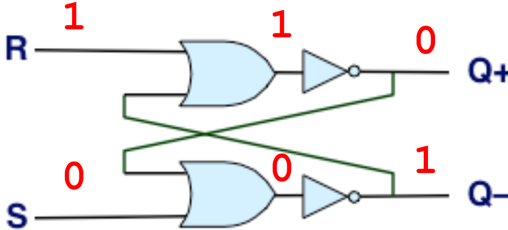

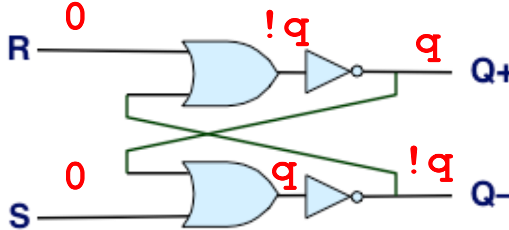

Storing and Accessing 1 Bit

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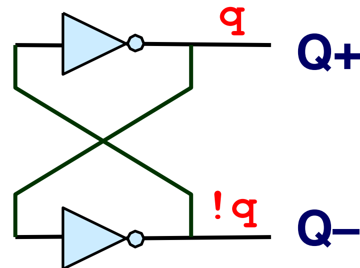

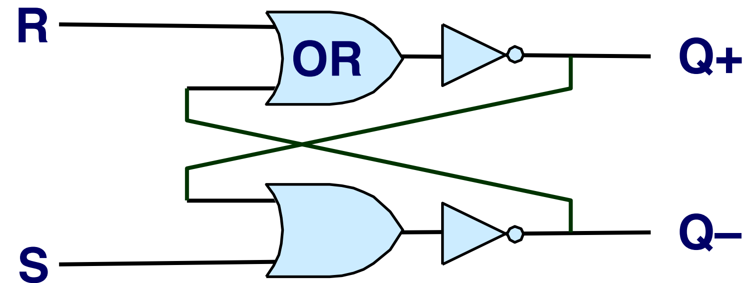

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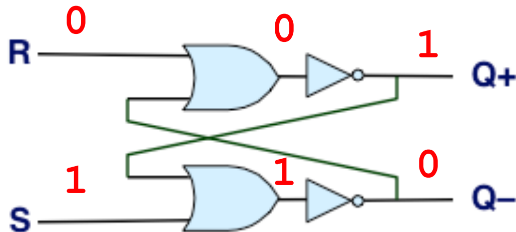
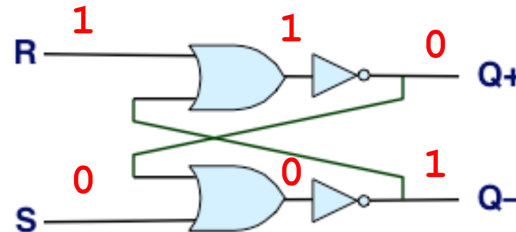
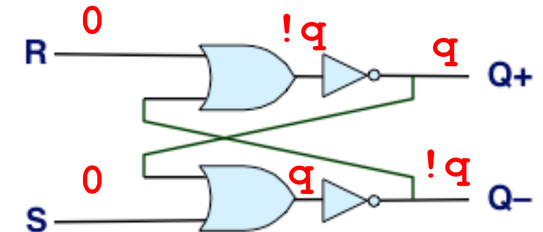


Setting Q+ to 0



Q+ value unchanged i.e., stored!



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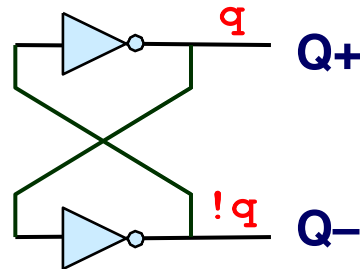

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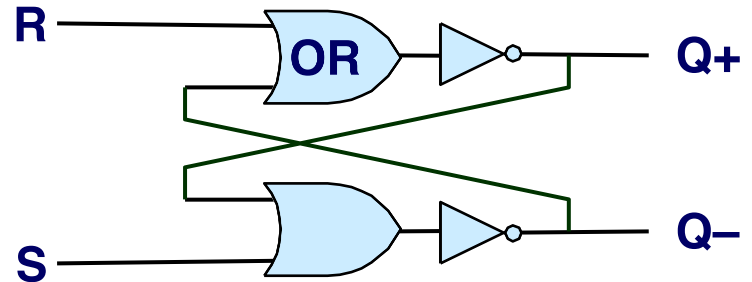
R-S Latch



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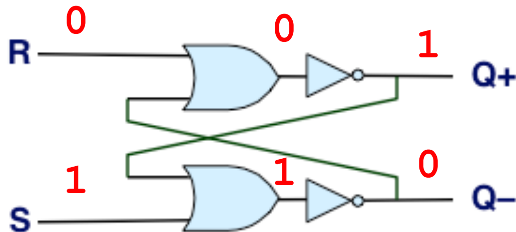
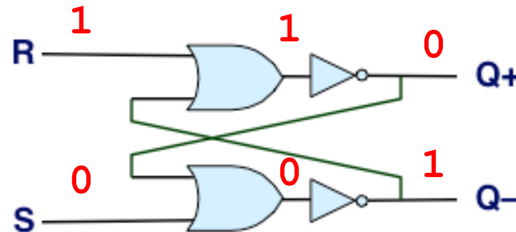


Setting Q+ to 0



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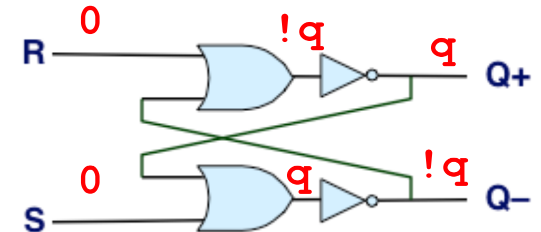

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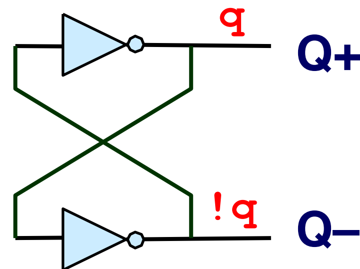

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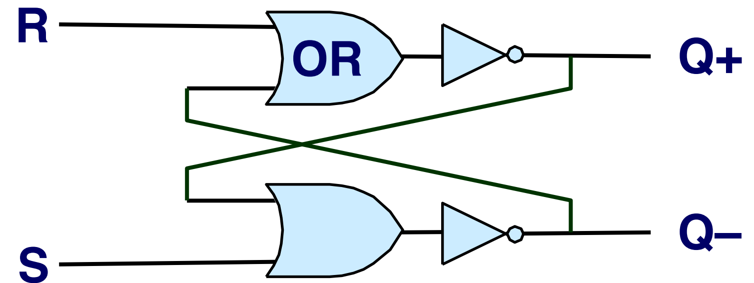

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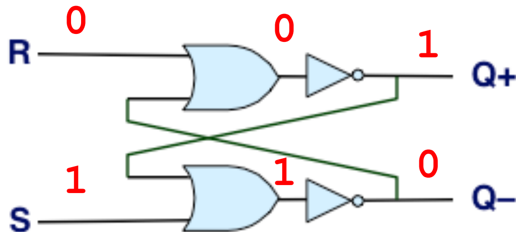
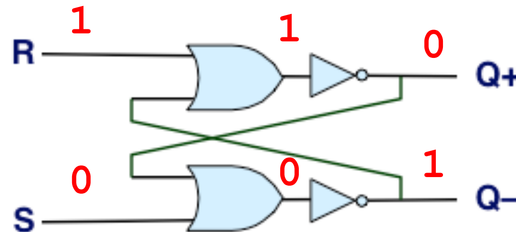


Setting Q+ to 0



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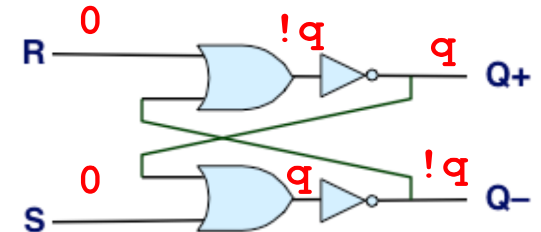
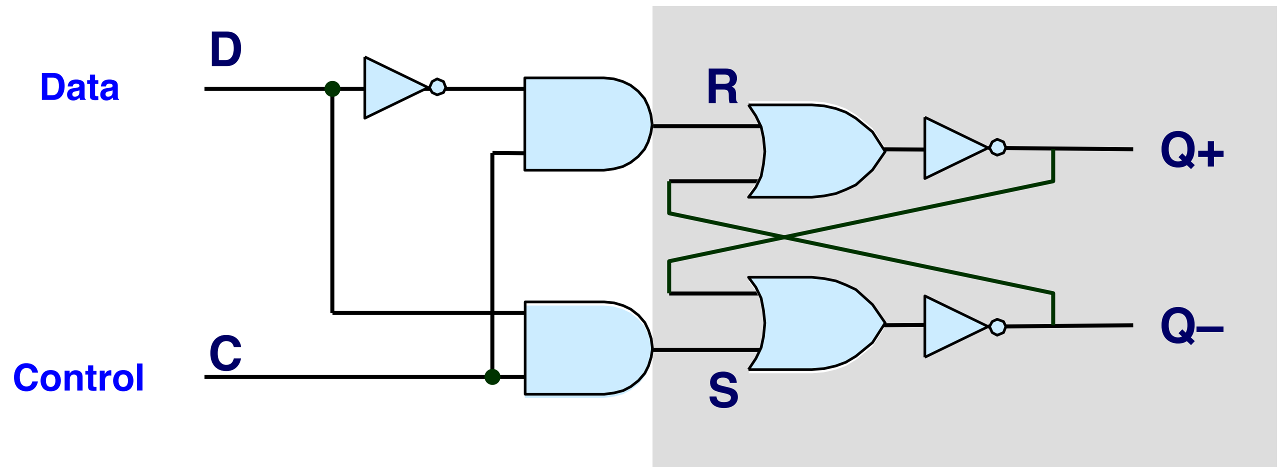


If R and S are different, Q+ is the same as S

Building on top of R-S Latch



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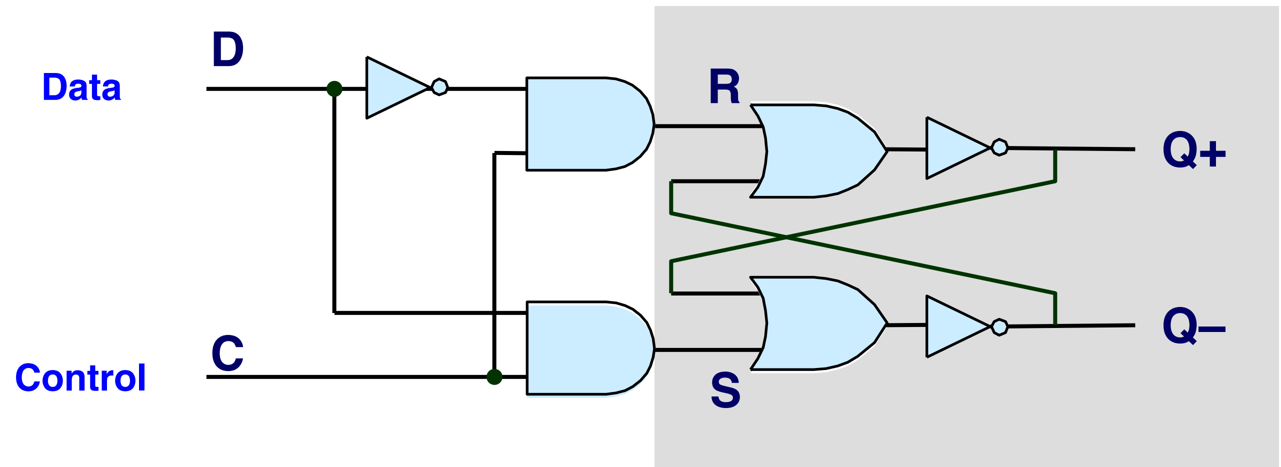

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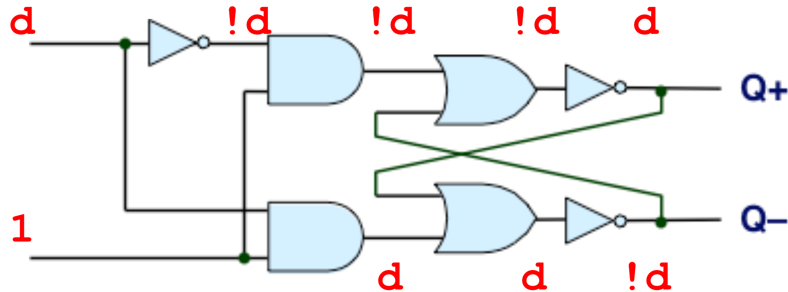
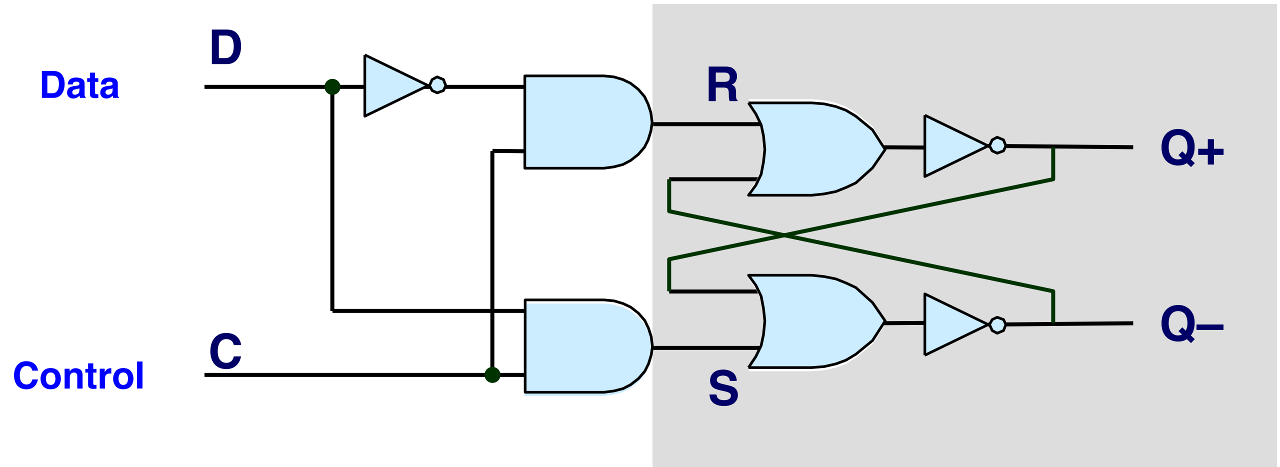
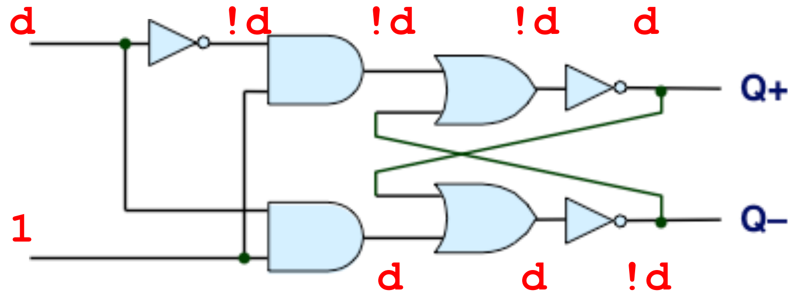


Building on top of R-S Latch

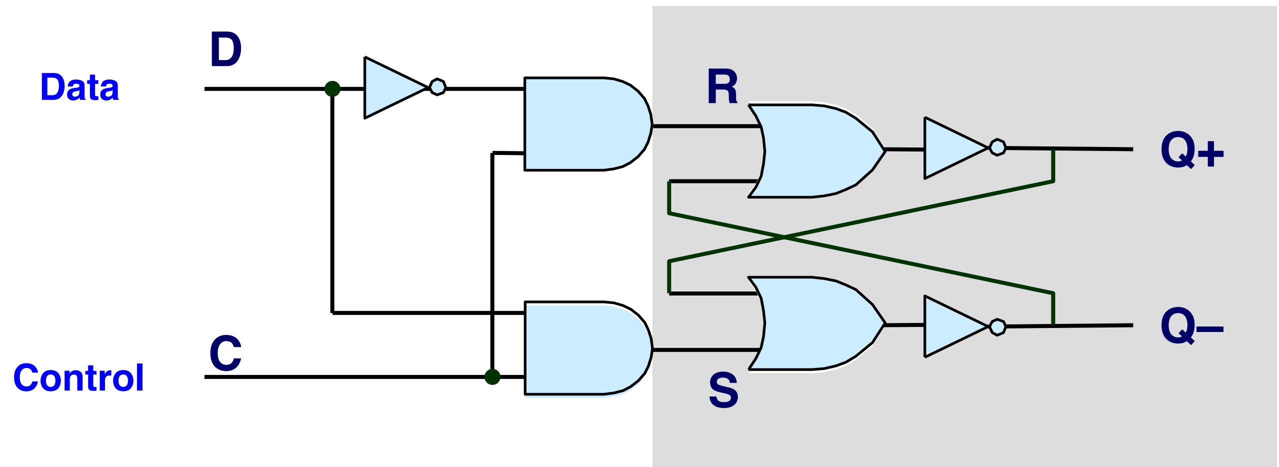


If R and S are different, Q+ is the same as S



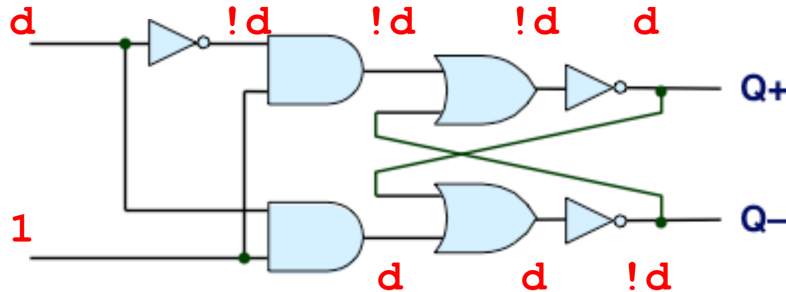
Q+ will continuously change as d changes

Building on top of R-S Latch



If R and S are different, Q+ is the same as S

Storing Data (Latching)



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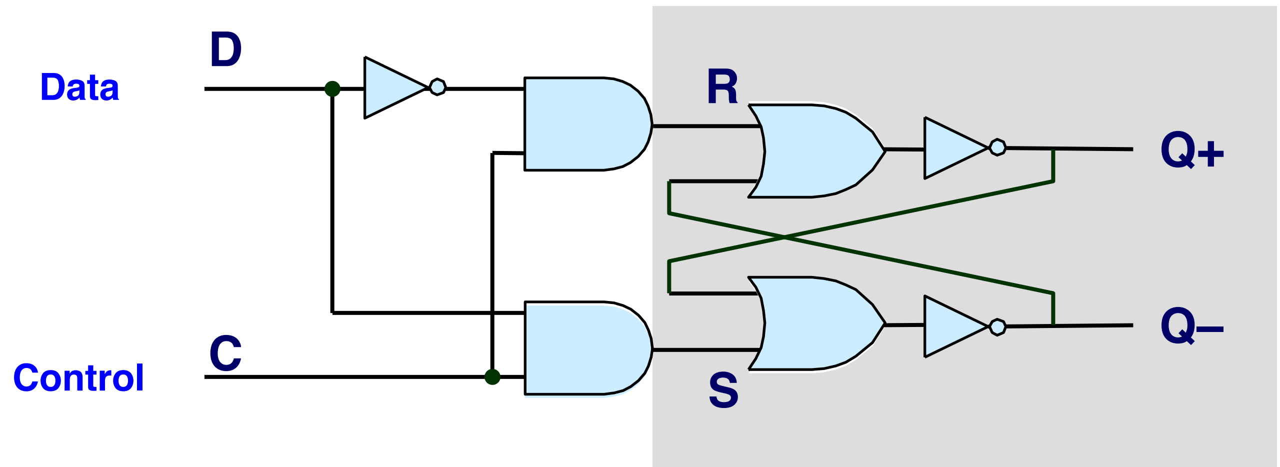

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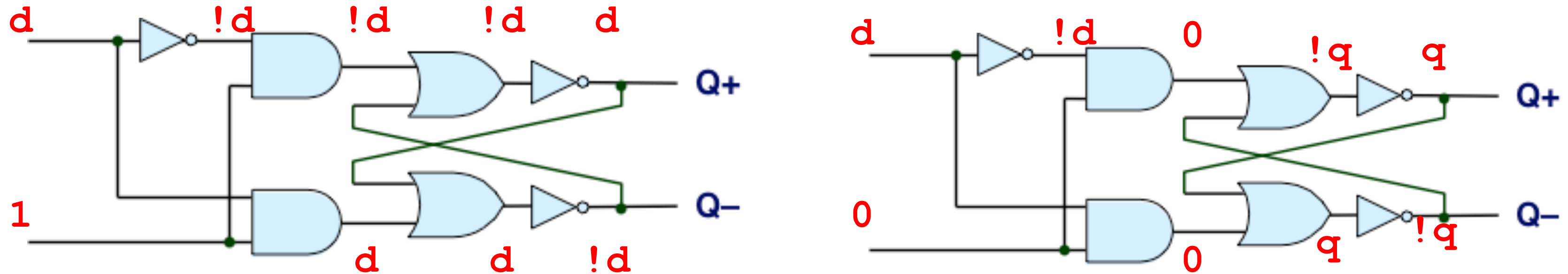

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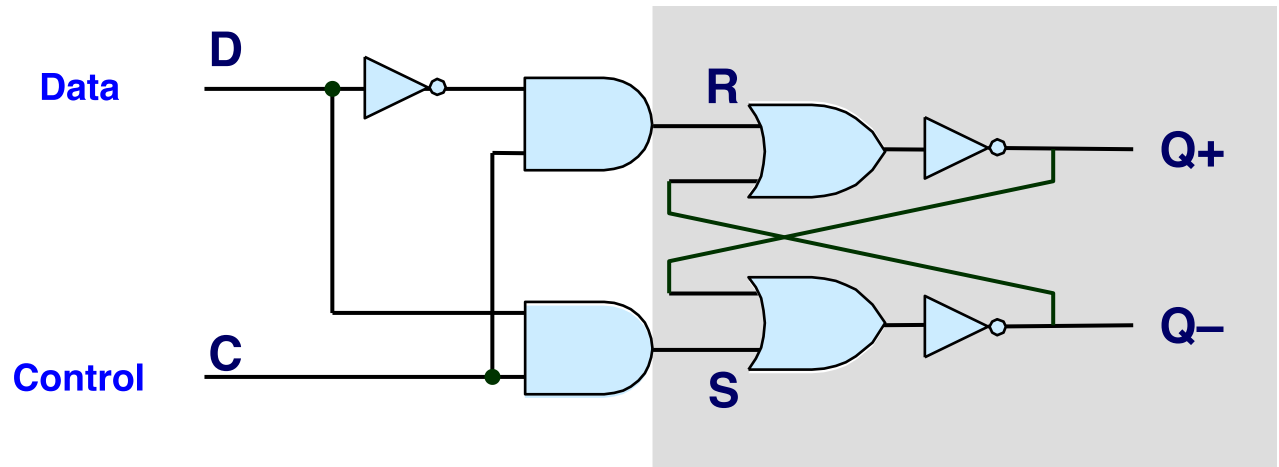

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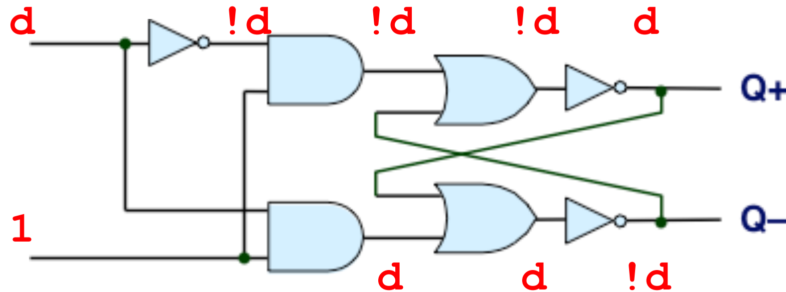

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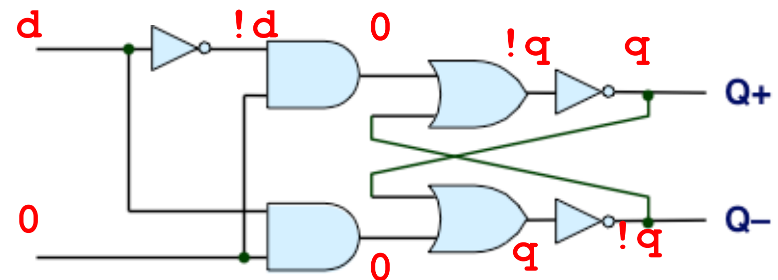

Q+ doesn't change with d

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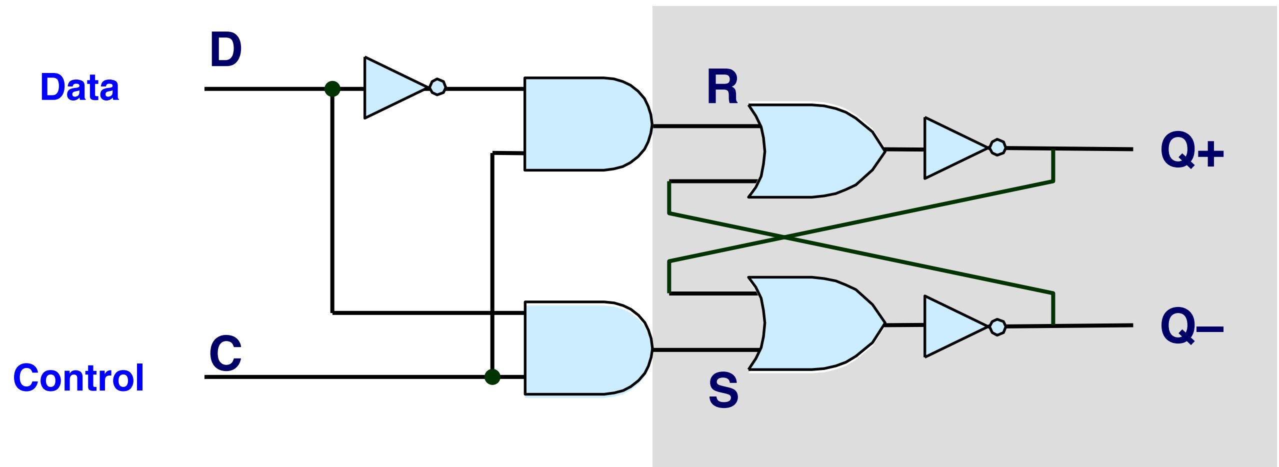

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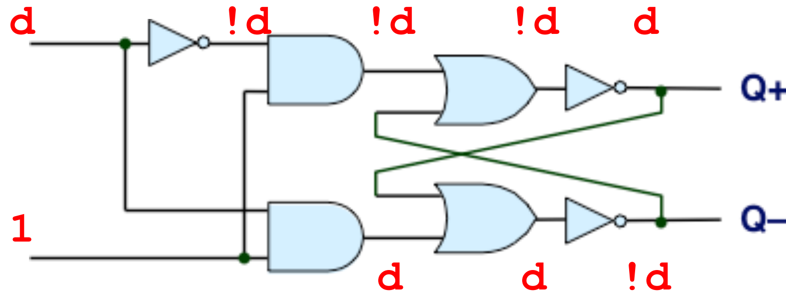

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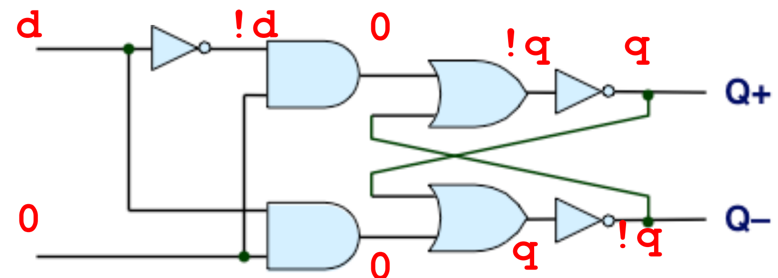
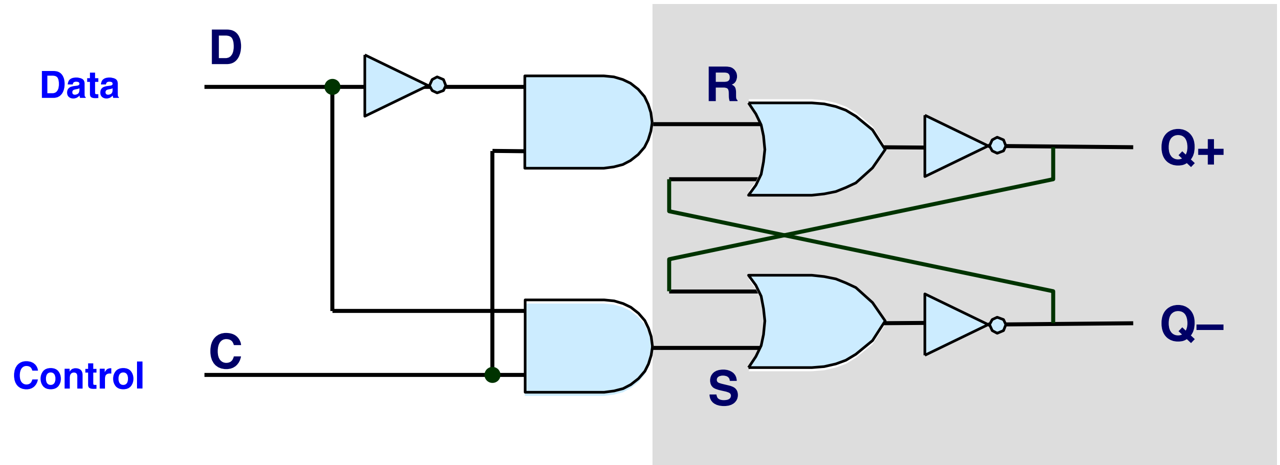
Holding Data



Q+ doesn’t change with d

Building on top of R-S Latch

D Latch



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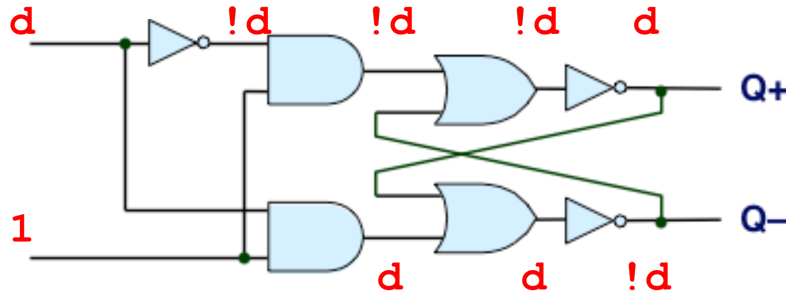

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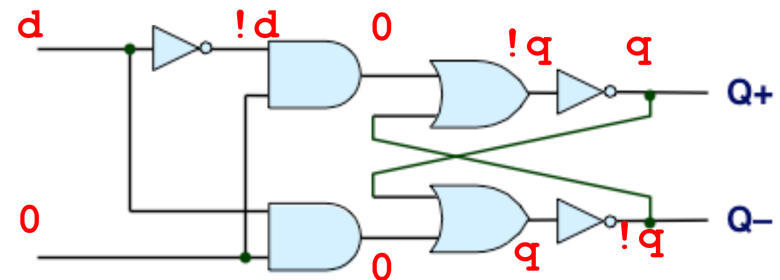
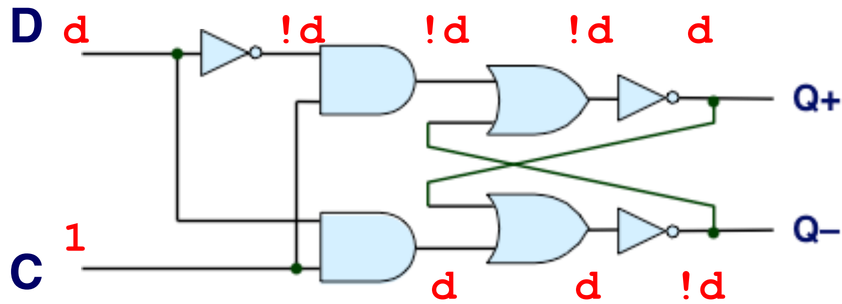


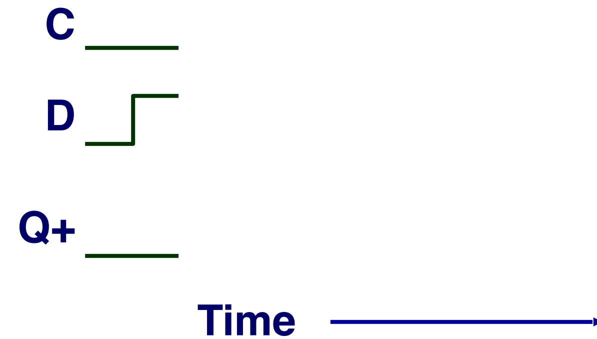
Q+ doesn't change with d

D-Latch is “Transparent”

Latching



Changing D



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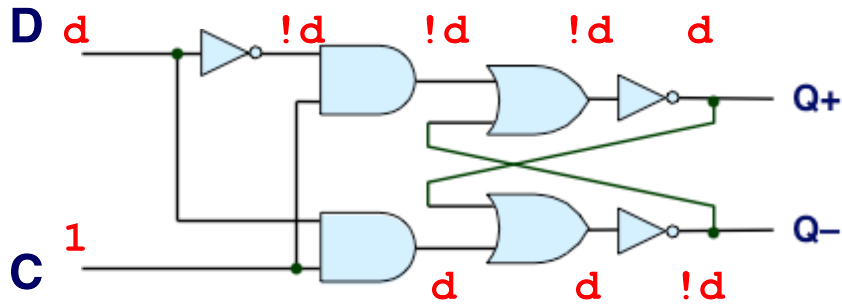

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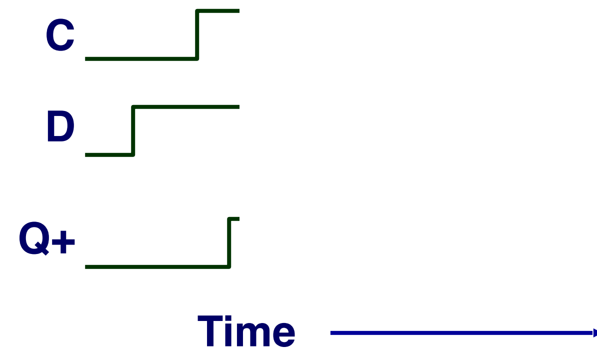

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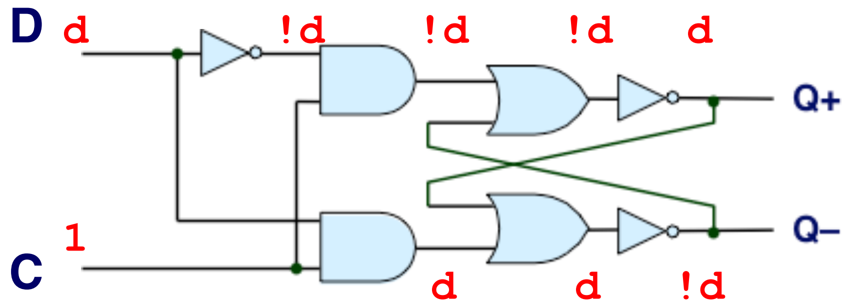

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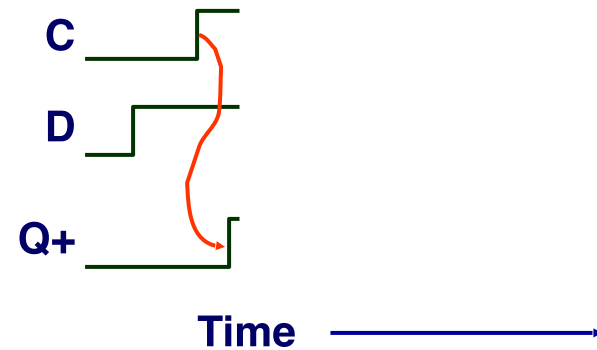

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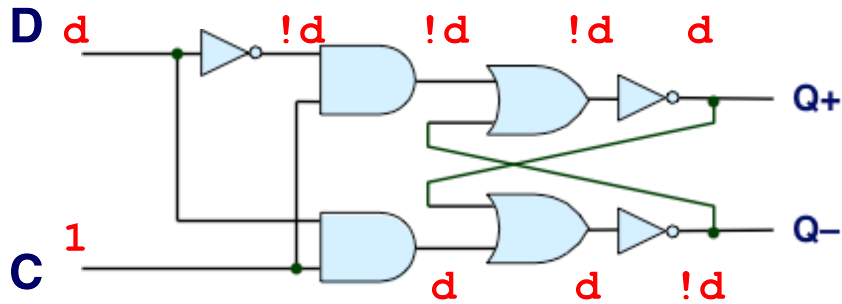

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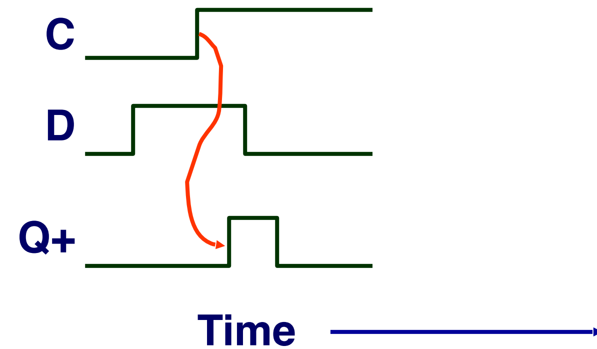

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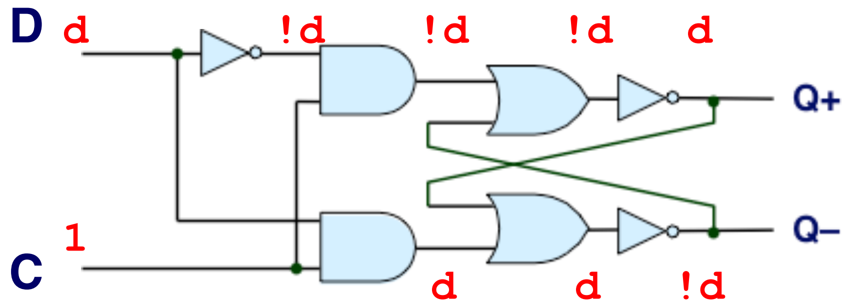

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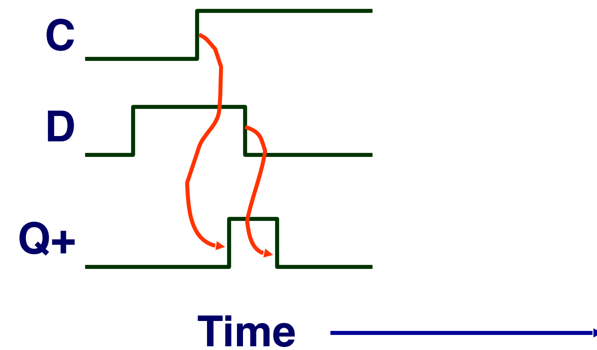

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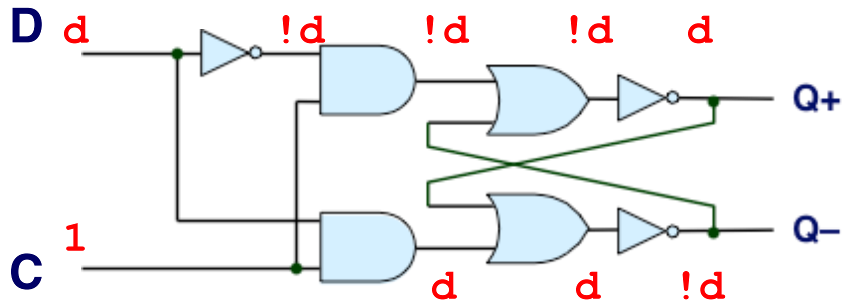

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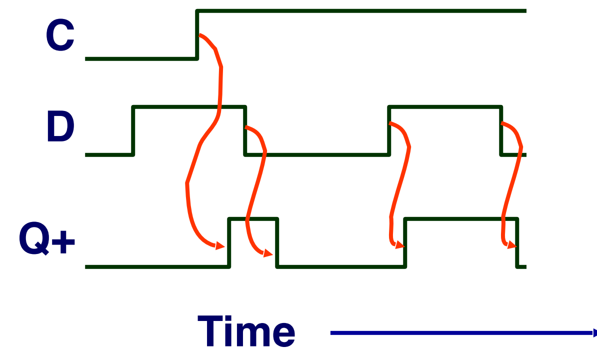

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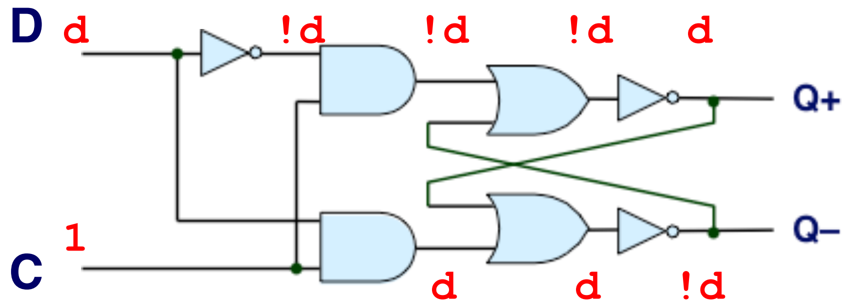

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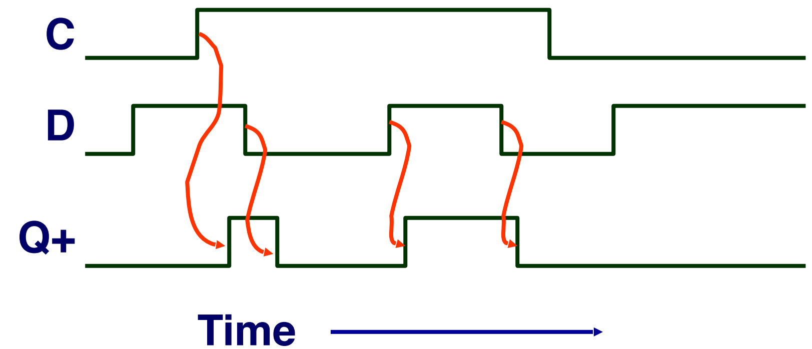

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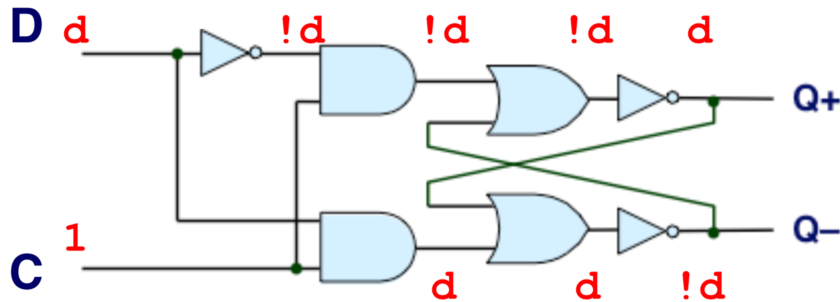

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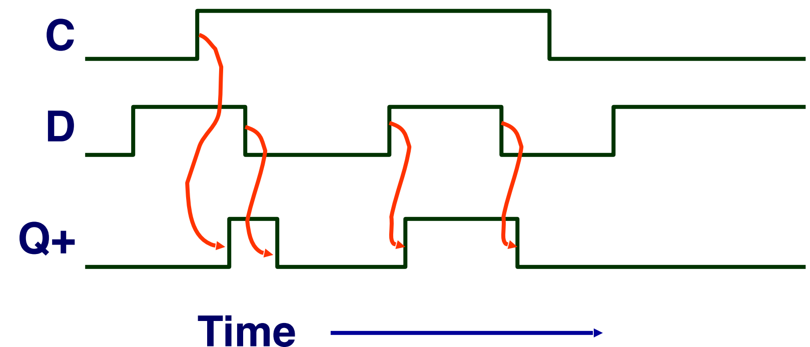

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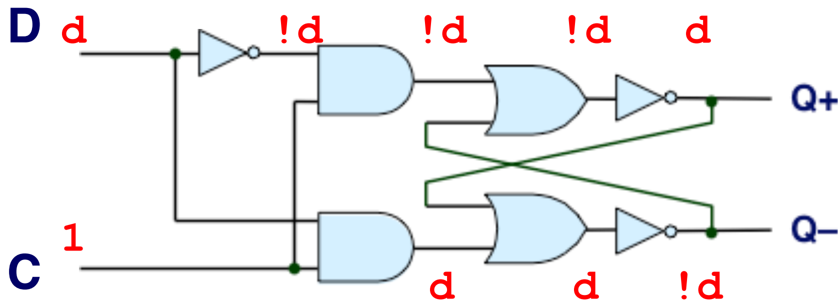

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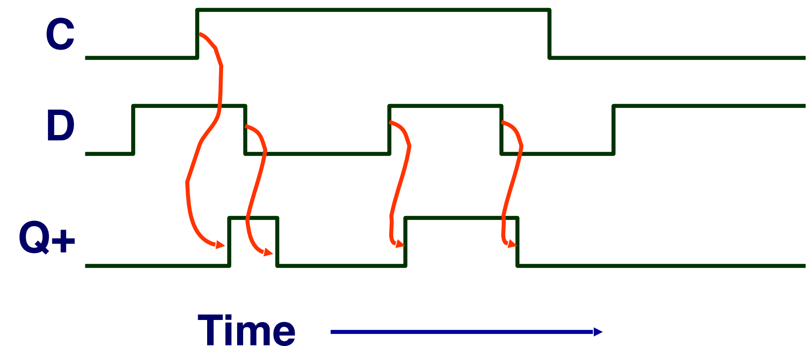

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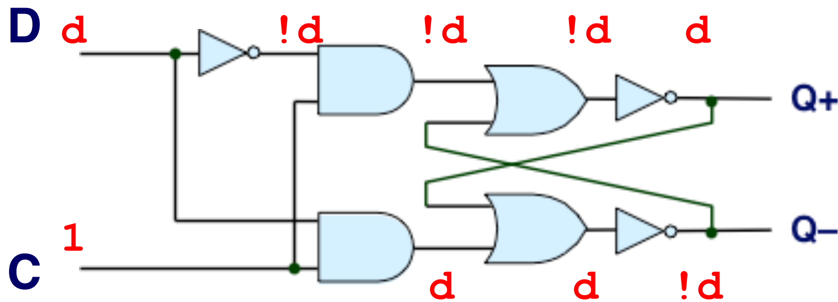

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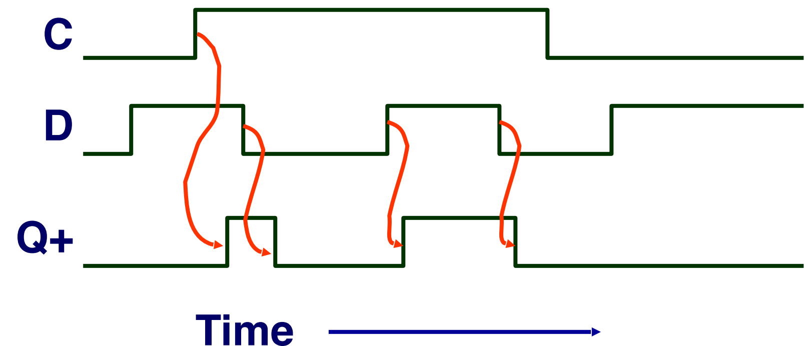

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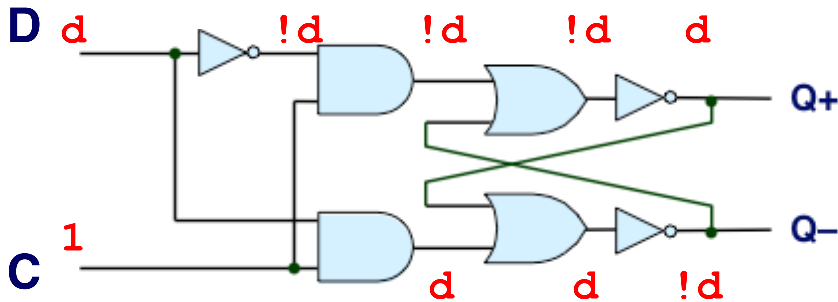

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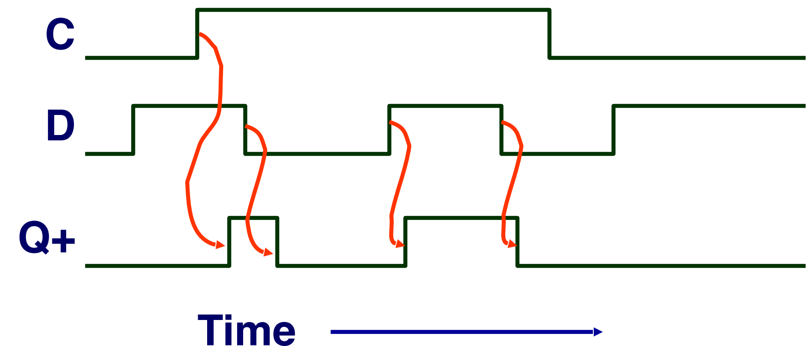

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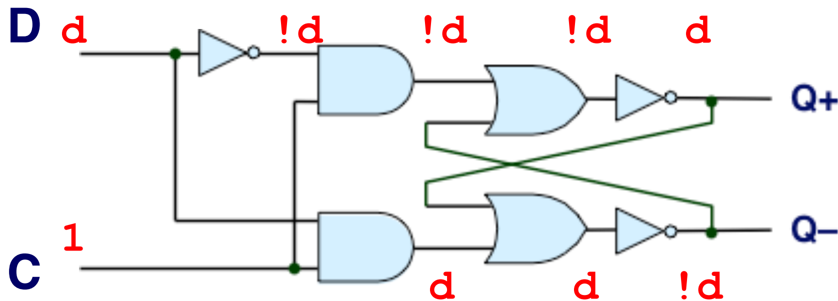
Latching



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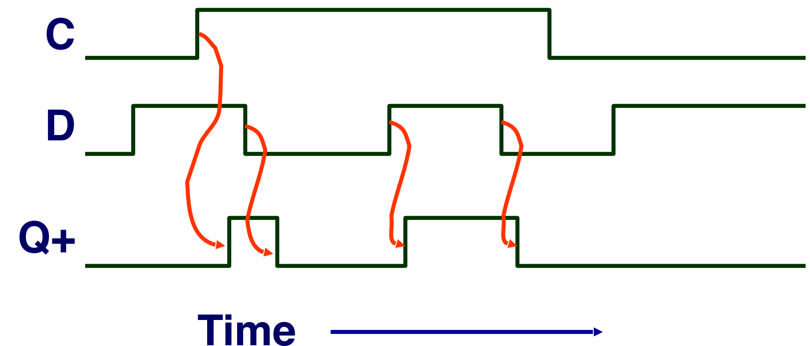

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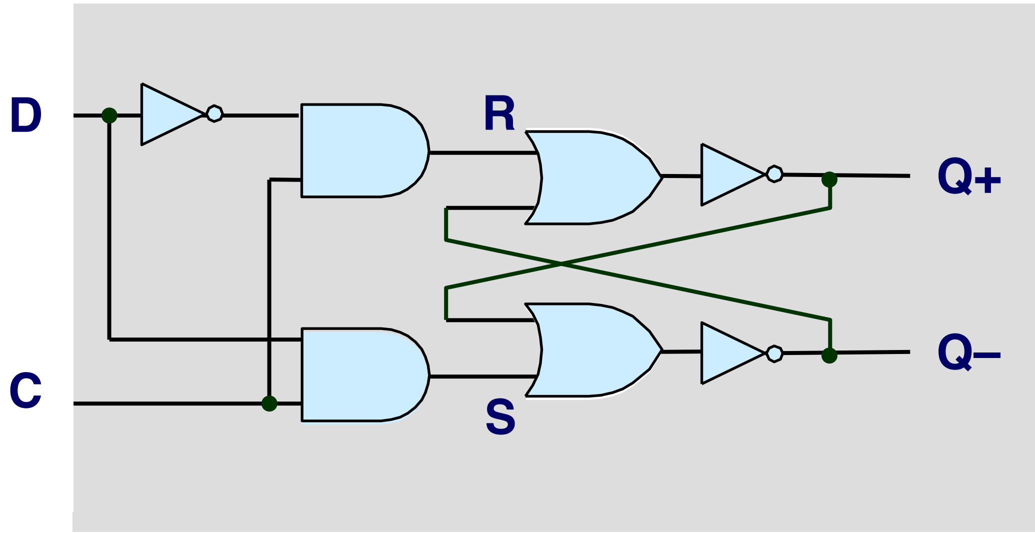
- D-latch is *transparent* when **C** is 1
- D-latch is “*level-triggered*” b/c **Q** changes as the voltage level of **C** rises.

Edge-Triggered Latch (Flip-Flop)



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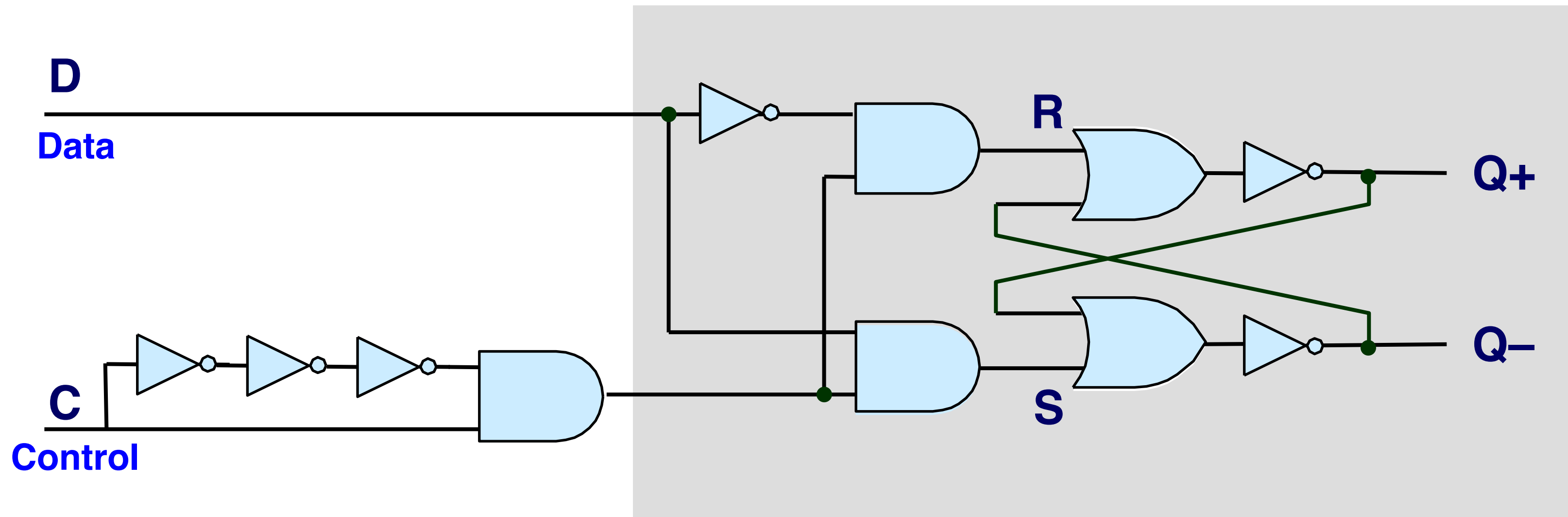

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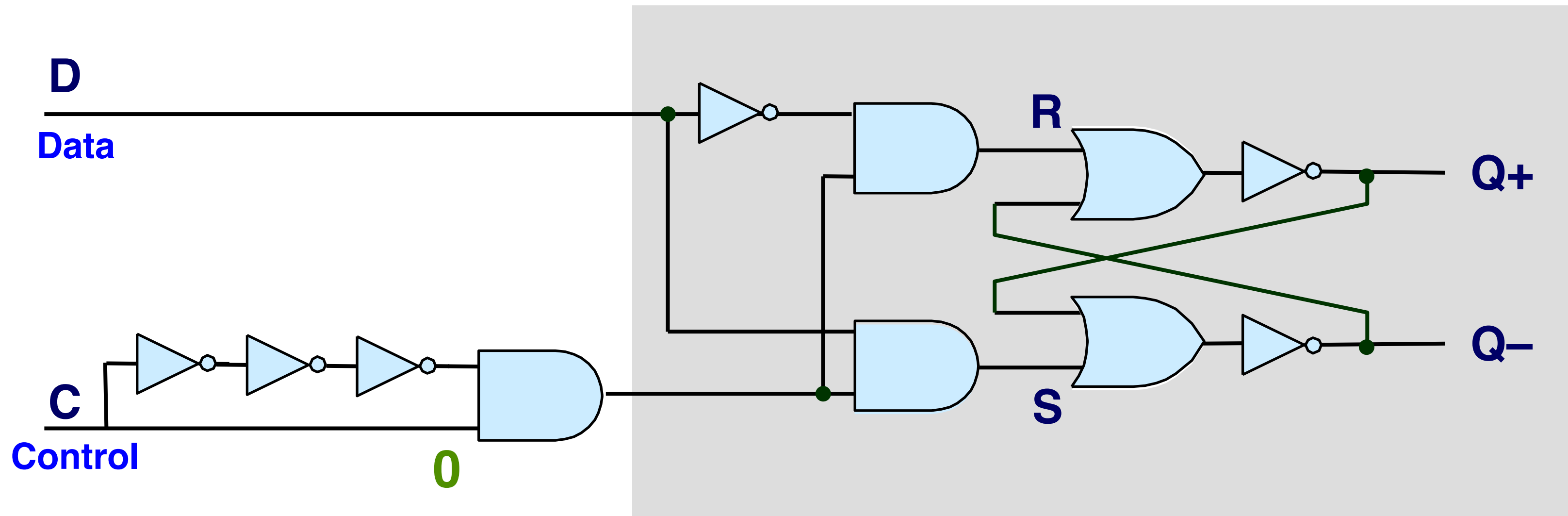

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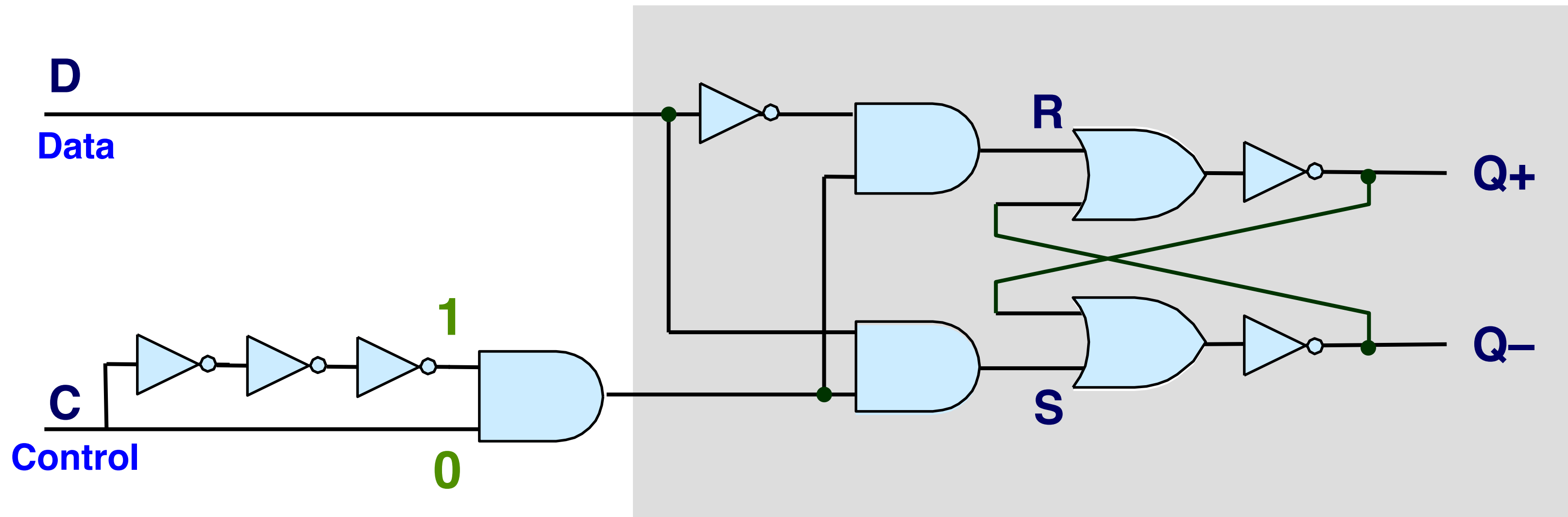

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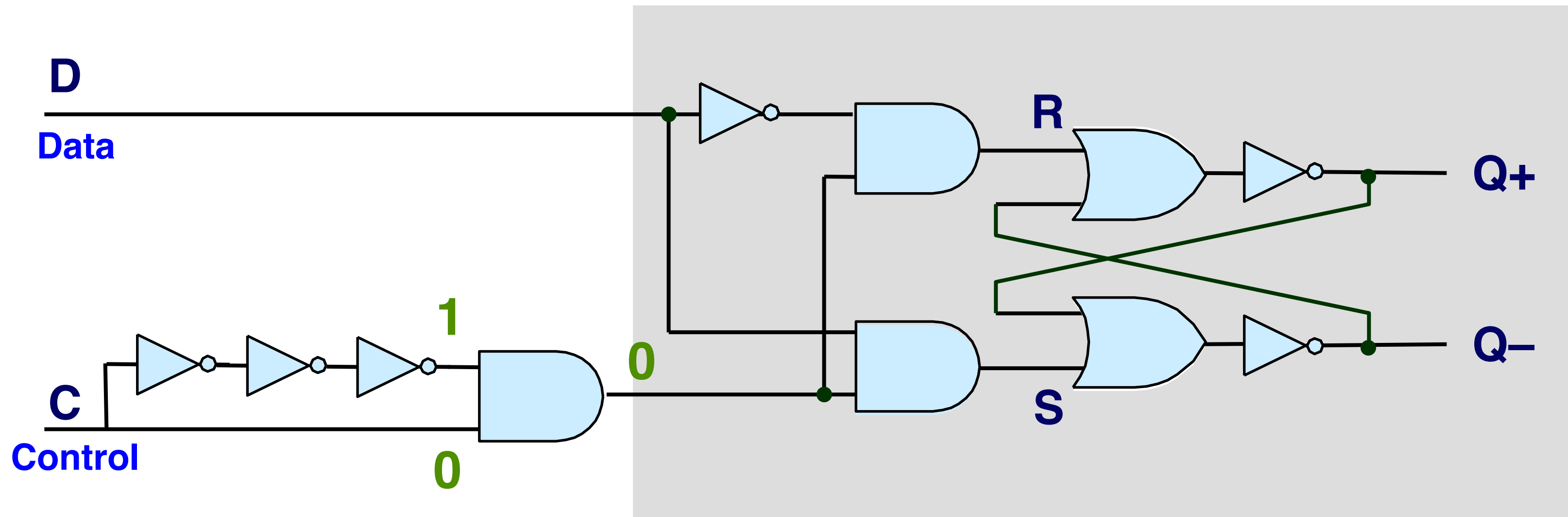

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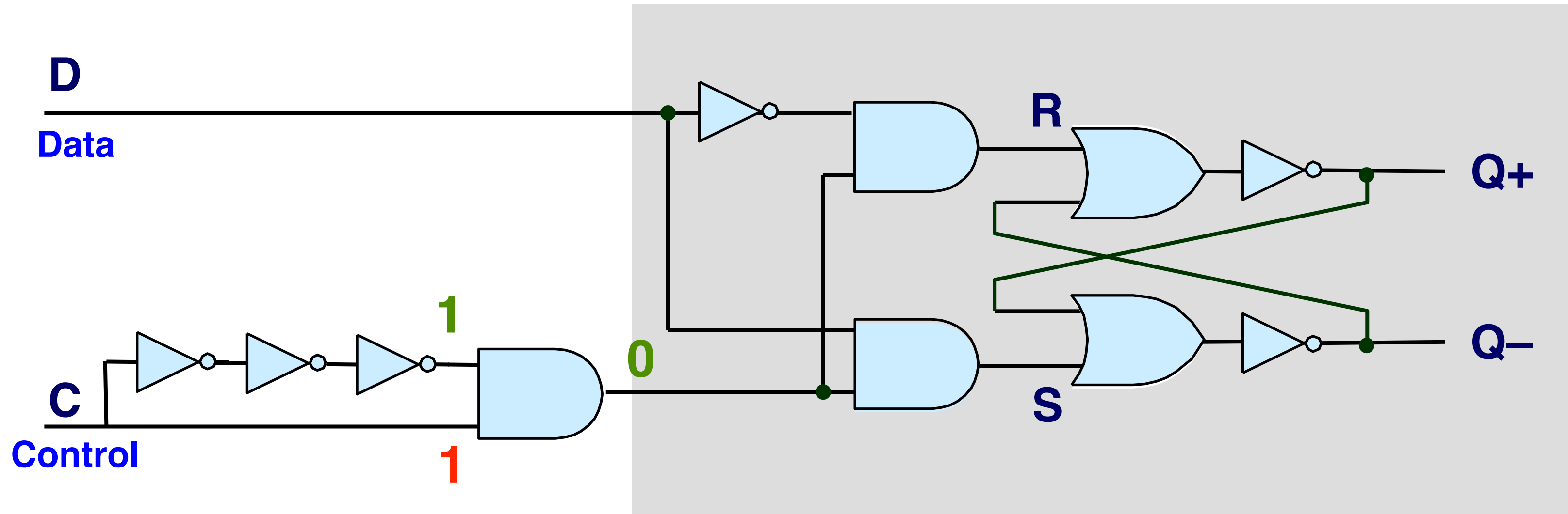

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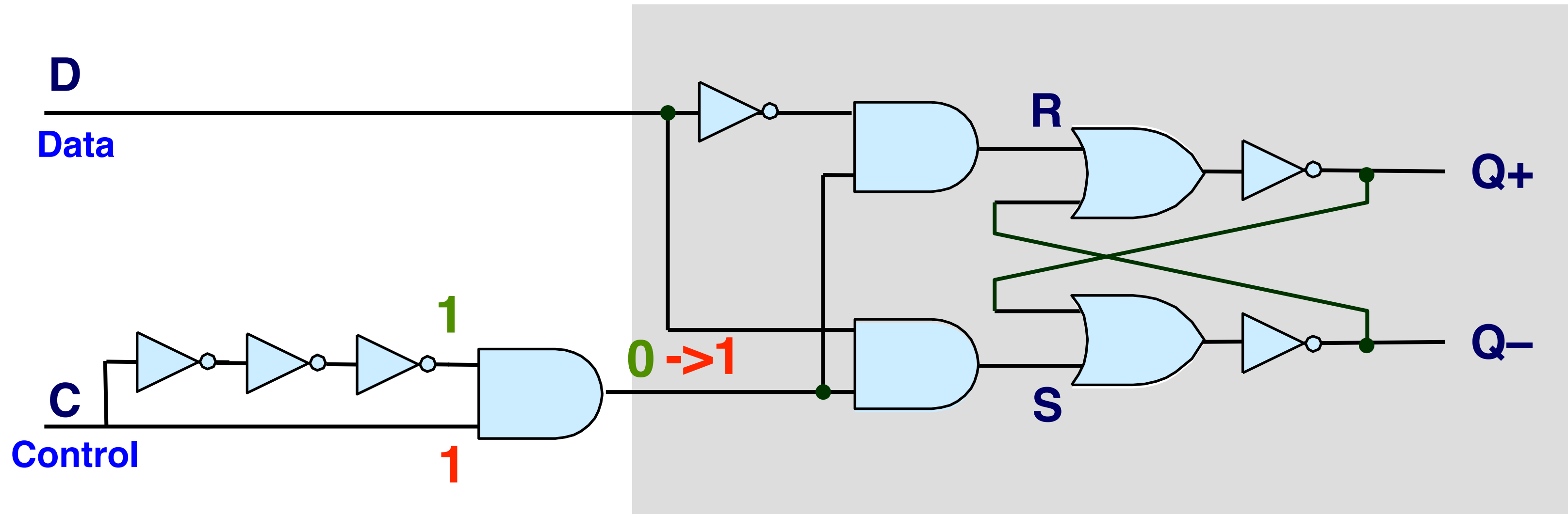

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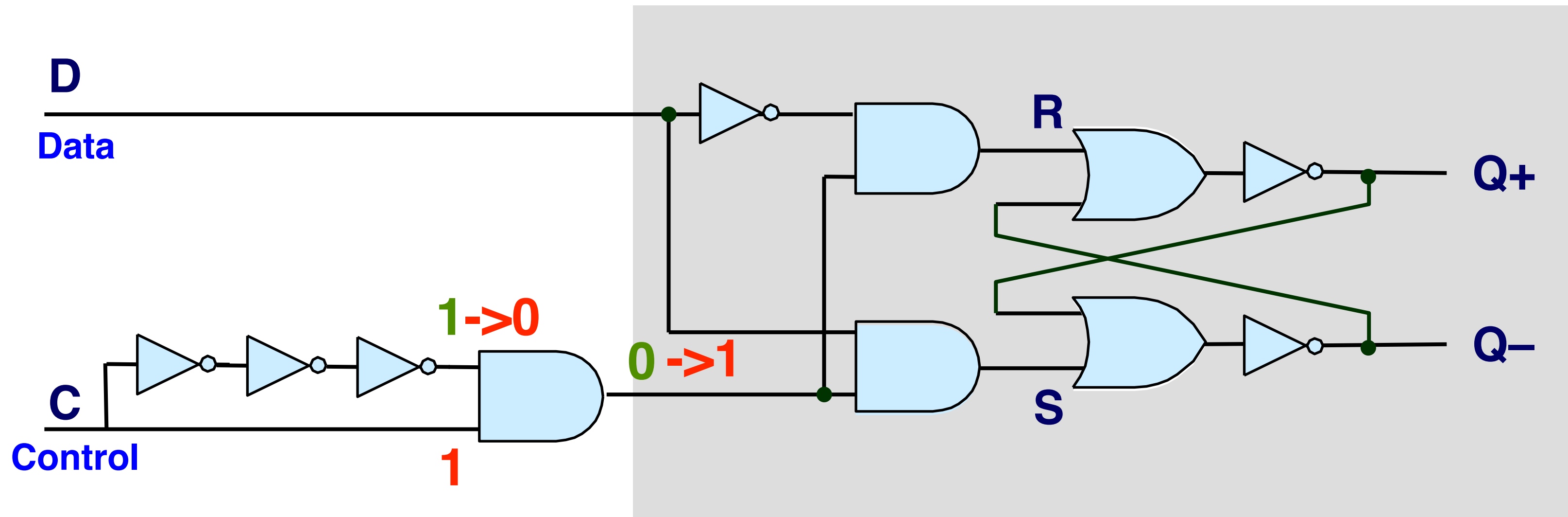

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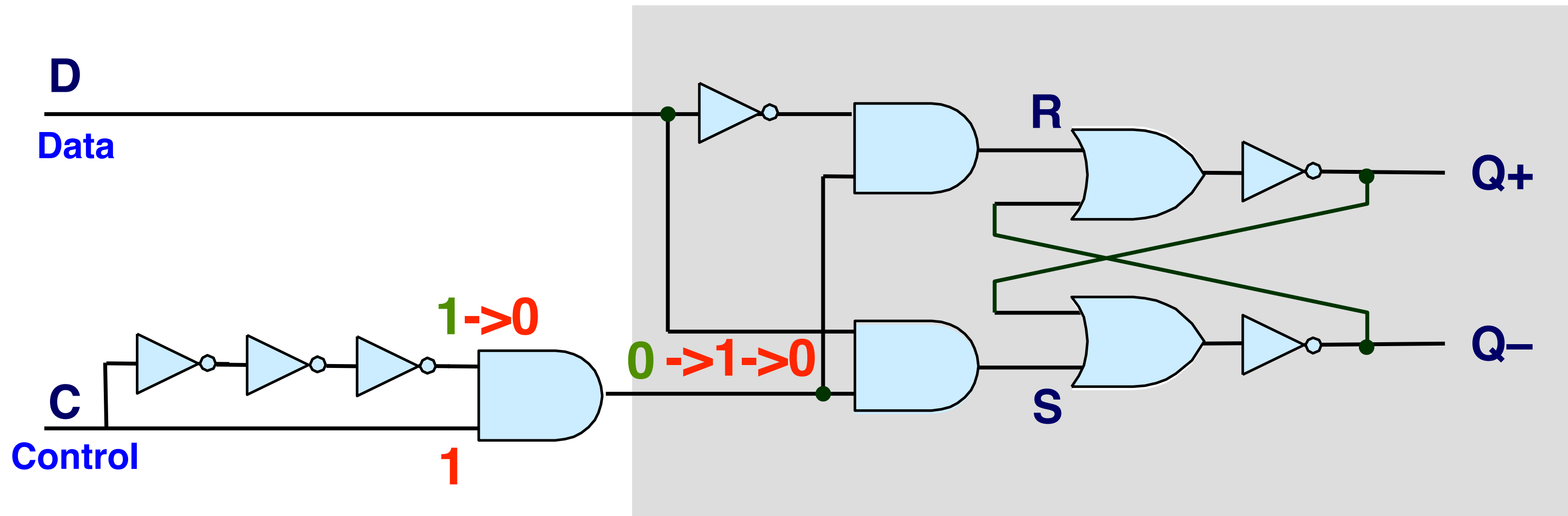

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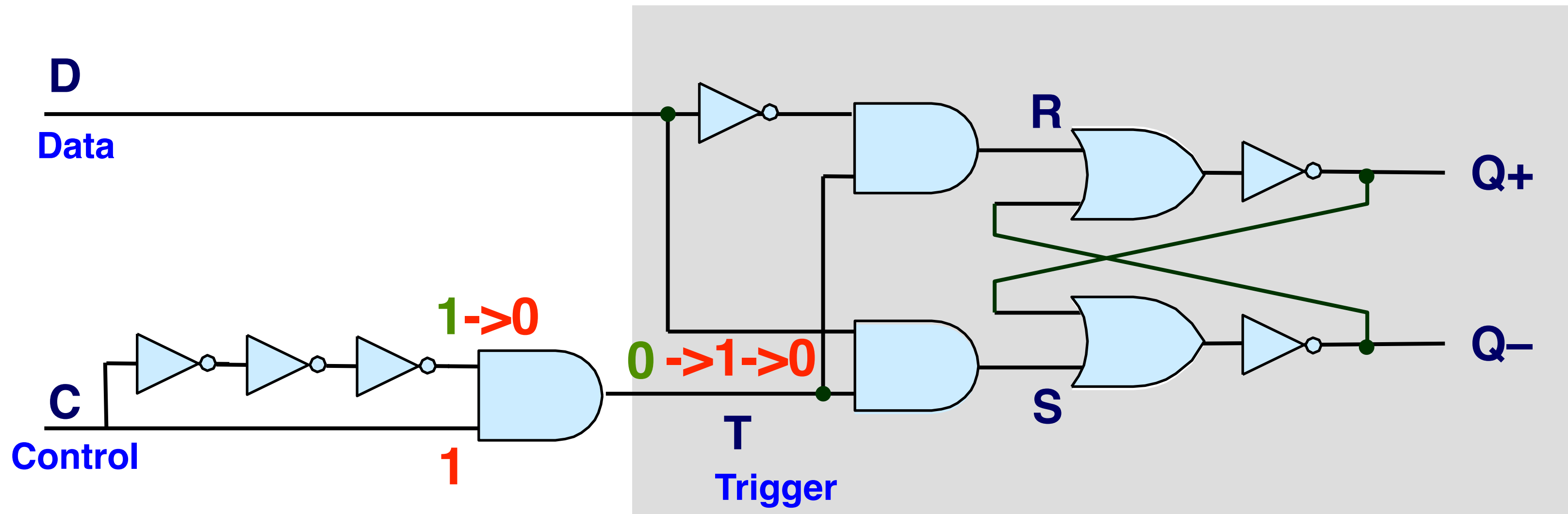

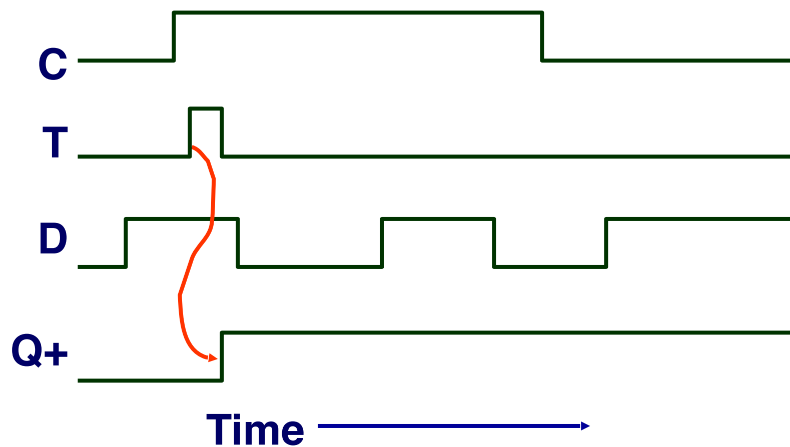

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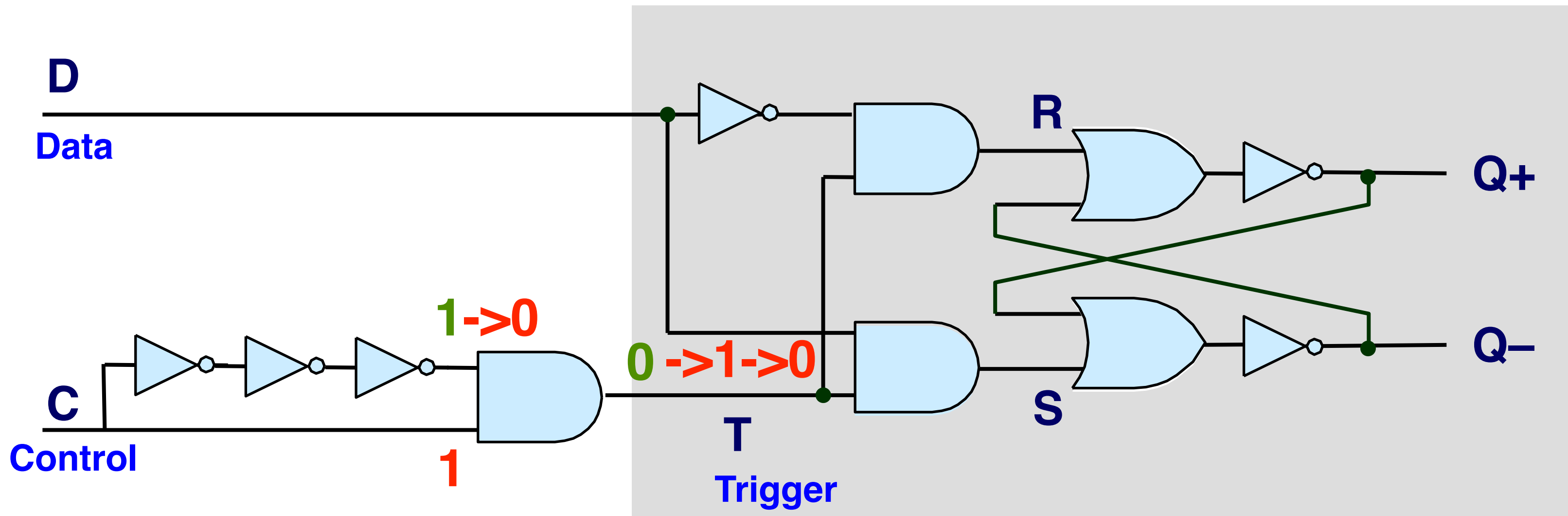
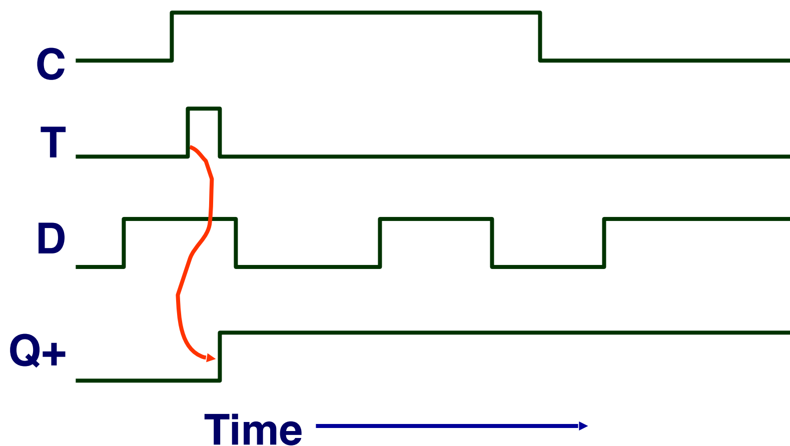
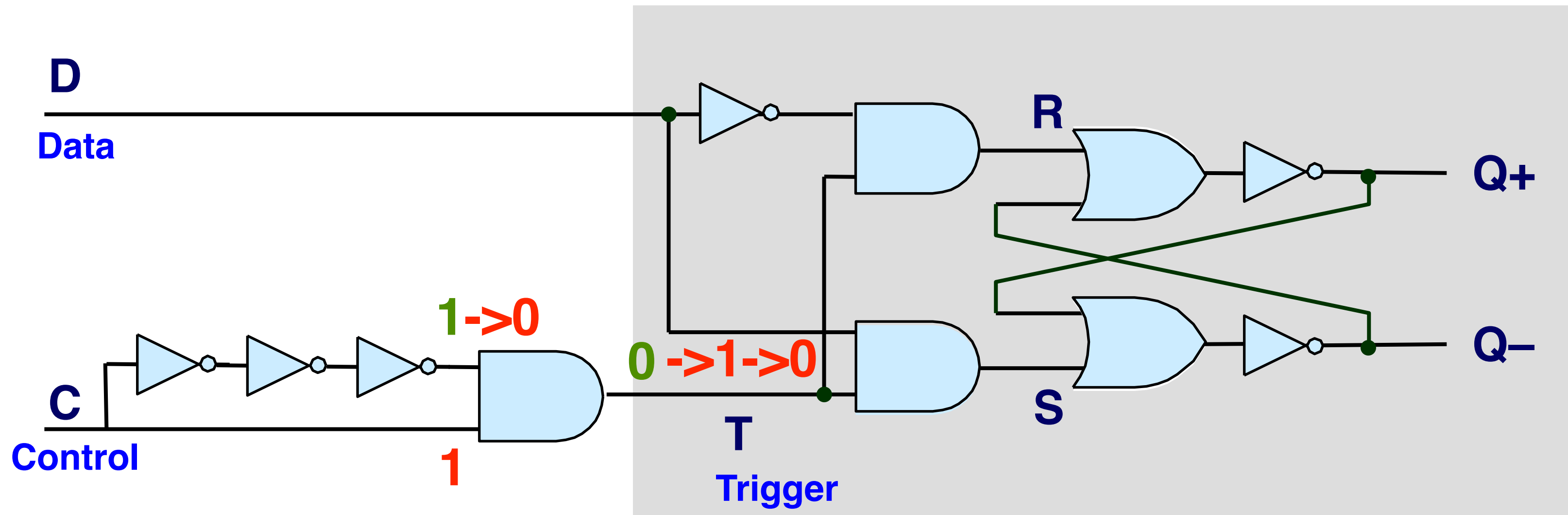
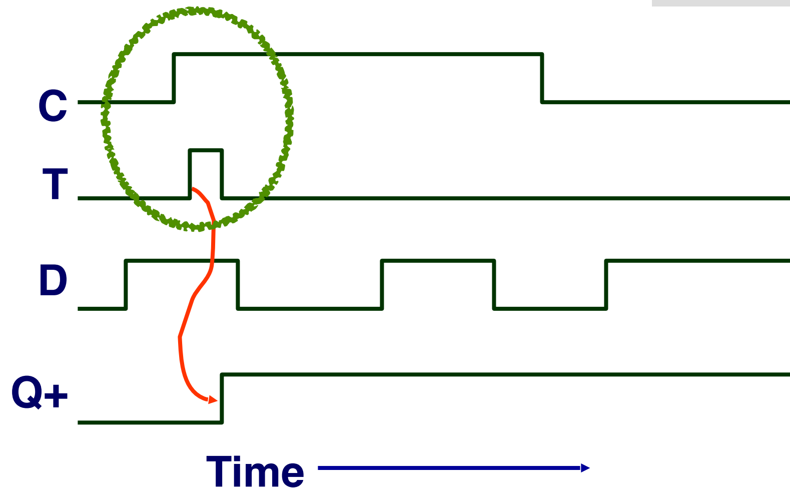




- Flip-flop: Only latches data for a brief period

Edge-Triggered Latch (Flip-Flop)





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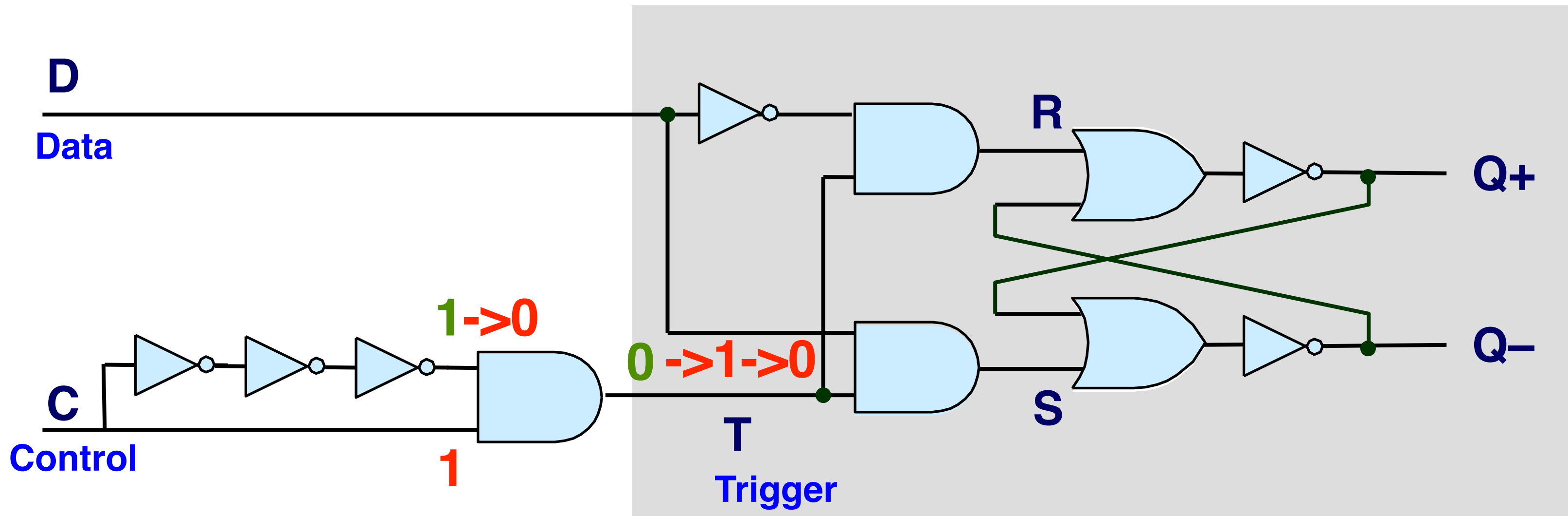

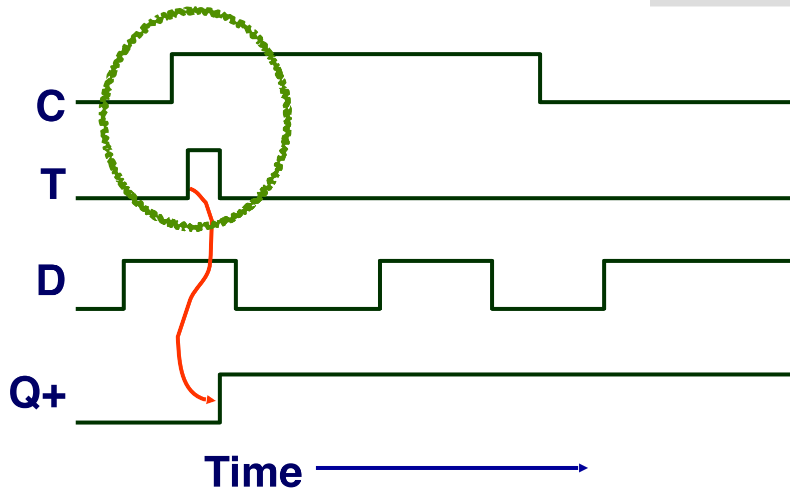

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- Output remains stable at all other times