

CSC 252: Computer Organization

Spring 2022: Lecture 17

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University of Rochester

Cache Placement

Cache

00		
01		
10		
11		

Memory

0000	
0001	
0010	
0011	
0100	
0101	
0110	
0111	
1000	
1001	
1010	
1011	
1100	
1101	
1110	
1111	

- Given a memory addr, say 0x0001, we want to put the data there into the cache; where does the data go?
- How about pick an arbitrary location in cache?
- If so, how do we later find it?

Fully Associative Cache

Cache

00	0xEF		1000
01	0xAC		1001
10	0x06		1010
11	0x70		1101

Content Valid? Tag

Memory

0000	
0001	
0010	
0011	
0100	
0101	
0110	
0111	
1000	0xEF
1001	0xAC
1010	0x06
1011	
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1101	0x70
1110	
1111	

- Every memory location can be mapped to any cache line in the cache.

Fully Associative Cache

Cache

00	0xEF		1000
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Content Valid? Tag

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- Every memory location can be mapped to any cache line in the cache.
- Given a request to address A from the CPU, detecting cache hit/miss requires:
 - Comparing address A with all four tags in the cache (a.k.a., associative search)

Fully Associative Cache

Cache

00	0xEF		1000
01	0xAC		1001
10	0x06		1010
11	0x70		1101

Content Valid? Tag

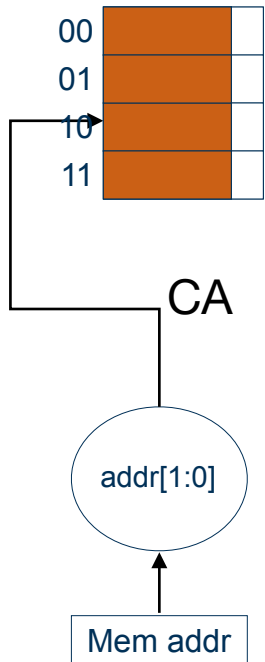
Memory

0000	
0001	
0010	
0011	
0100	
0101	
0110	
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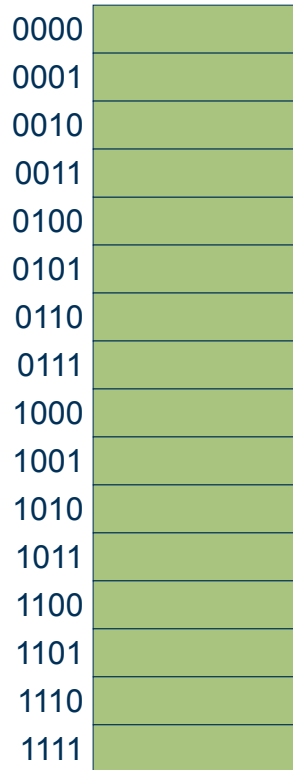
- Every memory location can be mapped to any cache line in the cache.
- Given a request to address A from the CPU, detecting cache hit/miss requires:
 - Comparing address A with all four tags in the cache (a.k.a., associative search)
- Can we reduce the overhead?

Direct-Mapped Cache

Cache



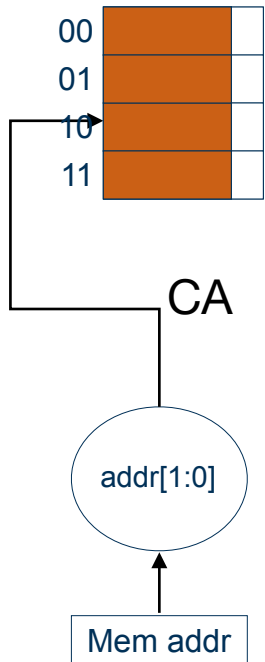
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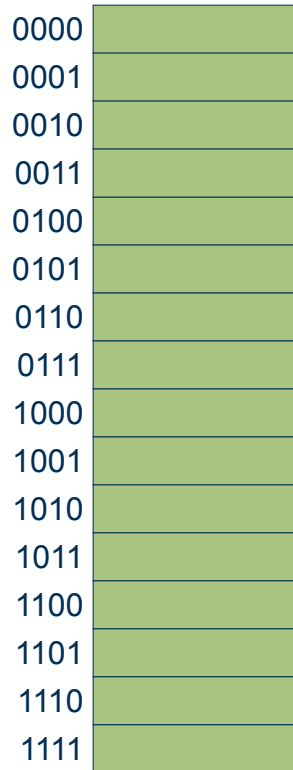
- Direct-Mapped Cache
 - $CA = ADDR[1], ADDR[0]$
- Multiple addresses can be mapped to the same location

Direct-Mapped Cache

Cache



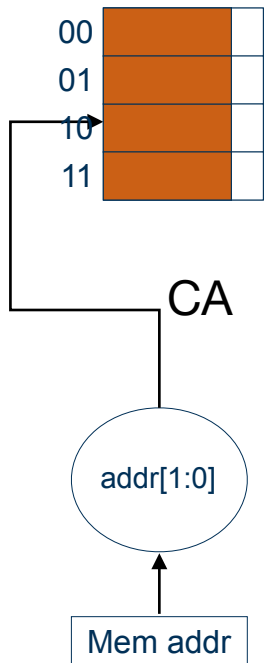
Memory



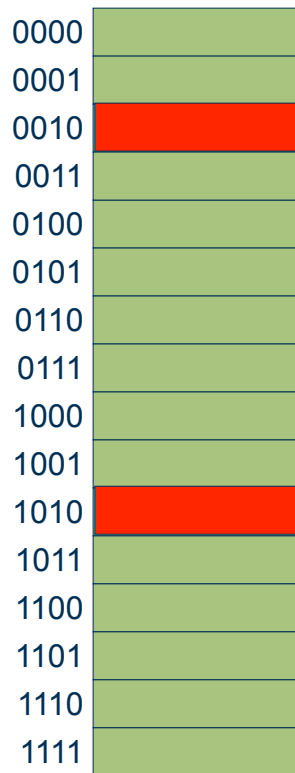
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 - E.g., 0010 and 1010

Direct-Mapped Cache

Cache

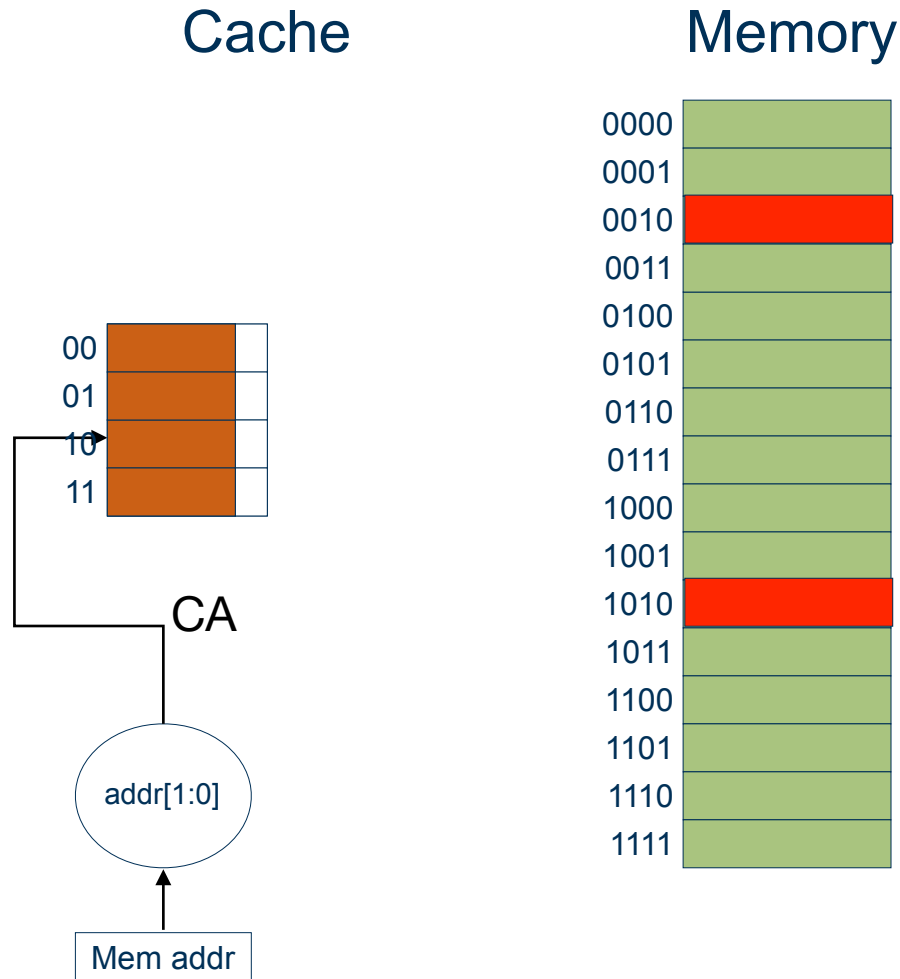


Memory



- Direct-Mapped Cache
 - $CA = ADDR[1], ADDR[0]$
- Multiple addresses can be mapped to the same location
 - E.g., 0010 and 1010
- How do we differentiate between different memory locations that are mapped to the same cache location?

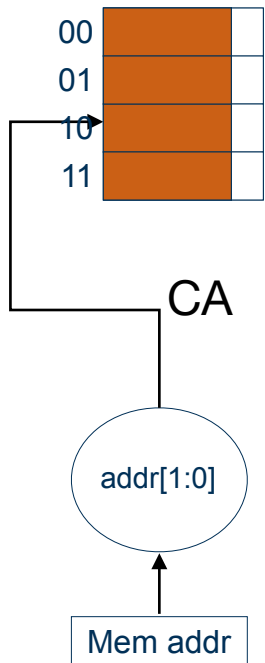
Direct-Mapped Cache



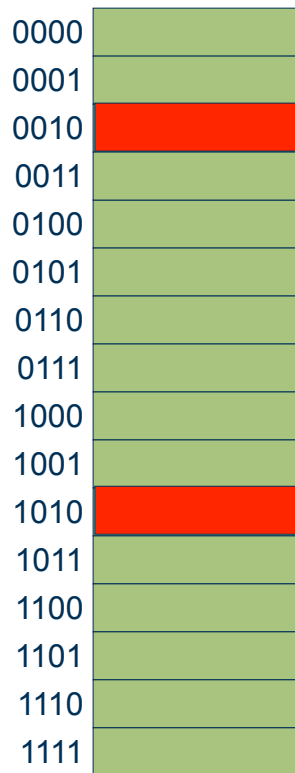
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 - Add a tag field for that purpose

Direct-Mapped Cache

Cache



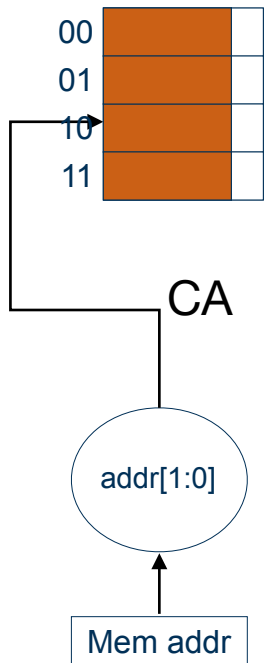
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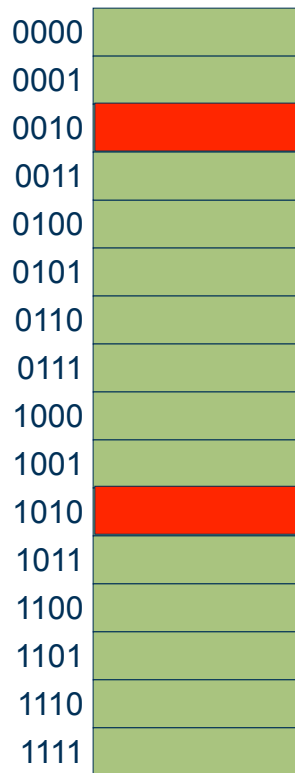
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Direct-Mapped Cache

Cache

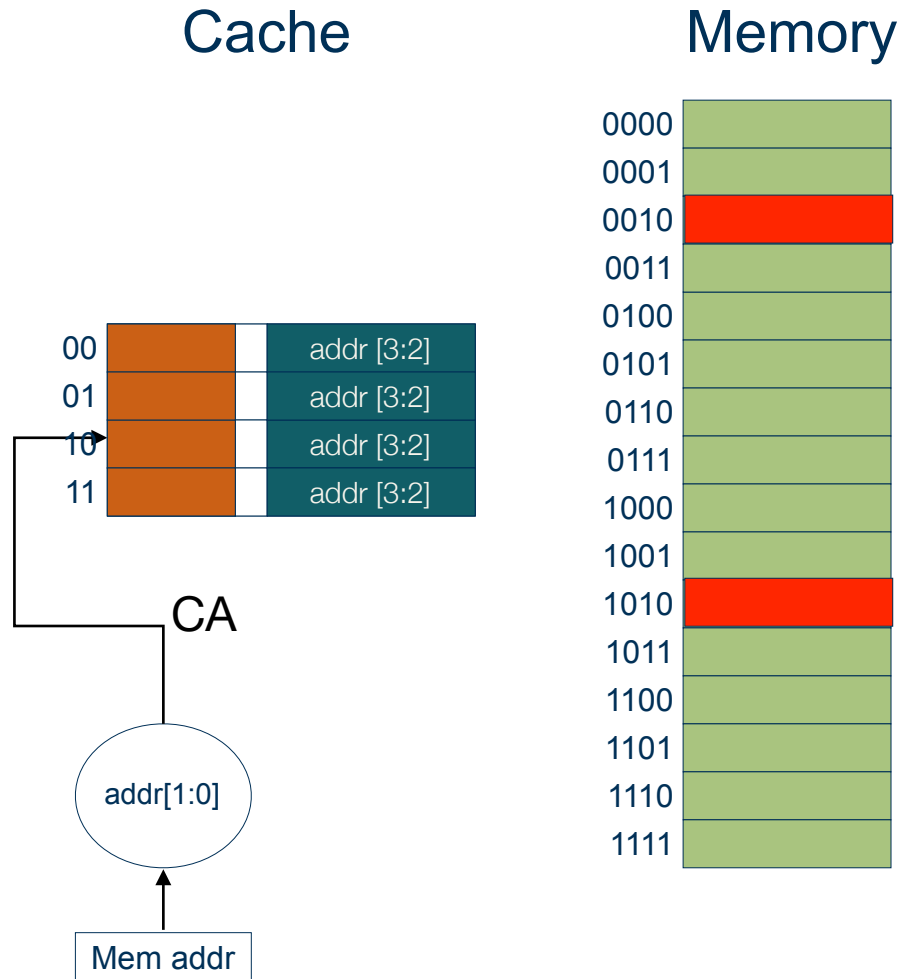


Memory



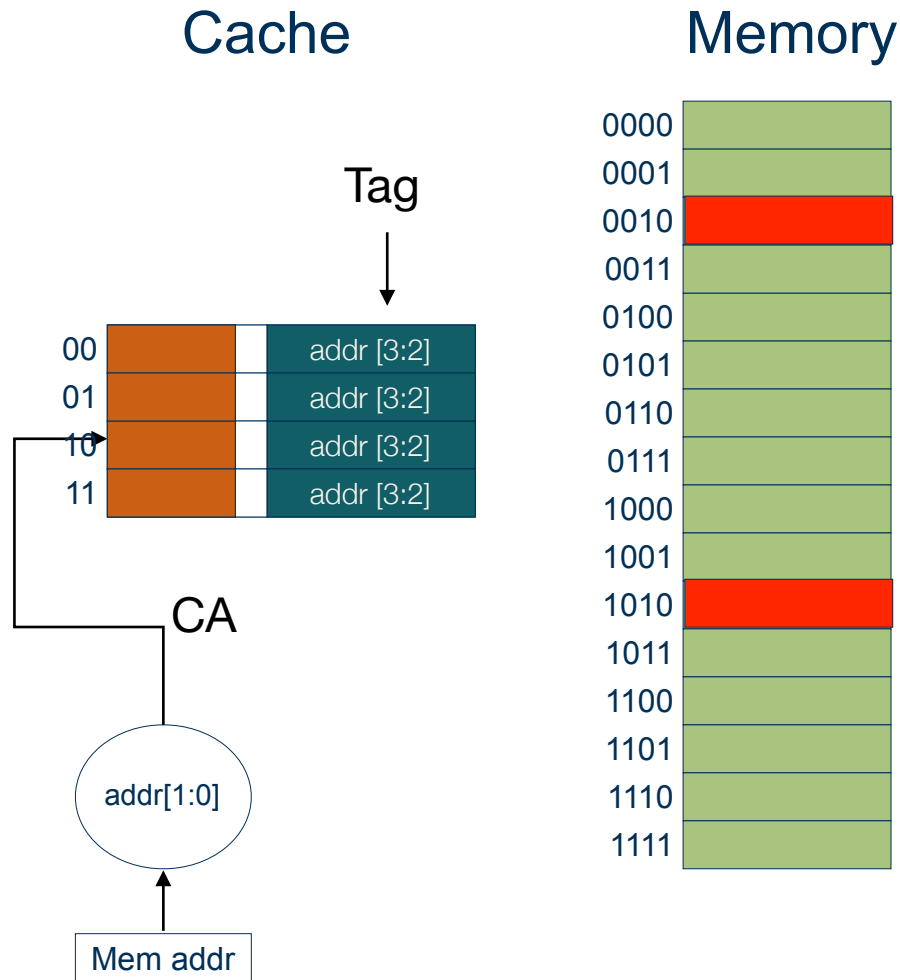
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 - Add a tag field for that purpose
 - What should the tag field be?
 - $ADDR[3]$ and $ADDR[2]$ in this particular example

Direct-Mapped Cache



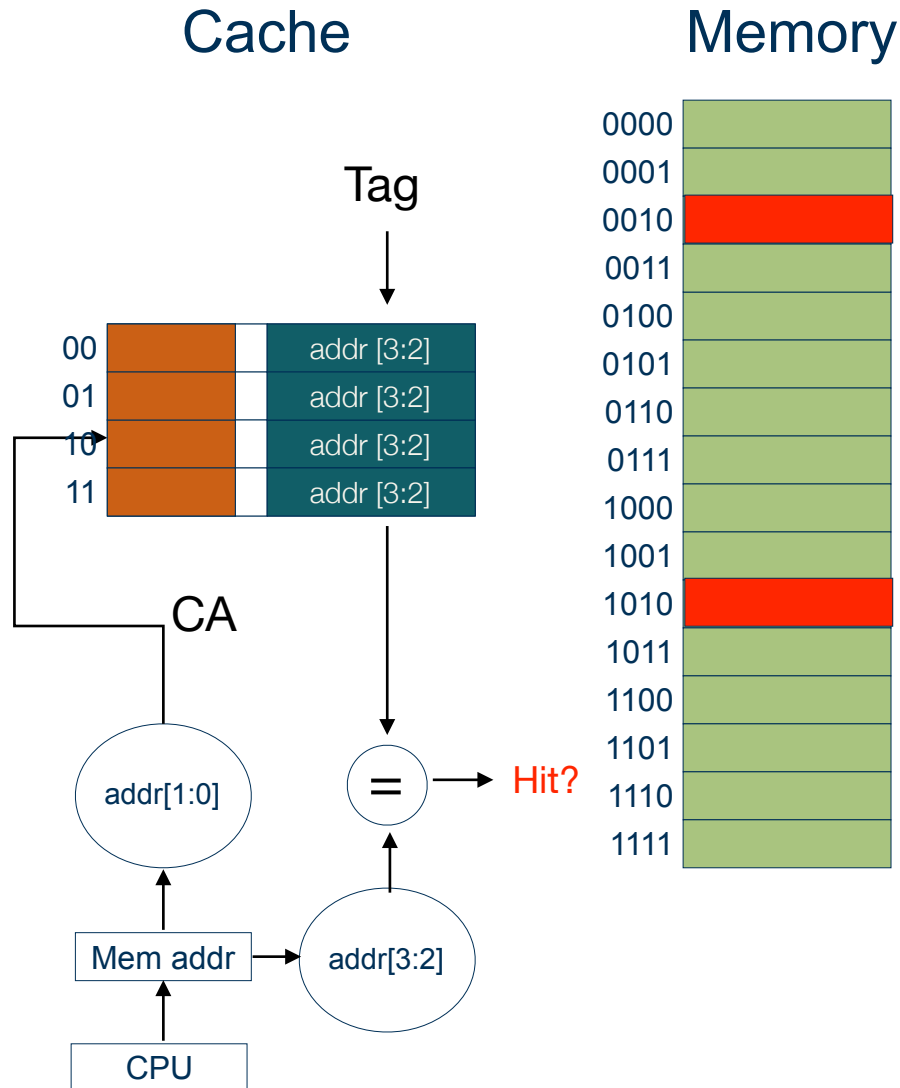
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Direct-Mapped Cache



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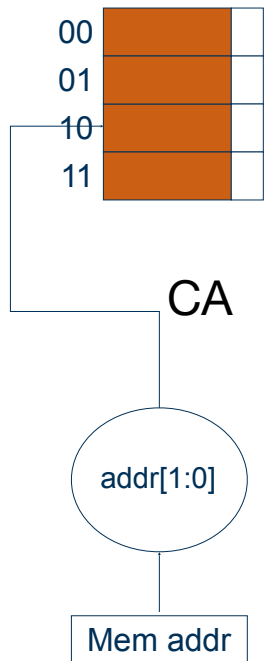
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Direct-Mapped Cache

Cache

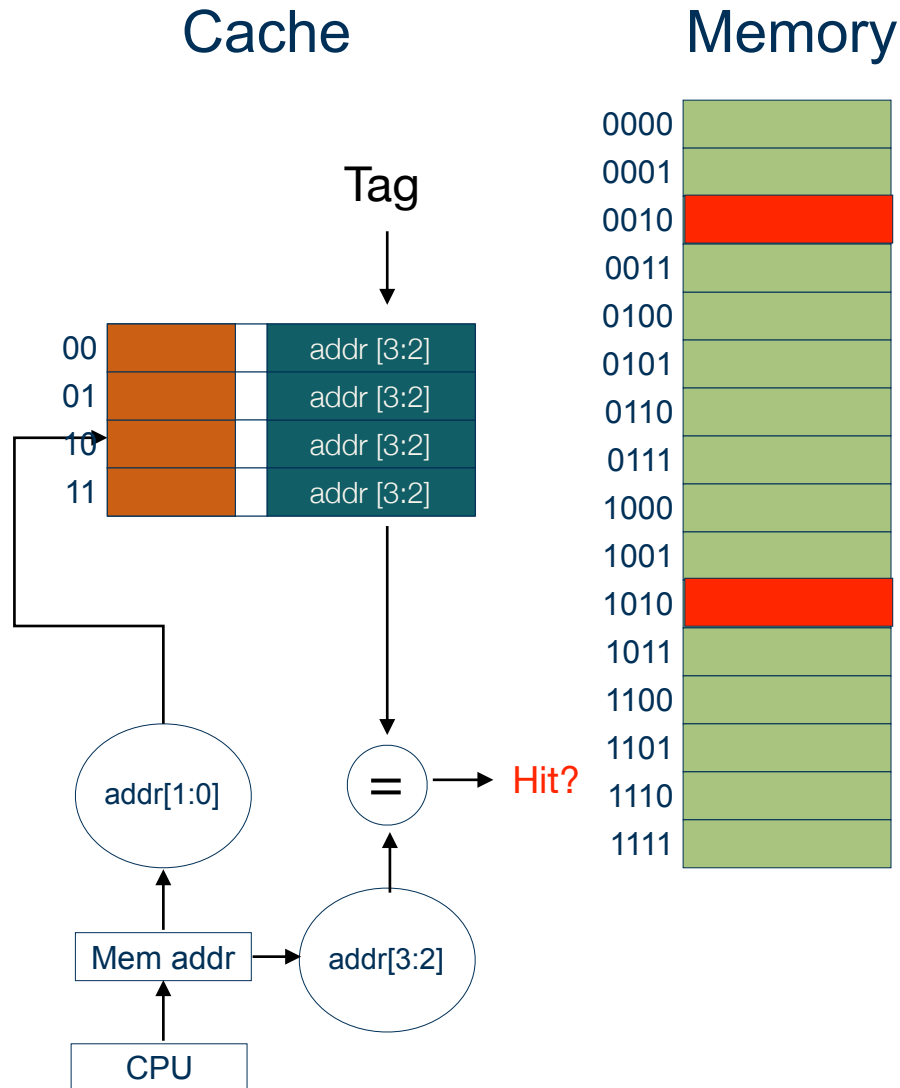


Memory

0000	
0001	
0010	
0011	
0100	
0101	
0110	
0111	
1000	
1001	
1010	
1011	
1100	
1101	
1110	
1111	

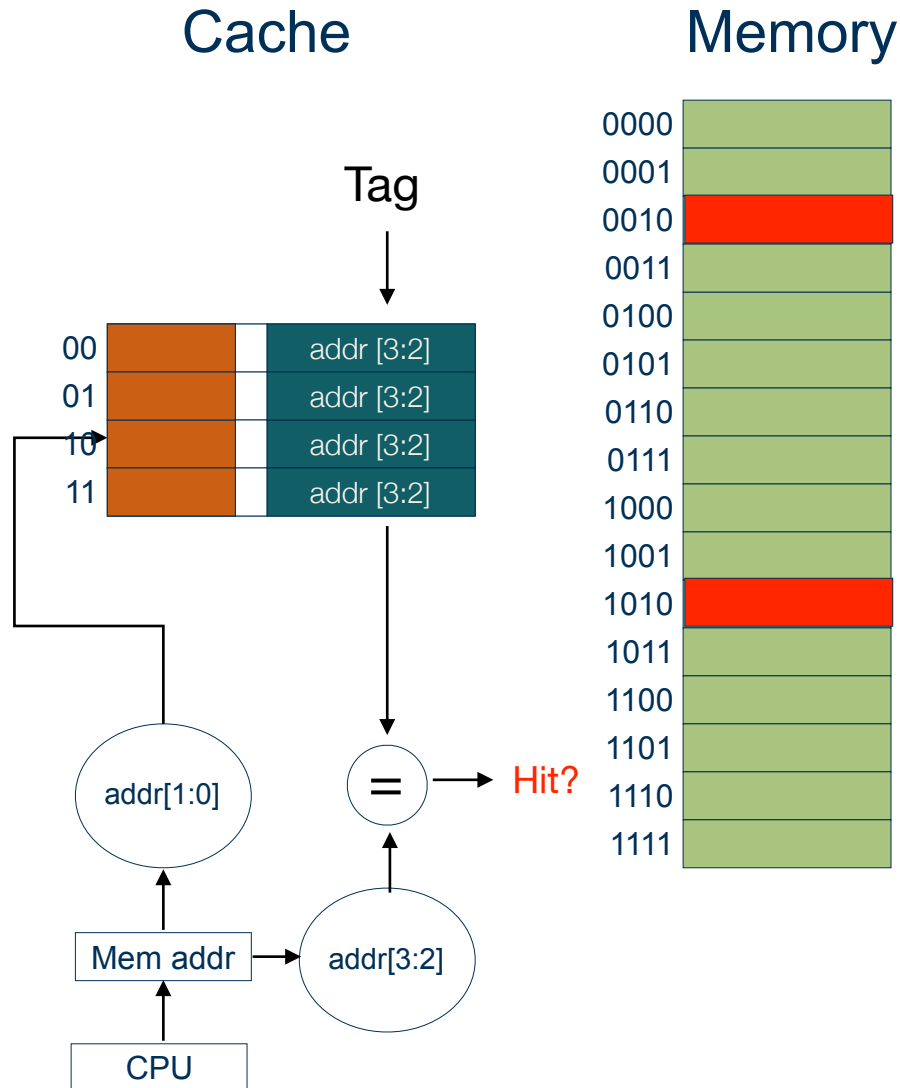
- Why use the lower two bits?
- Six combinations in total
 - $CA = ADDR[3], ADDR[2]$
 - $CA = ADDR[3], ADDR[1]$
 - $CA = ADDR[3], ADDR[0]$
 - $CA = ADDR[2], ADDR[1]$
 - $CA = ADDR[2], ADDR[0]$
 - $CA = ADDR[1], ADDR[0]$
- How about using $ADDR[3]$, $ADDR[2]$?

Direct-Mapped Cache



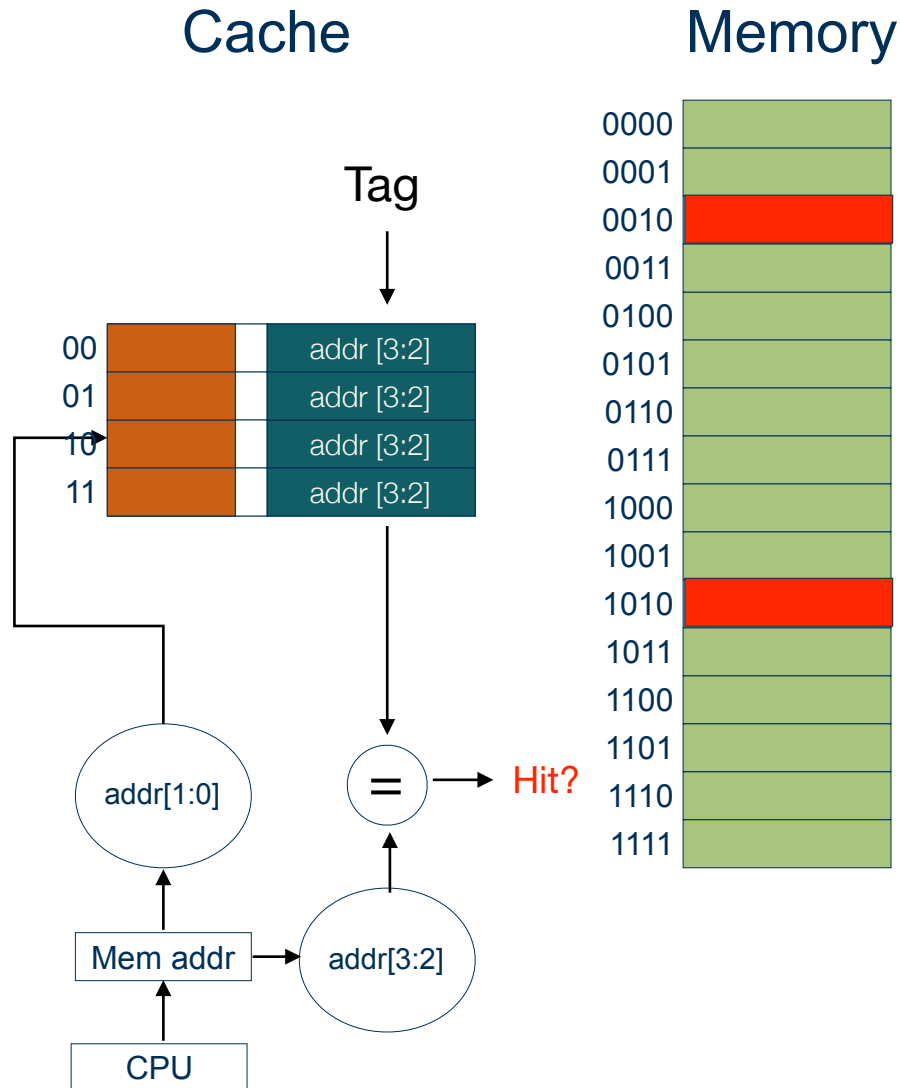
- Limitation: each memory location can be mapped to only one cache location.

Direct-Mapped Cache



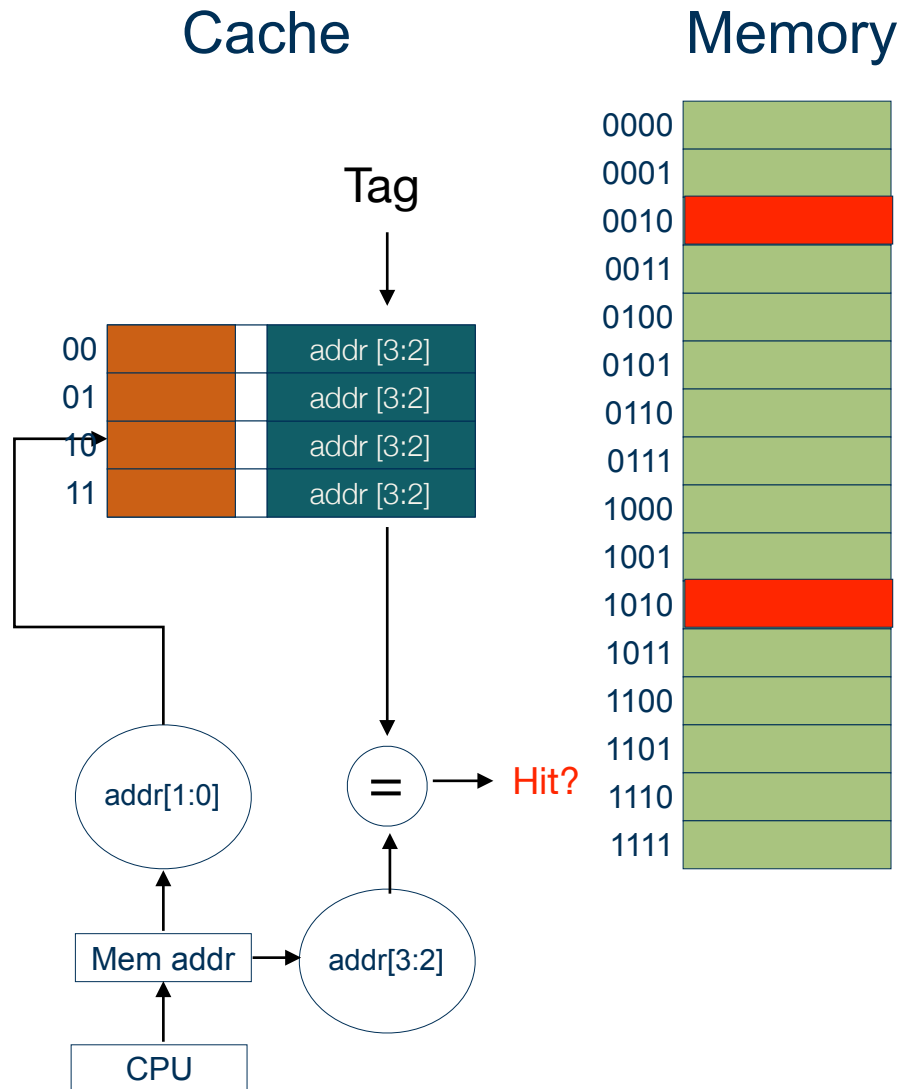
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- This leads to a lot of conflicts.

Direct-Mapped Cache



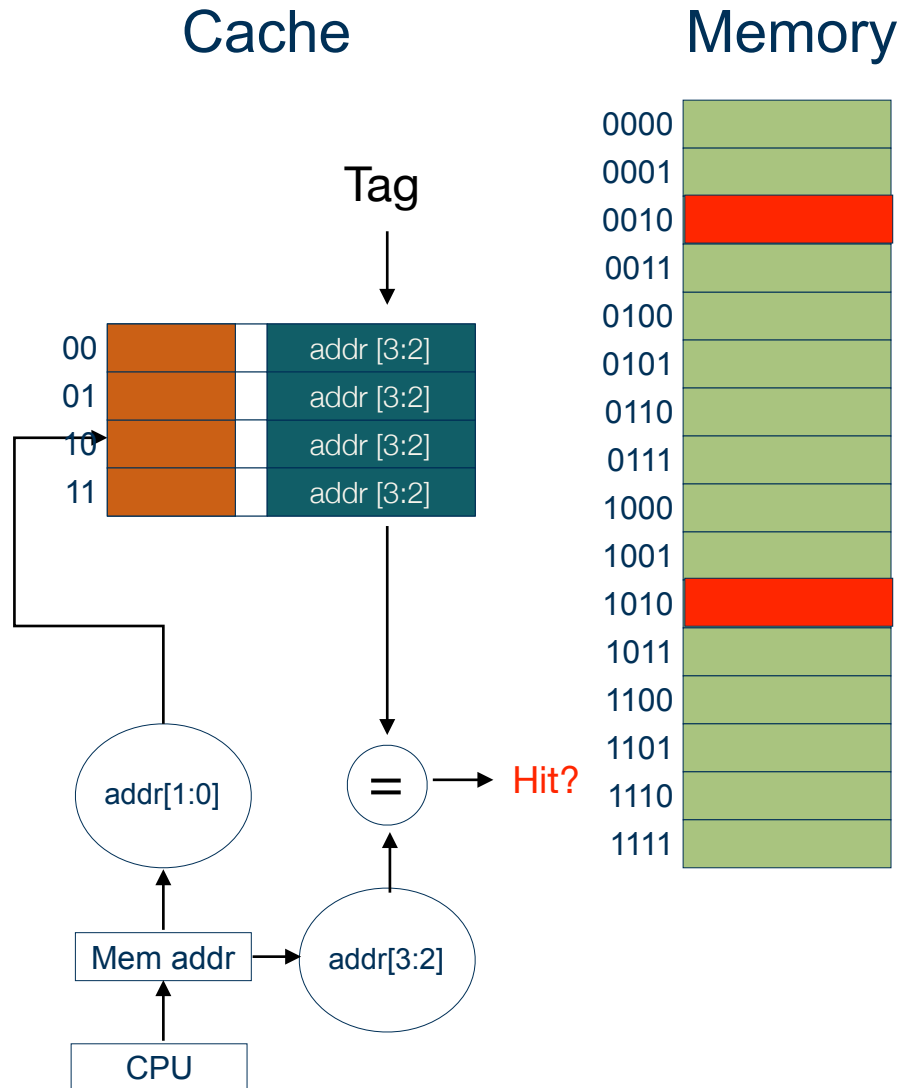
- Limitation: each memory location can be mapped to only one cache location.
- This leads to a lot of conflicts.
- How do we improve this?

Direct-Mapped Cache



- Limitation: each memory location can be mapped to only one cache location.
- This leads to a lot of conflicts.
- How do we improve this?
- Can each memory location have the flexibility to be mapped to different cache locations?

Direct-Mapped Cache



- Limitation: each memory location can be mapped to only one cache location.
- This leads to a lot of conflicts.
- How do we improve this?
- Can each memory location have the flexibility to be mapped to different cache locations?
 - Fully associative cache does this, but comes with the overhead of requiring more comparisons.

A Middle Ground: 2-Way Associative Cache



- 4 cache lines are organized into two sets; each set has 2 cache lines (i.e., 2 ways)

0000	
0001	
0010	
0011	
0100	
0101	
0110	
0111	
1000	0xEF
1001	0xAC
1010	0x06
1011	
1100	
1101	0x70
1110	
1111	

A Middle Ground: 2-Way Associative Cache



- 4 cache lines are organized into two sets; each set has 2 cache lines (i.e., 2 ways)
- Even address go to first set and odd addresses go to the second set

0000	
0001	
0010	
0011	
0100	
0101	
0110	
0111	
1000	0xEF
1001	0xAC
1010	0x06
1011	
1100	
1101	0x70
1110	
1111	

A Middle Ground: 2-Way Associative Cache



- 4 cache lines are organized into two sets; each set has 2 cache lines (i.e., 2 ways)
- Even address go to first set and odd addresses go to the second set
- Each address can be mapped to either cache line in the same set
 - Using the LSB to find the set (i.e., odd vs. even)
 - Tag now stores the higher 3 bits instead of the entire address

0000	
0001	
0010	
0011	
0100	
0101	
0110	
0111	
1000	0xEF
1001	0xAC
1010	0x06
1011	
1100	
1101	0x70
1110	
1111	

2-Way Associative Cache



- Given a request to address, say 1011, from the CPU, detecting cache hit/miss requires:

0000	
0001	
0010	
0011	
0100	
0101	
0110	
0111	
1000	0xEF
1001	0xAC
1010	0x06
1011	
1100	
1101	0x70
1110	
1111	

2-Way Associative Cache



- Given a request to address, say 1011, from the CPU, detecting cache hit/miss requires:
 - Using the LSB to index into the cache and find the corresponding set, in this case set 1

0000	
0001	
0010	
0011	
0100	
0101	
0110	
0111	
1000	0xEF
1001	0xAC
1010	0x06
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1110	
1111	

2-Way Associative Cache



- Given a request to address, say 1011, from the CPU, detecting cache hit/miss requires:
 - Using the LSB to index into the cache and find the corresponding set, in this case set 1
 - Then do an associative search in that set, i.e., compare the highest 3 bits 101 with both tags in set 1

0000	
0001	
0010	
0011	
0100	
0101	
0110	
0111	
1000	0xEF
1001	0xAC
1010	0x06
1011	
1100	
1101	0x70
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2-Way Associative Cache



- Given a request to address, say 1011, from the CPU, detecting cache hit/miss requires:
 - Using the LSB to index into the cache and find the corresponding set, in this case set 1
 - Then do an associative search in that set, i.e., compare the highest 3 bits 101 with both tags in set 1
 - Only two comparisons required

0000	
0001	
0010	
0011	
0100	
0101	
0110	
0111	
1000	0xEF
1001	0xAC
1010	0x06
1011	
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1110	
1111	

Direct-Mapped (1-way Associative) Cache

00	0xEF		10
01	0xAC		10
10	0x06		10
11			

Content Valid? Tag

- 4 cache lines are organized into four sets
- Each memory localization can only be mapped to one set
 - Using the 2 LSBs to find the set
 - Tag now stores the higher 2 bits

0000	
0001	
0010	
0011	
0100	
0101	
0110	
0111	
1000	0xEF
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1011	
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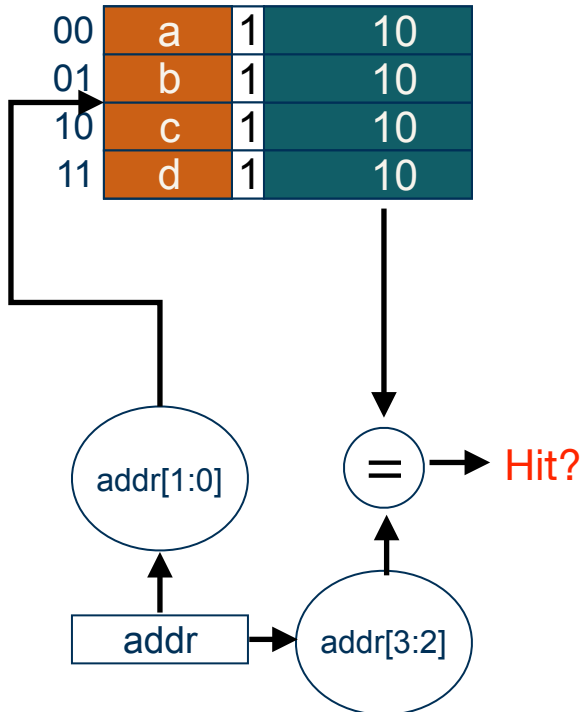
Associative verses Direct Mapped Trade-offs

Associative verses Direct Mapped Trade-offs

- Direct-Mapped cache
 - Generally lower hit rate
 - Simpler, Faster

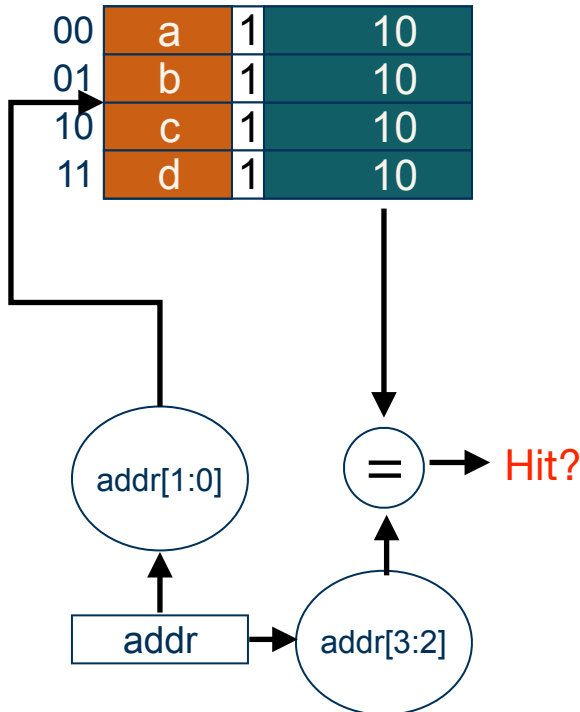
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Associative verses Direct Mapped Trade-offs

- Direct-Mapped cache
 - Generally lower hit rate
 - Simpler, Faster
- Associative cache
 - Generally higher hit rate. Better utilization of cache resources
 - Slower and higher power consumption. Why?

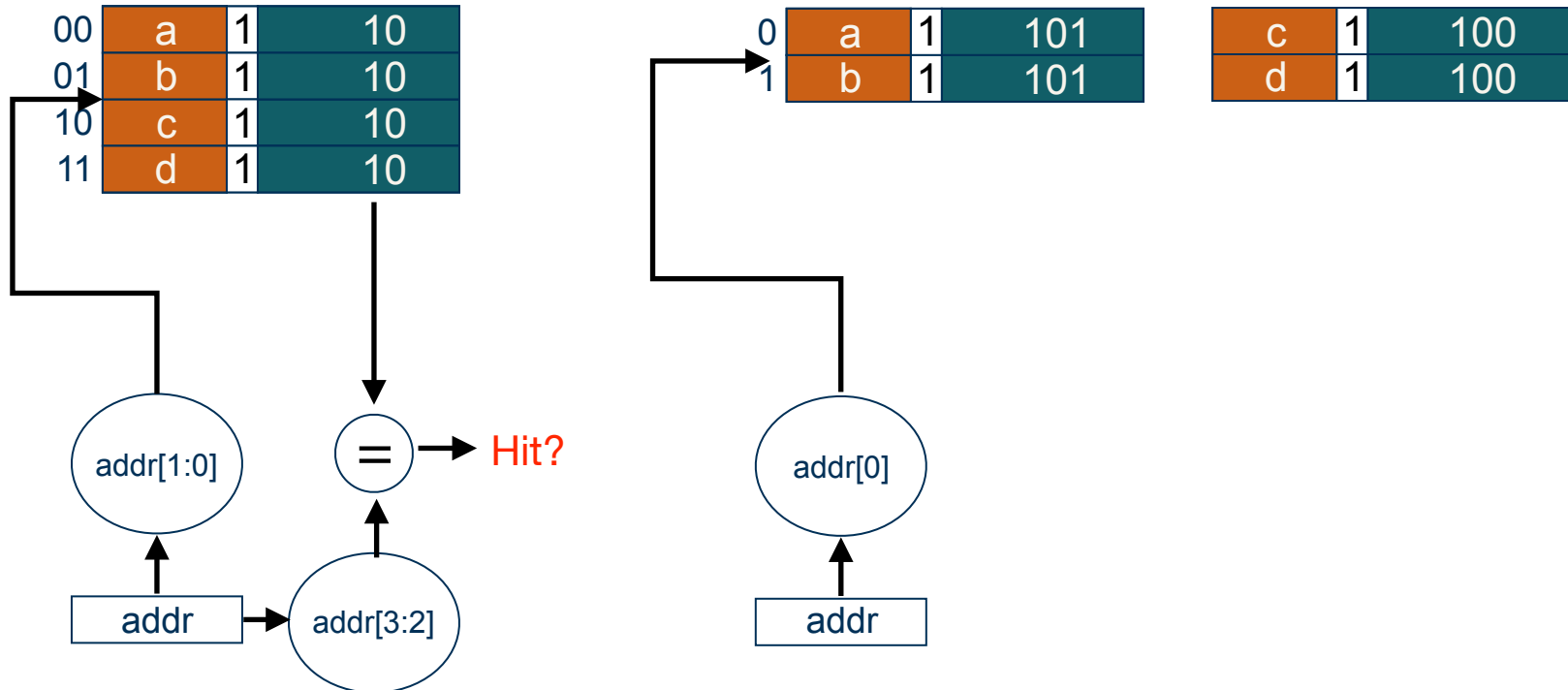


0	a	1	101
1	b	1	101

	c	1	100
	d	1	100

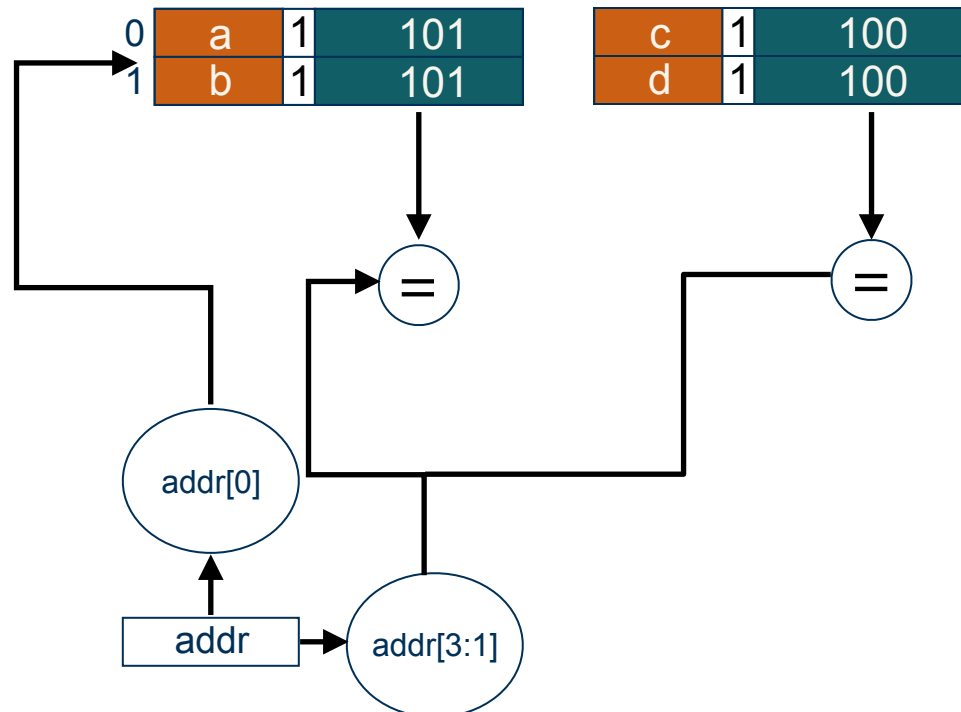
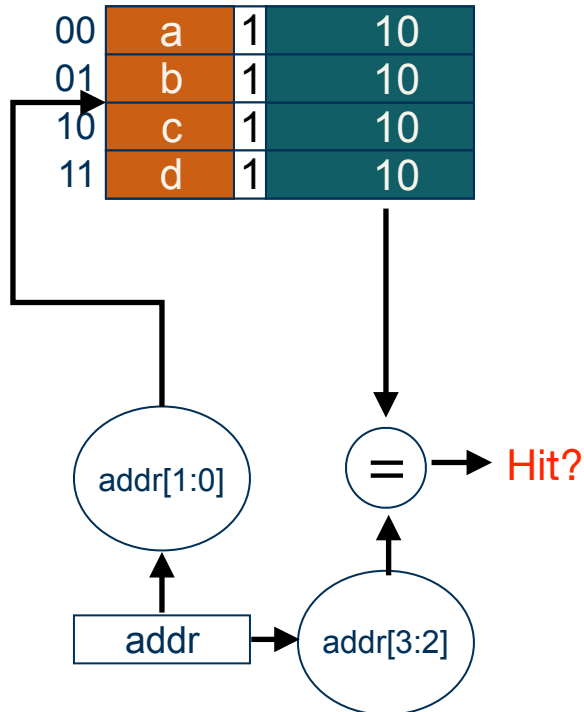
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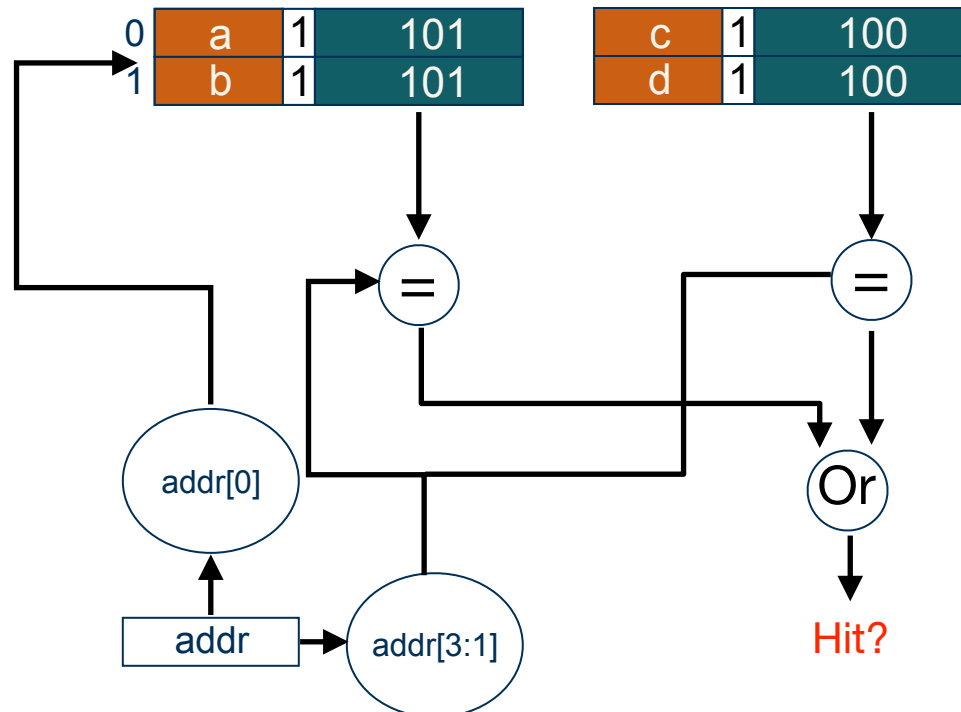
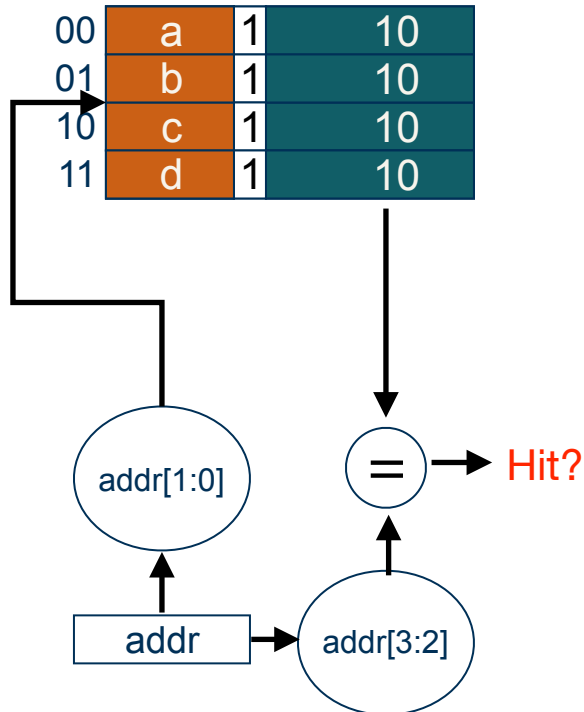
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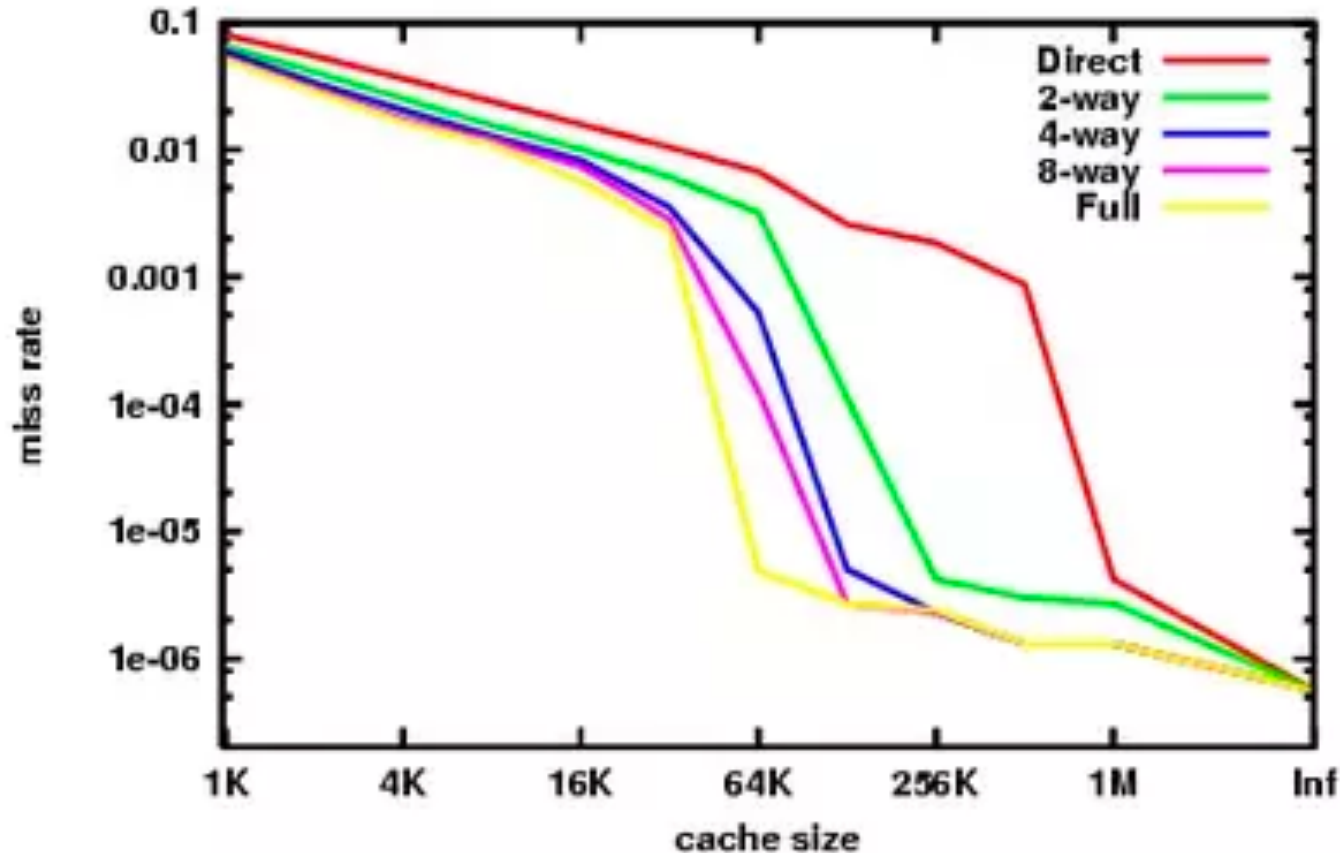


Associative verses Direct Mapped Trade-offs

- Direct-Mapped cache
 - Generally lower hit rate
 - Simpler, Faster
- Associative cache
 - Generally higher hit rate. Better utilization of cache resources
 - Slower and higher power consumption. Why?



Associative versus Direct Mapped Trade-offs



Miss rate versus cache size on the Integer portion of SPEC CPU2000

A Few Terminologies



Content Valid? Tag

- A cache line: content + valid bit + tag bits
 - Valid bit + tag bits are “overhead”
 - Content is what you really want to store
 - But we need valid and tag bits to correctly access the cache

0000	
0001	
0010	
0011	
0100	
0101	
0110	
0111	
1000	0xEF
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Cache Organization

- Finding a name in a roster
- If the roster is completely unorganized
 - Need to compare the name with all the names in the roster
 - Same as a fully-associative cache
- If the roster is ordered by last name, and within the same last name different first names are unordered
 - First find the last name group
 - Then compare the first name with all the first names in the same group
 - Same as a set-associative cache

Cache Access Summary (So far...)

- Assuming b bits in a memory address
- The b bits are split into two halves:
 - Lower s bits used as index to find a set. Total sets $S = 2^s$
 - The higher $(b - s)$ bits are used for the tag
- Associativity n (i.e., the number of ways in a cache set) is **independent** of the the split between index and tag

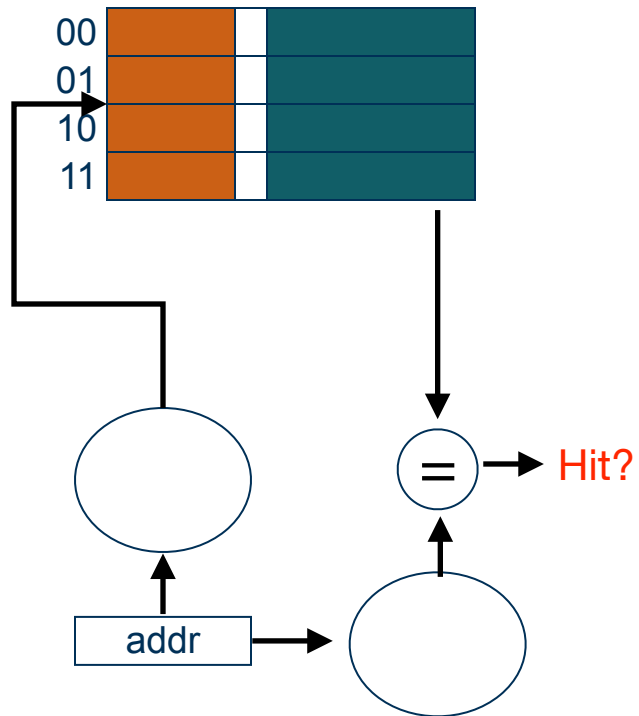


Locality again

- So far: temporal locality
- What about spatial?
- Idea: Each cache location (cache line) store multiple bytes

Cache-Line Size of 2

Cache

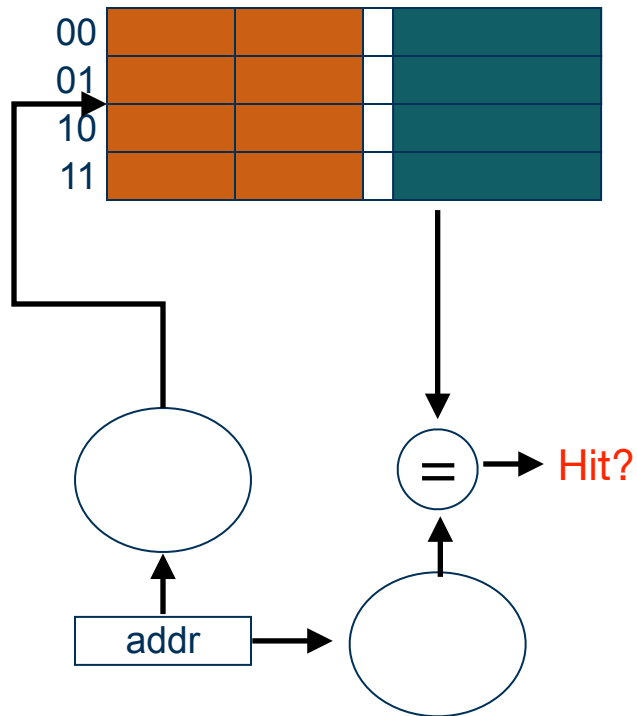


Memory

0000	
0001	
0010	
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Cache-Line Size of 2

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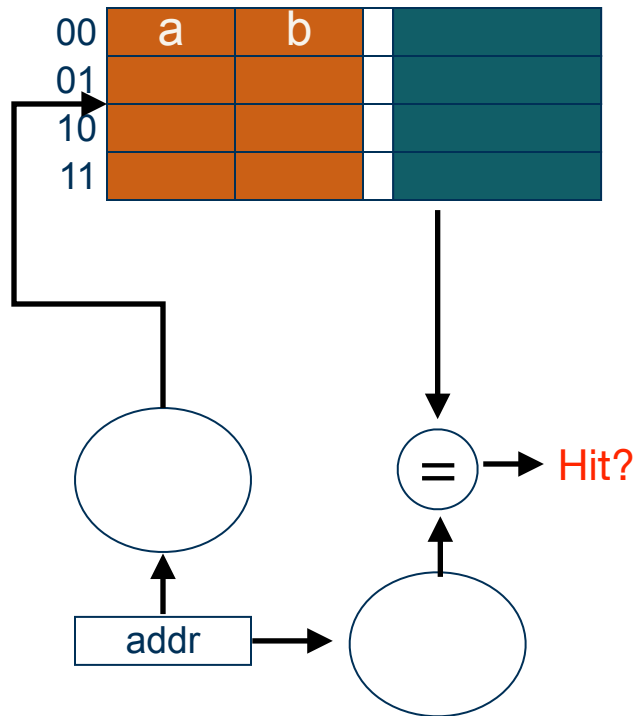


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Cache-Line Size of 2

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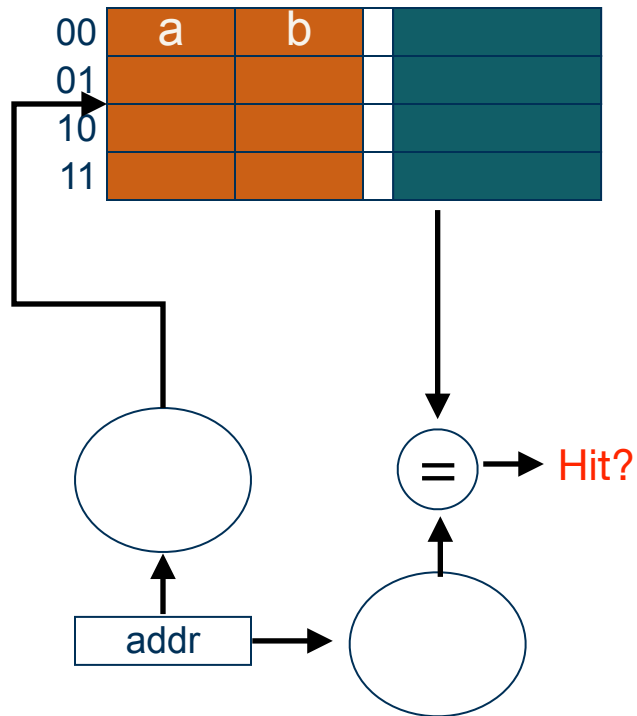
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- Read 1000

Cache-Line Size of 2

Cache



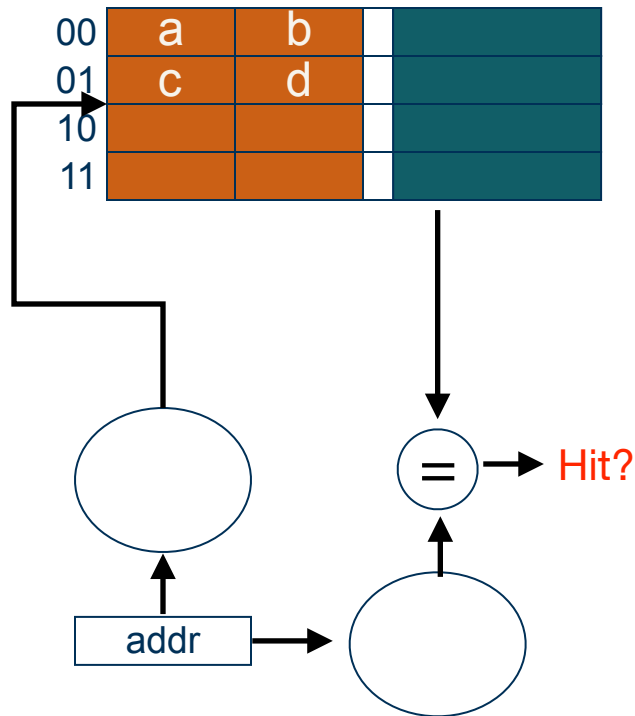
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- Read 1000
- Read 1001 (**Hit!**)

Cache-Line Size of 2

Cache



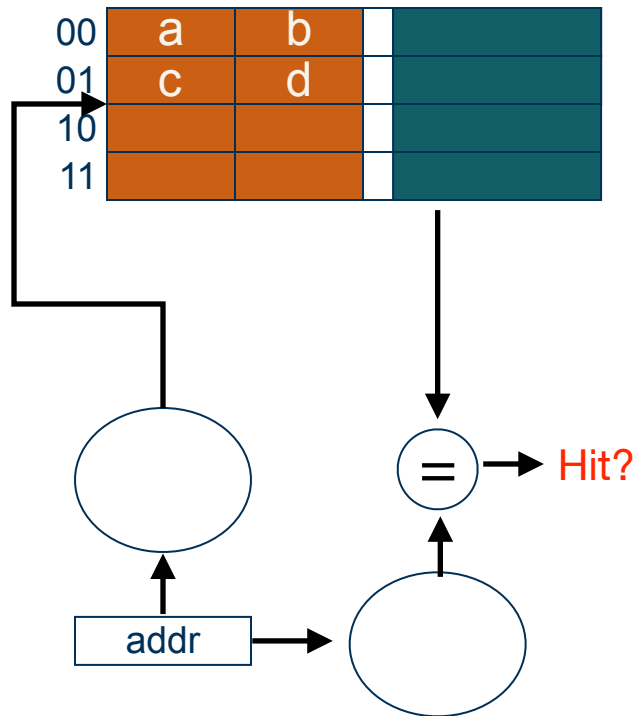
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- Read 1000
- Read 1001 (Hit!)
- Read 1010

Cache-Line Size of 2

Cache



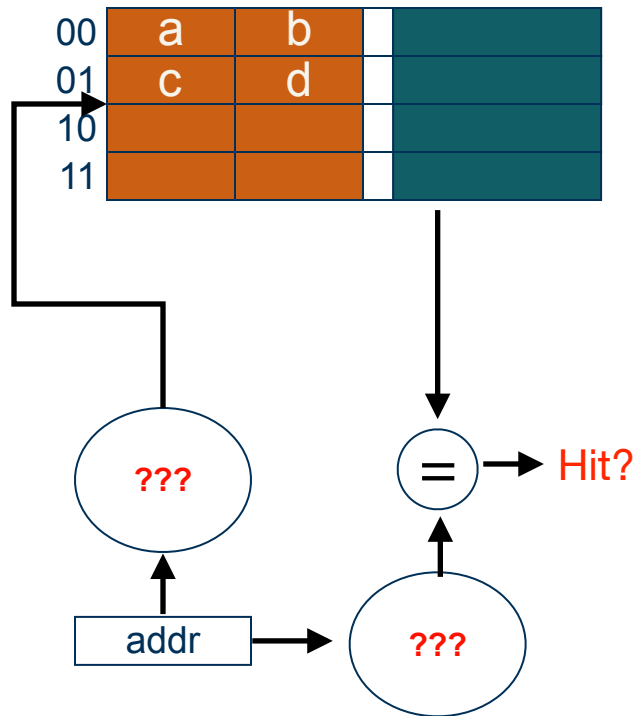
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- Read 1000
- Read 1001 (Hit!)
- Read 1010
- Read 1011 (Hit!)

Cache-Line Size of 2

Cache



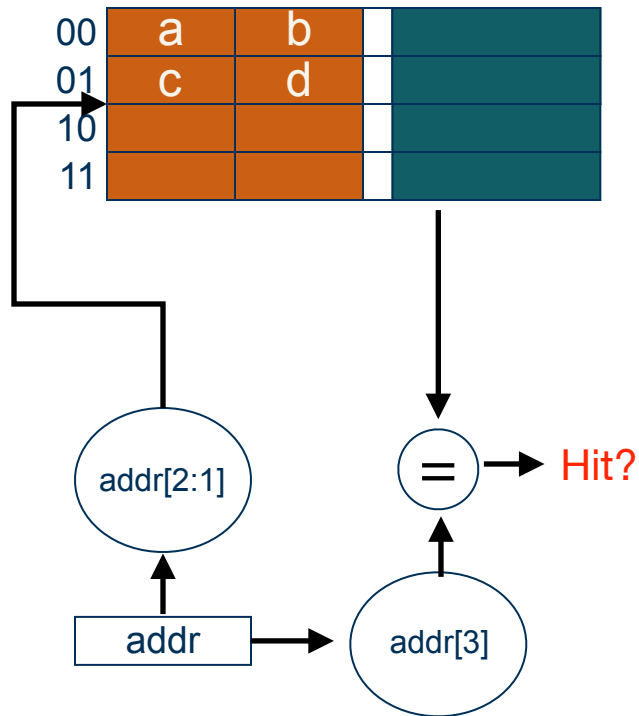
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0111	
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1101	
1110	
1111	

- Read 1000
- Read 1001 (**Hit!**)
- Read 1010
- Read 1011 (**Hit!**)
- **How to access the cache now?**

Cache-Line Size of 2

Cache



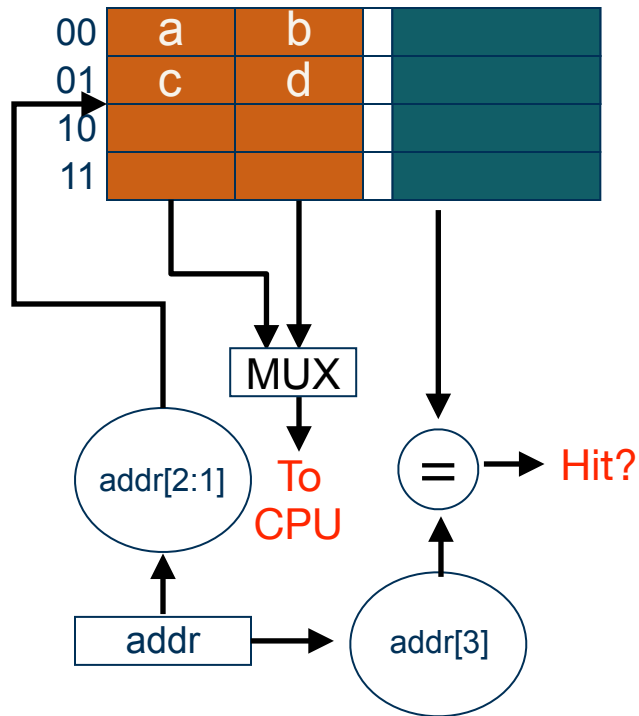
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- Read 1000
- Read 1001 (Hit!)
- Read 1010
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Cache-Line Size of 2

Cache



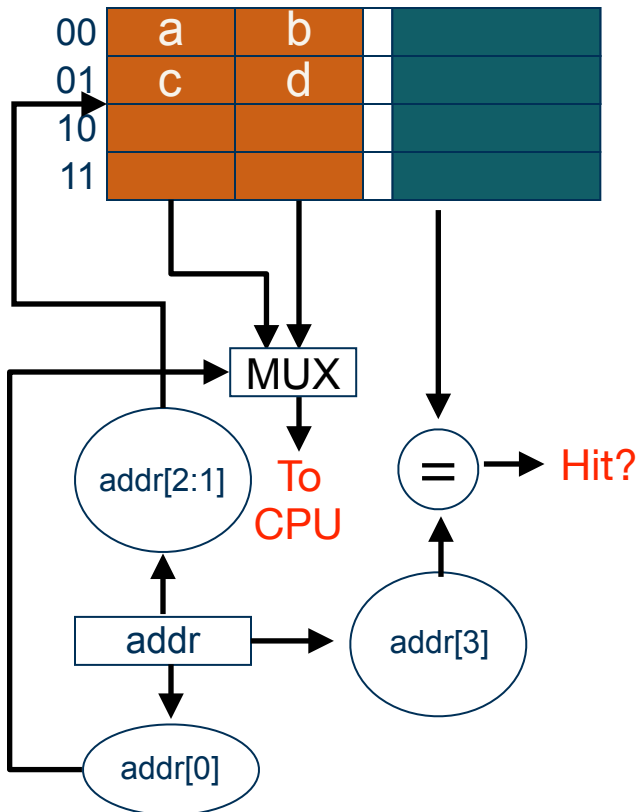
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0001	
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1111	

- Read 1000
- Read 1001 (Hit!)
- Read 1010
- Read 1011 (Hit!)

Cache-Line Size of 2

Cache



Memory

0000	
0001	
0010	
0011	
0100	
0101	
0110	
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- Read 1000
- Read 1001 (**Hit!**)
- Read 1010
- Read 1011 (**Hit!**)

Cache Access Summary

- Assuming b bits in a memory address
- The b bits are split into three fields:
 - Lower l bits are used for byte offset within a cache line. Cache line size $L = 2^l$
 - Next s bits used as index to find a set. Total sets $S = 2^s$
 - The higher $(b - l - s)$ bits are used for the tag
- Associativity n is independent of the the split between index and tag



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- Read hit: Nothing special. Enjoy the hit!

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Potentially saves bandwidth between cache and memory + saves energy
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- Write-through
 - + Simpler
 - + Memory is up to date
 - - More bandwidth intensive; no coalescing of writes
 - - Requires transfer of the whole cache line (although only one byte might have been modified)

Handling Writes (Miss)

- Do we allocate a cache line on a write miss?
 - **Write-allocate**: Allocate on write miss
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- Non-allocate
 - + Conserves cache space if locality of writes is low (potentially better cache hit rate)

Instruction vs. Data Caches

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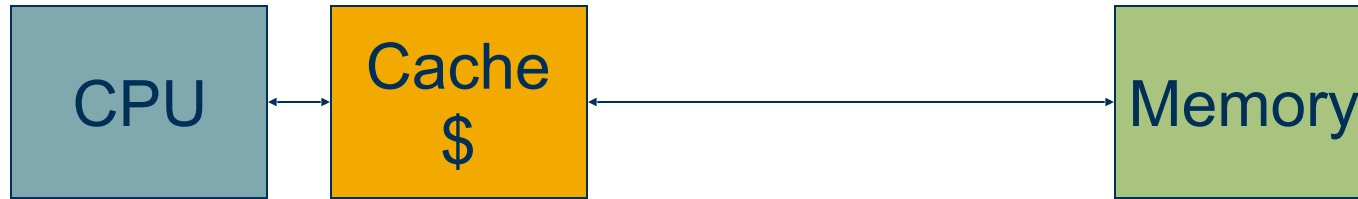
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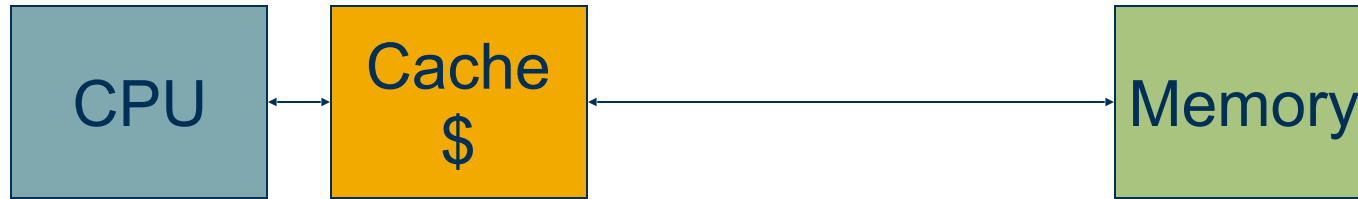
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Where do we place the unified cache for fast access?
- **First level caches are almost always split**
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- **Second and higher levels are almost always unified**

General Rule: Bigger == Slower



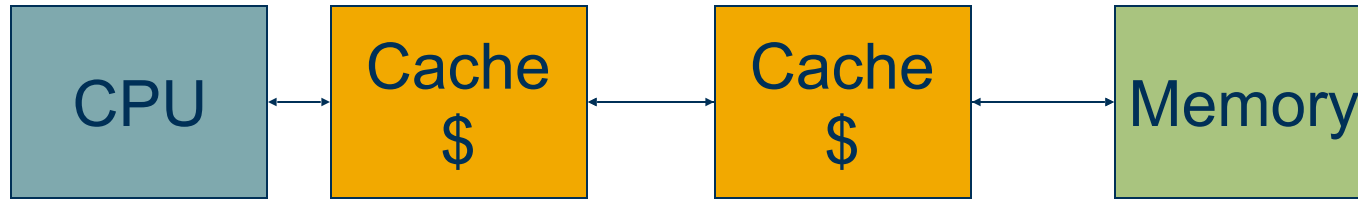
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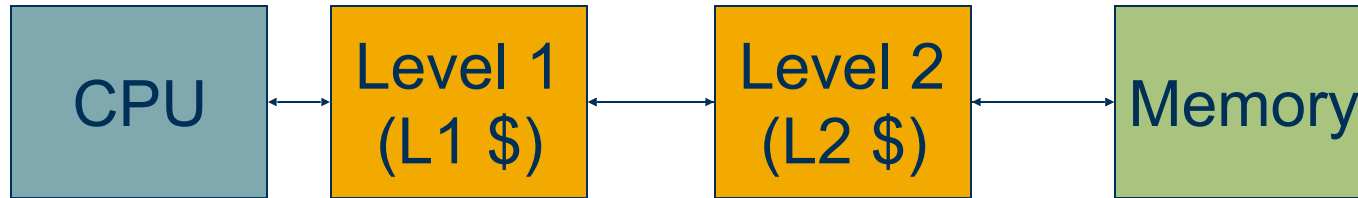
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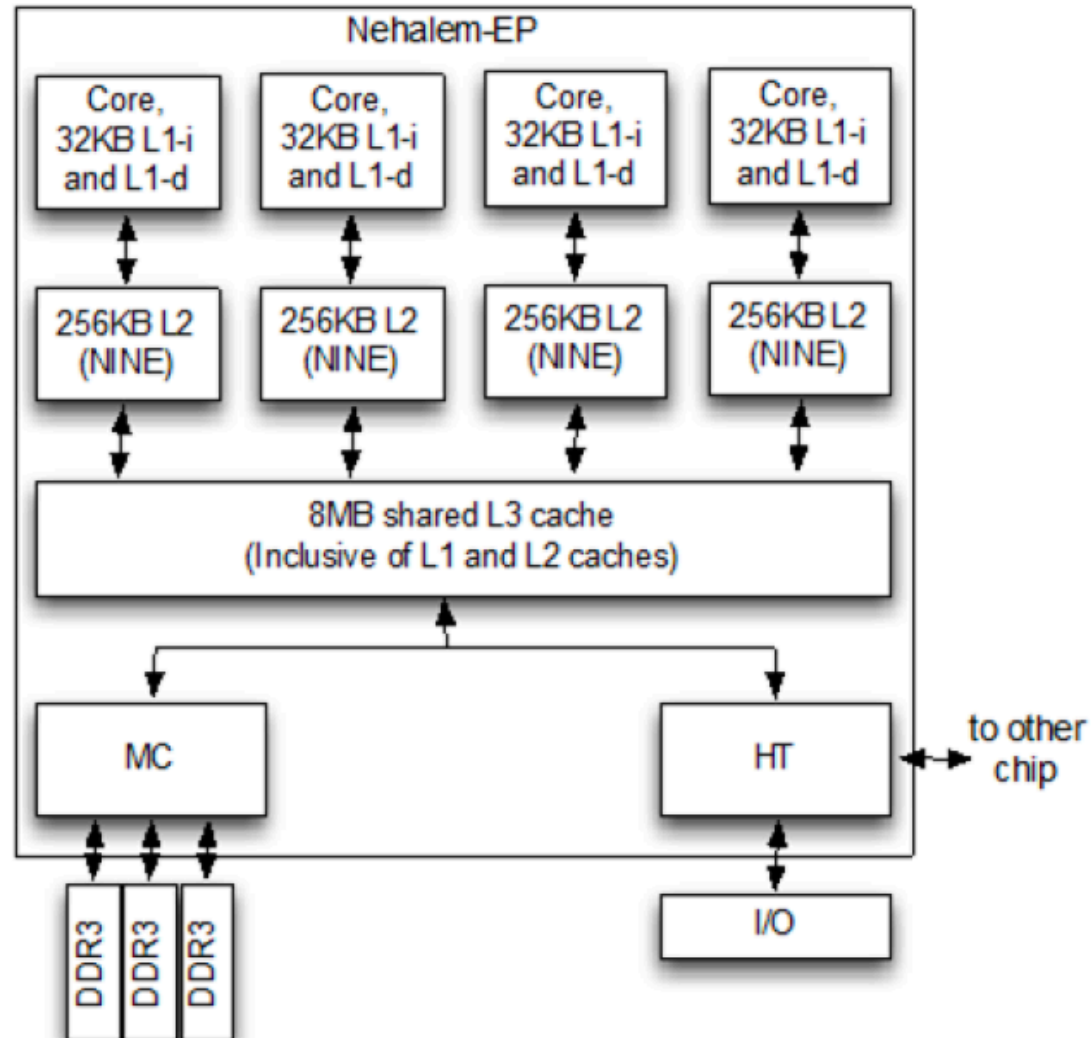
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A Real Intel Processor



Eviction/Replacement Policy

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 - Ideally: Replace the cache line that's least likely going to be used again
 - Approximation: Least recently used (LRU)

Implementing LRU

- Idea: Evict the least recently accessed block
- Challenge: Need to keep track of access ordering of blocks
- Question: 2-way set associative cache:
 - What do you need to implement LRU perfectly? One bit?

Cache Lines

0

1

LRU index (1-bit)



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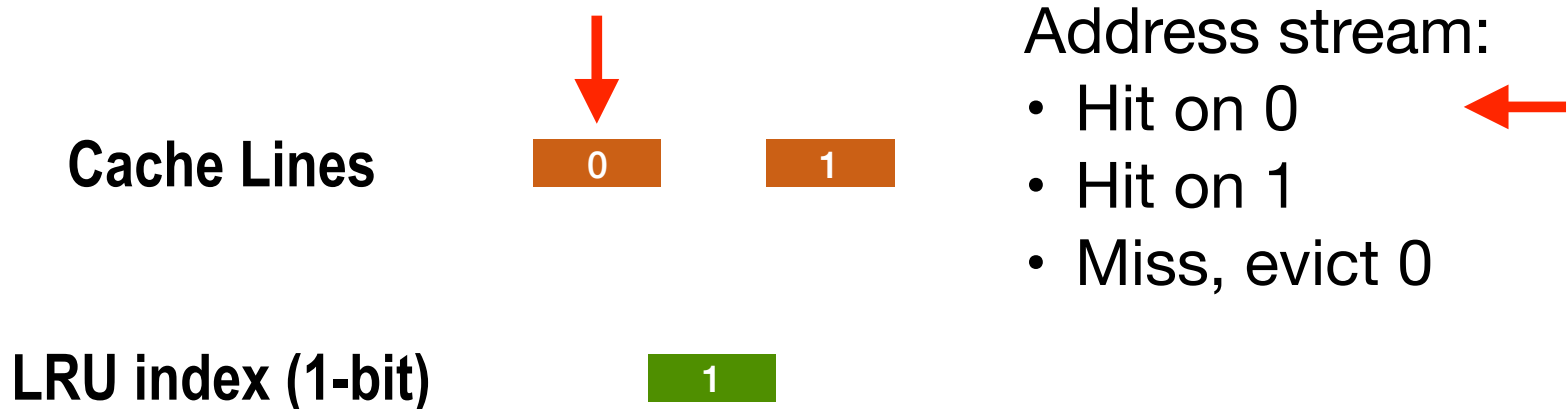
LRU index (1-bit)

Address stream:

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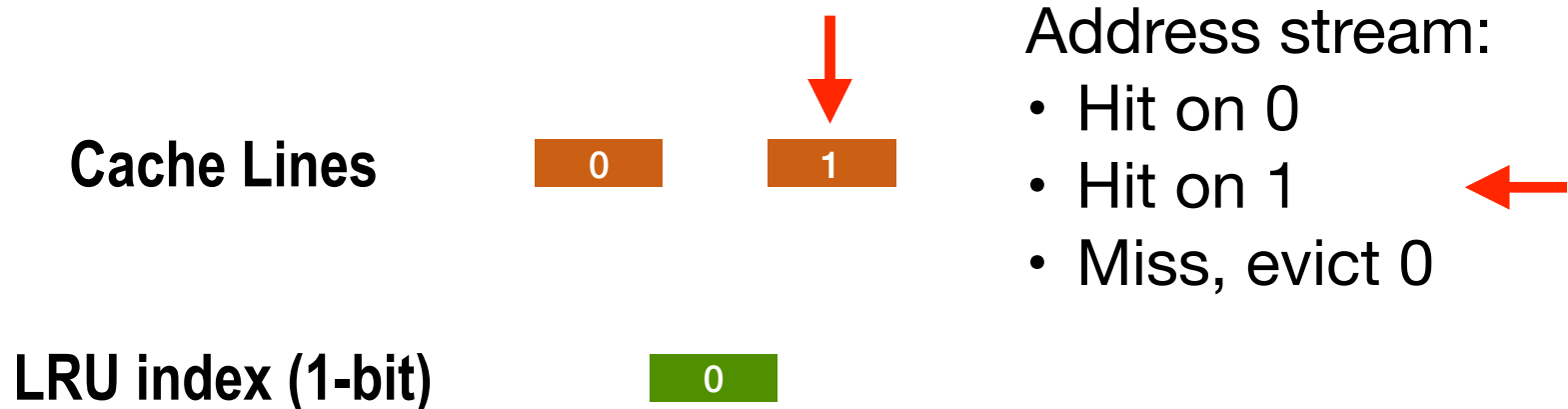
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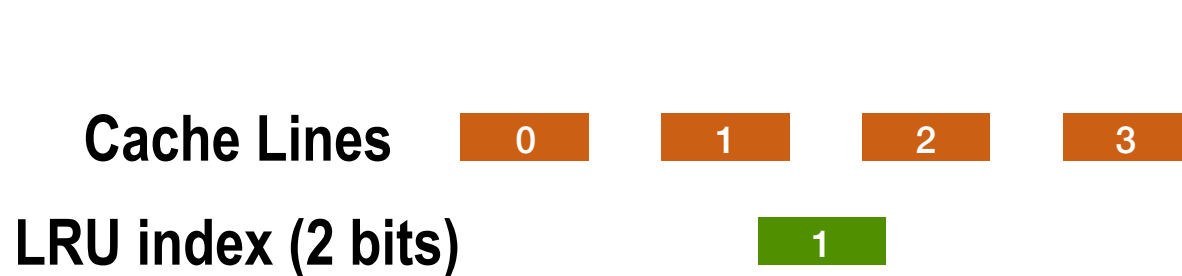
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Implementing LRU

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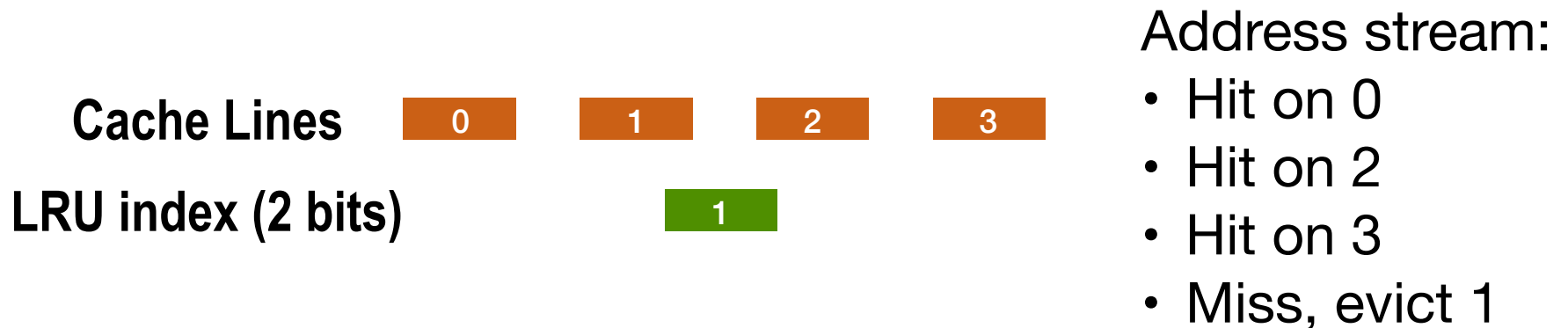


Address stream:

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- Hit on 2
- Hit on 3
- Miss, evict 1

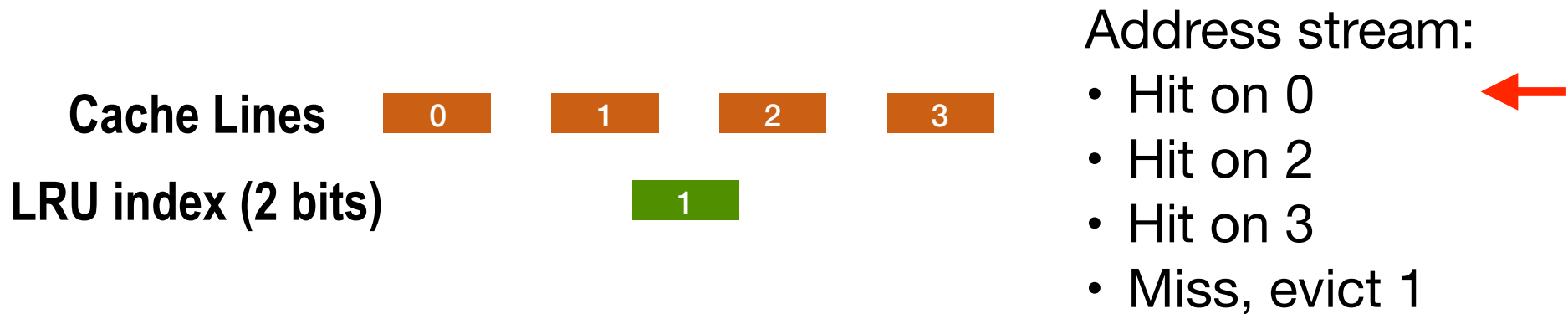
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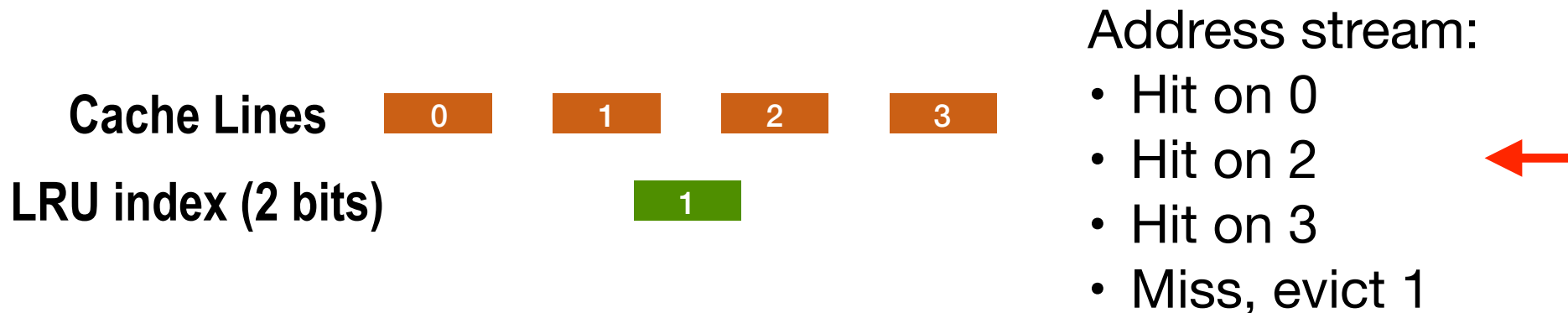
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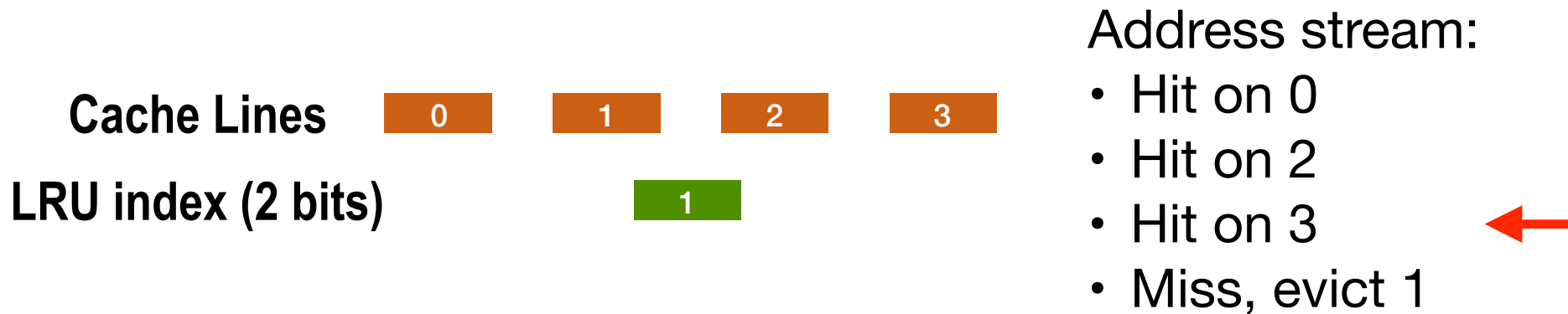
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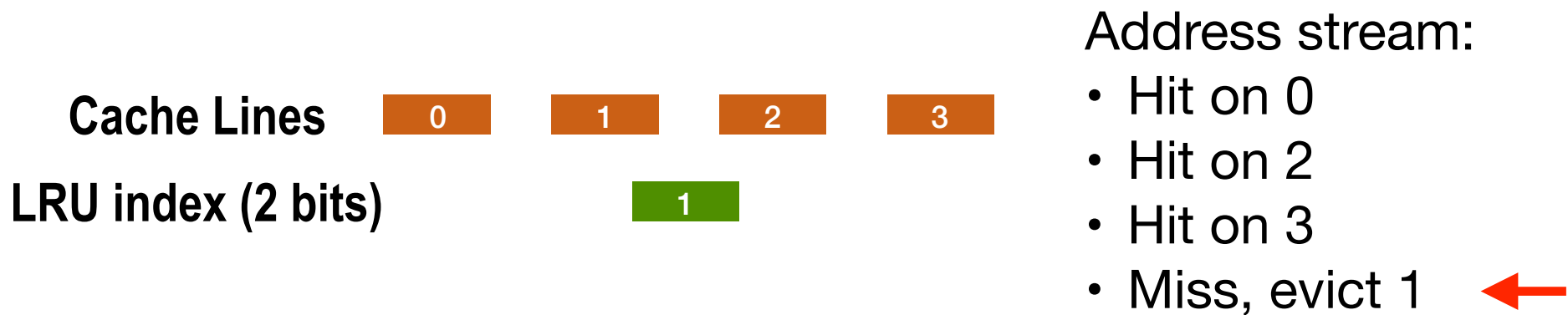
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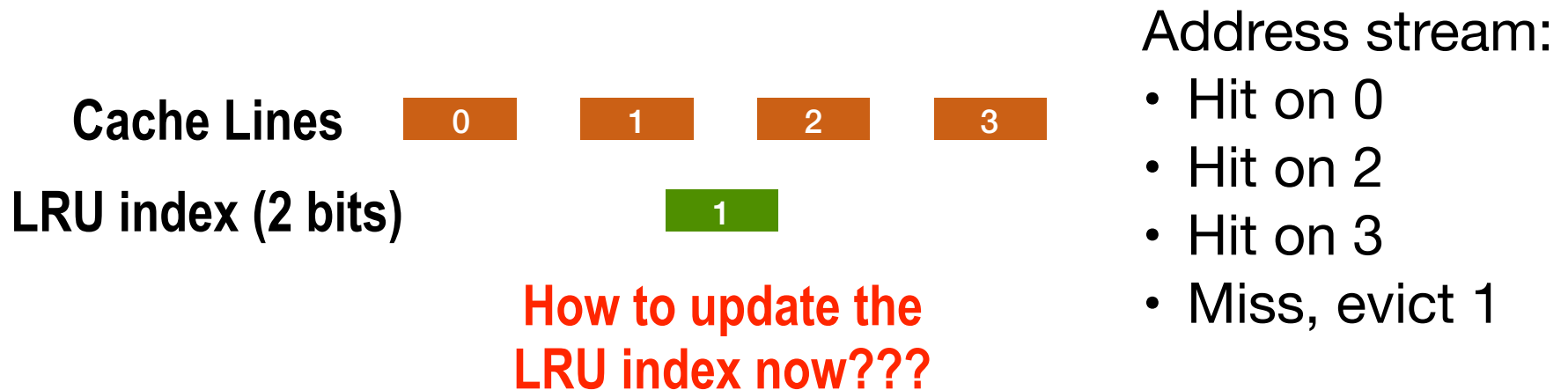
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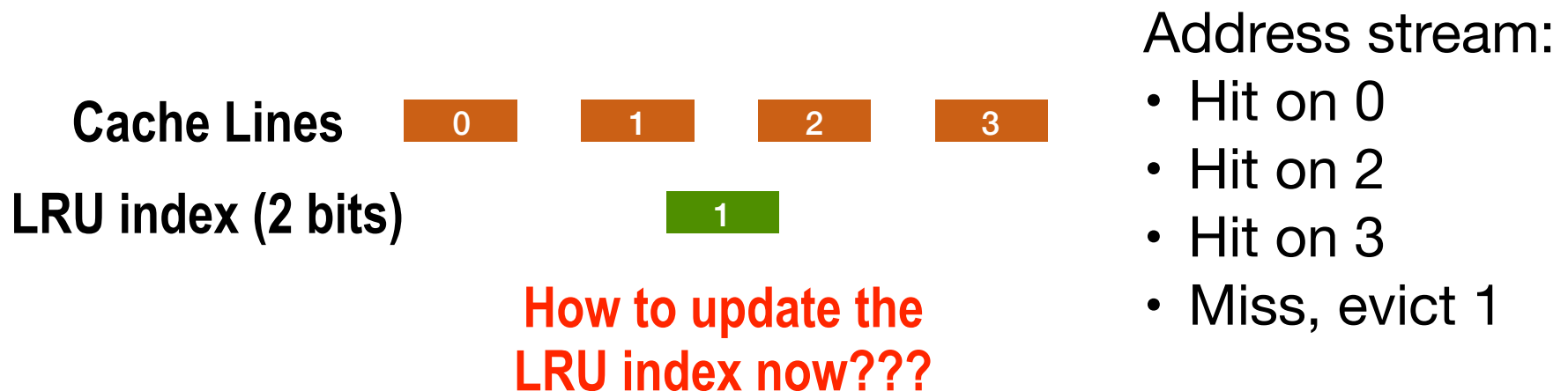
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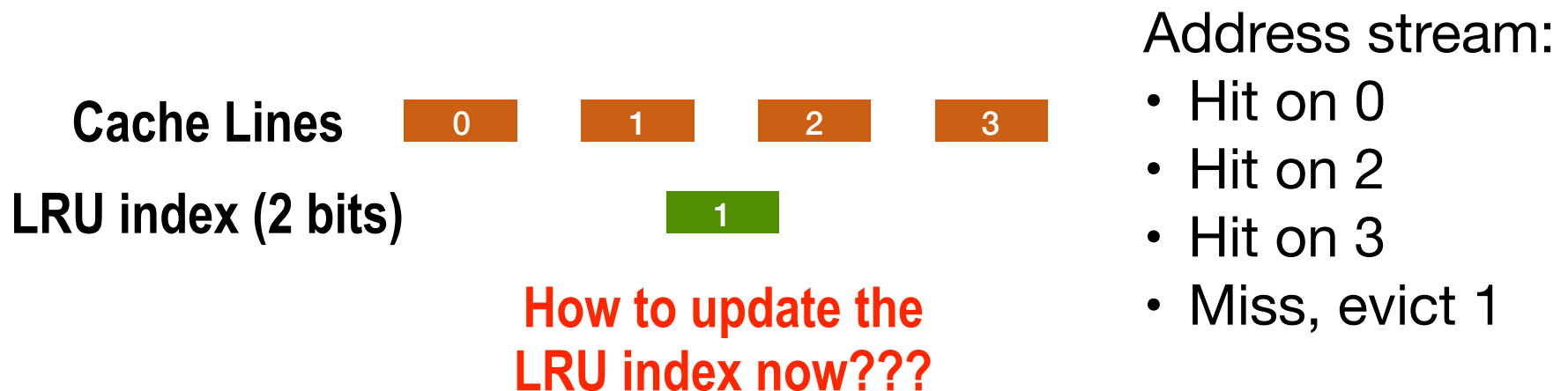
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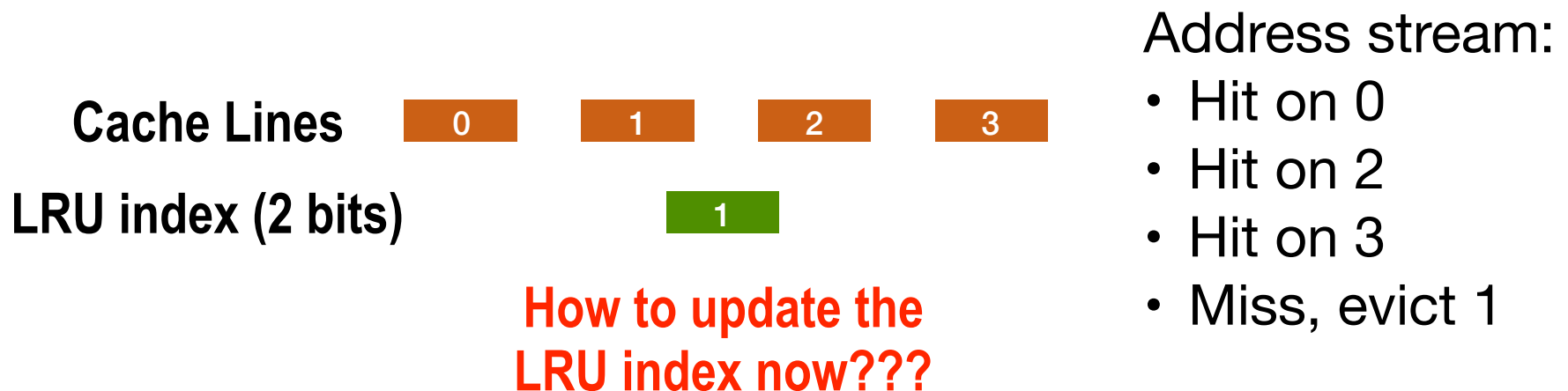
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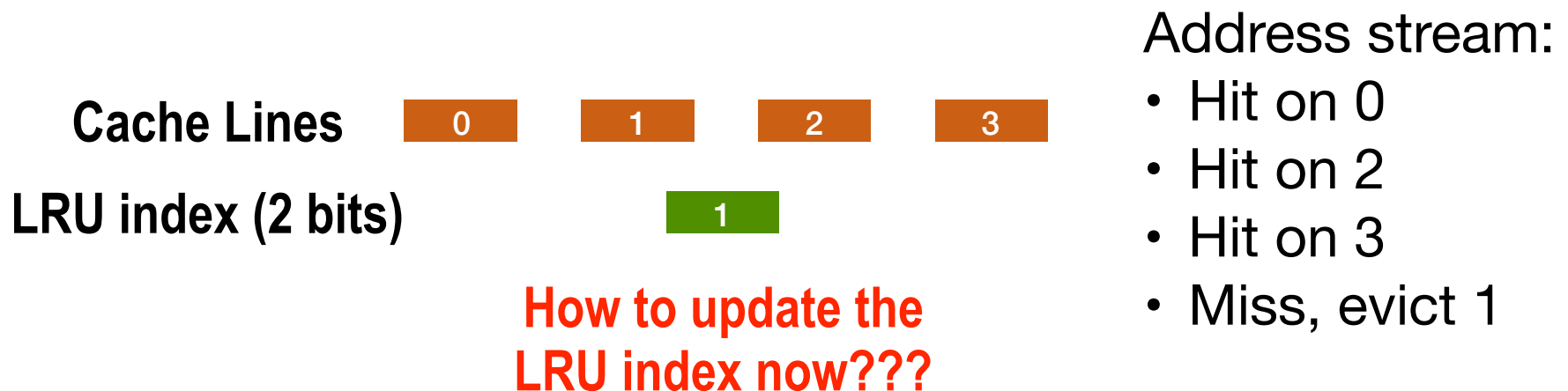
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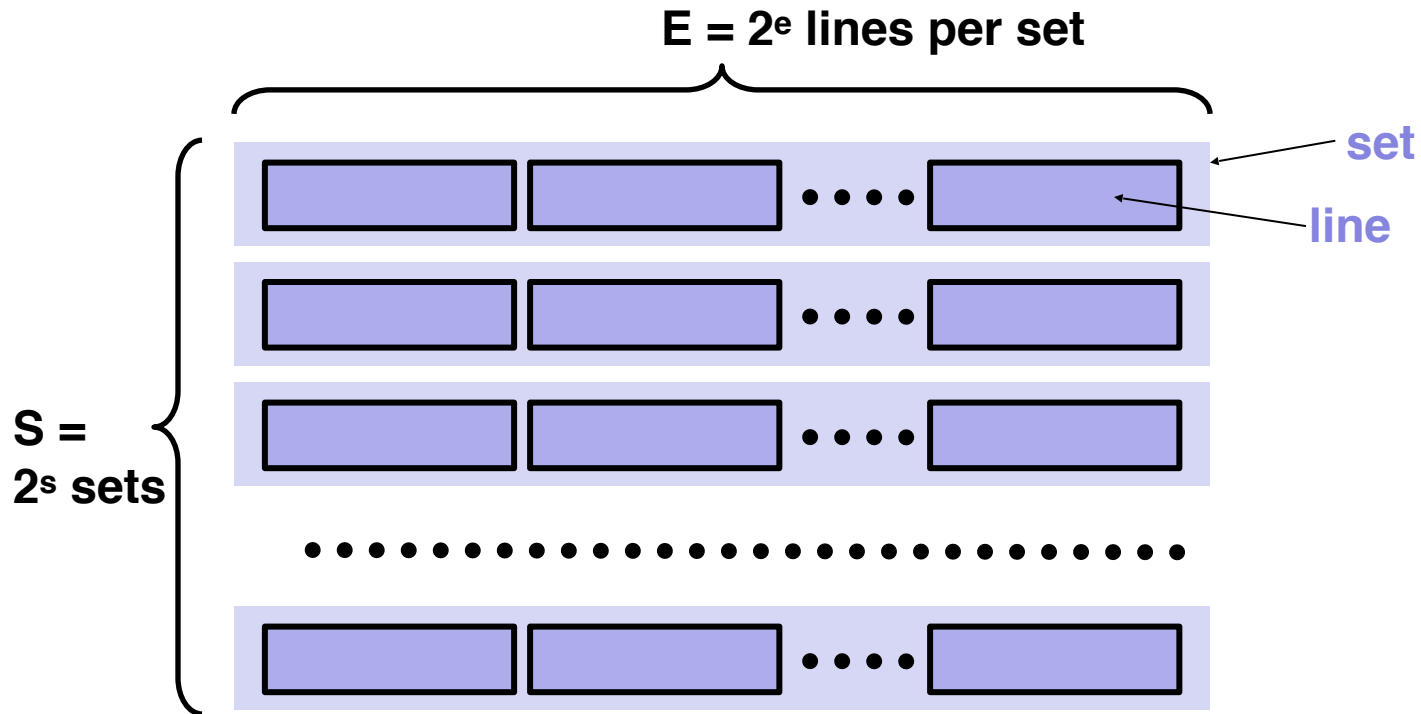


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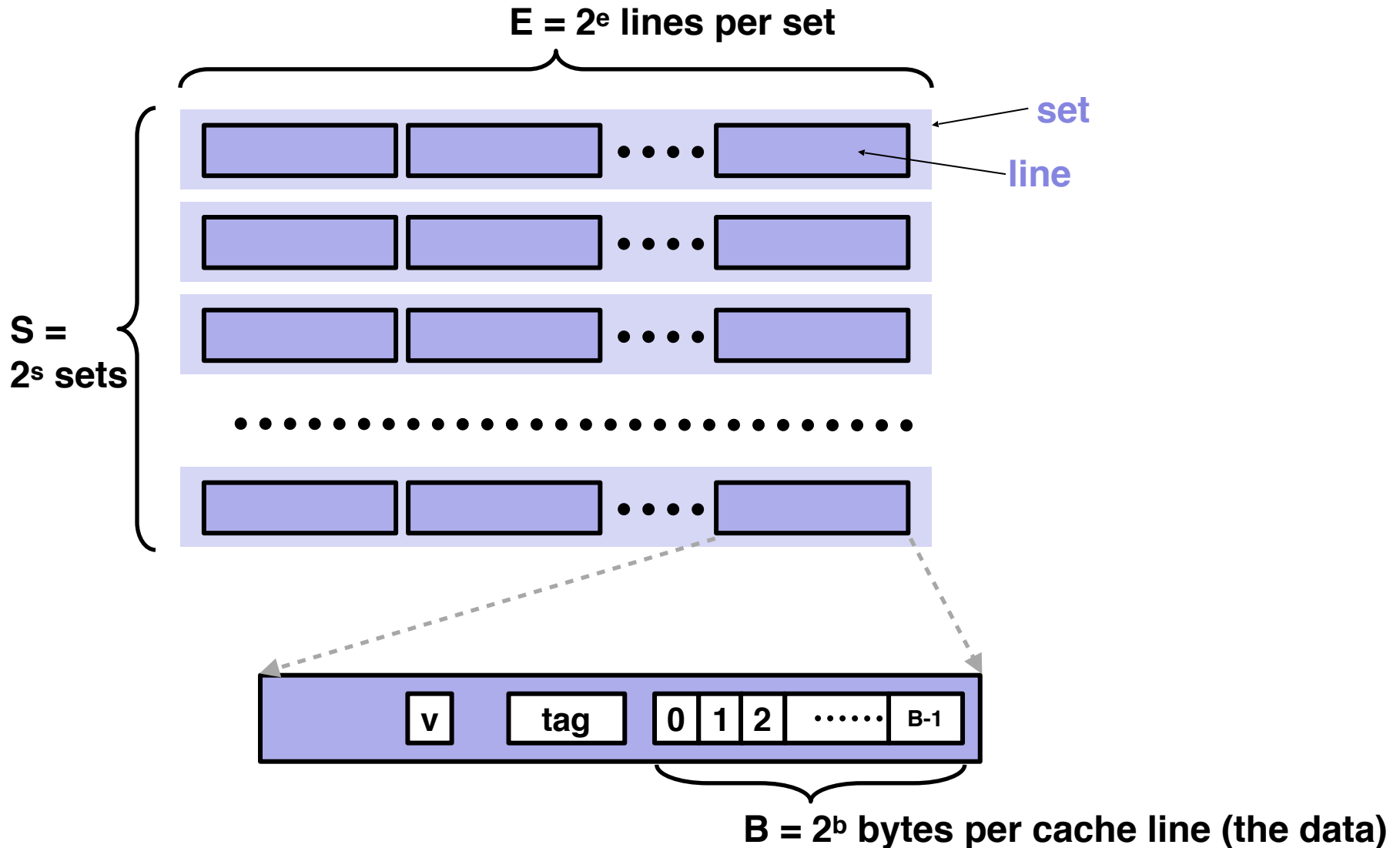
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 - “Pseudo-LRU” is usually used in real processors.



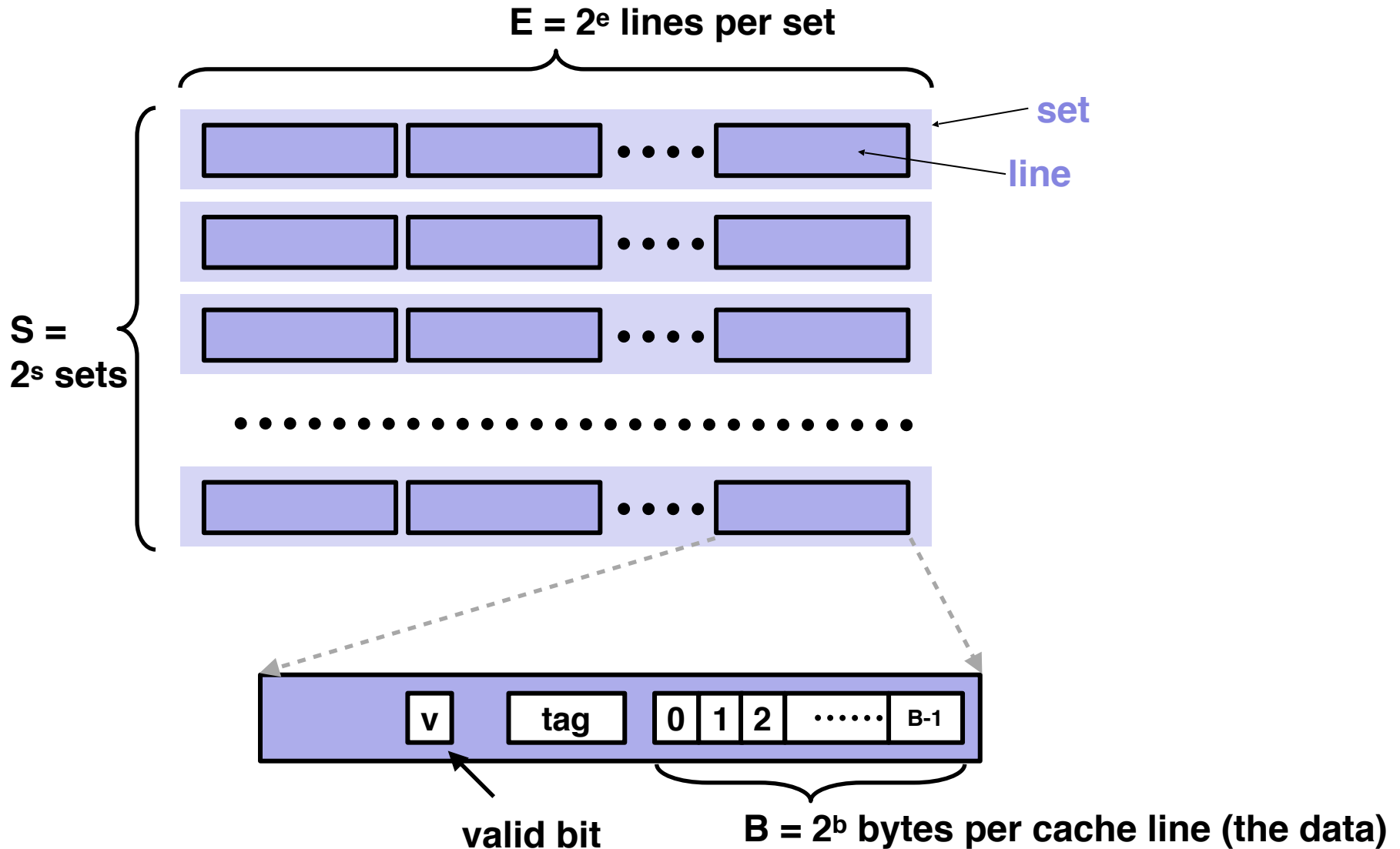
General Cache Organization (S, E, B)



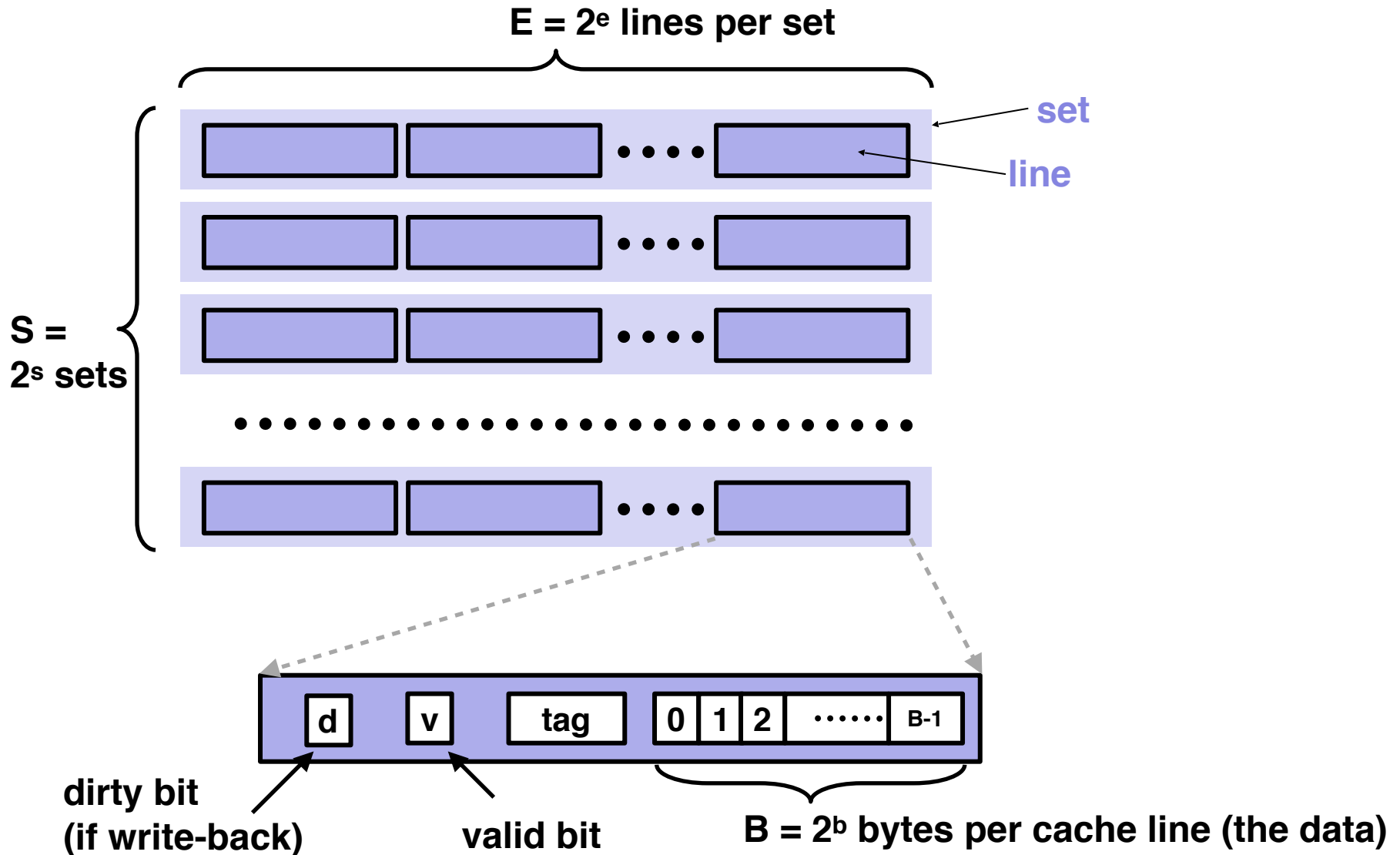
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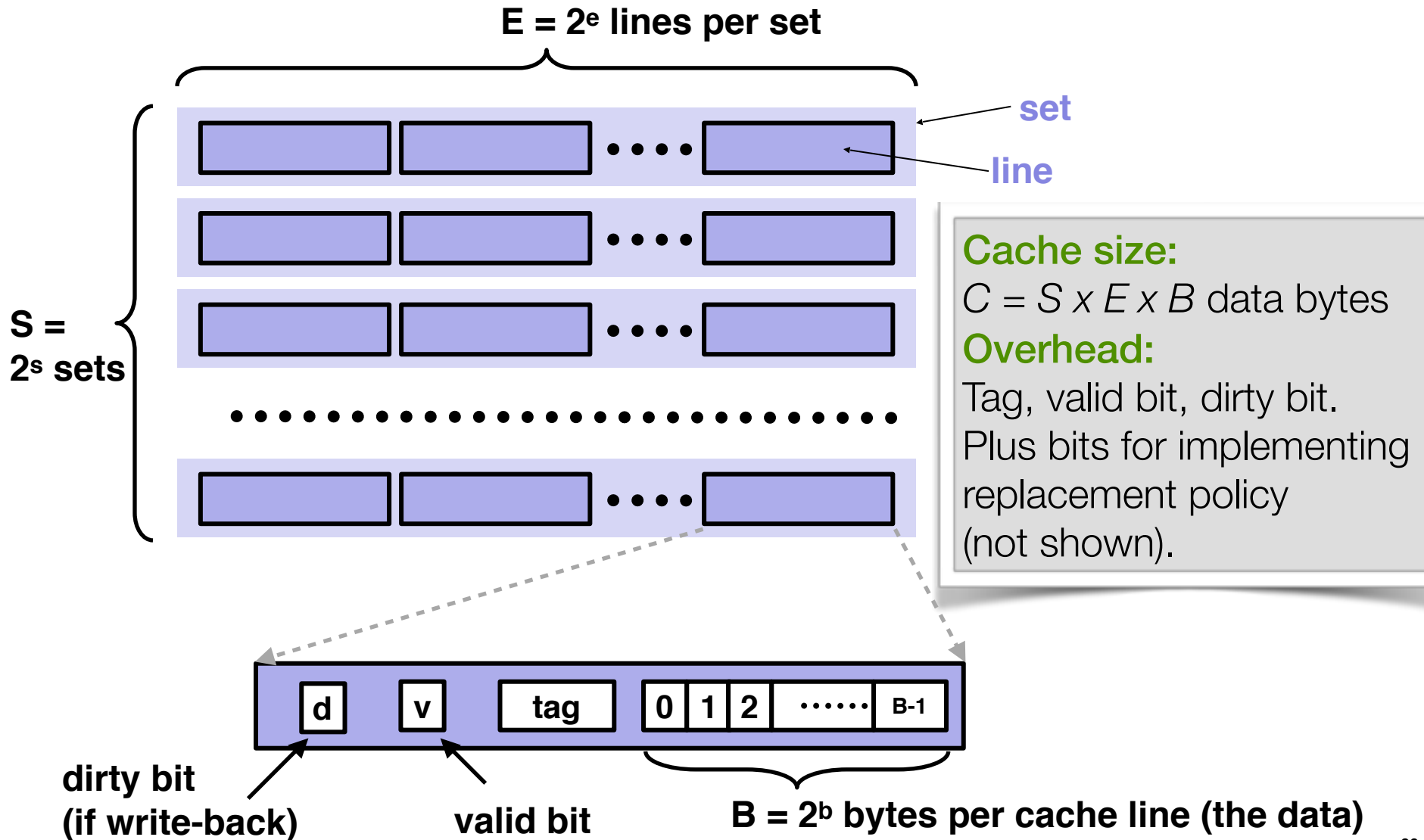
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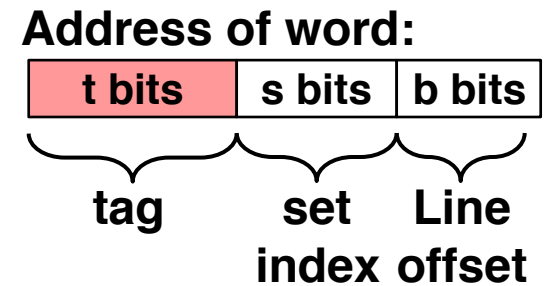
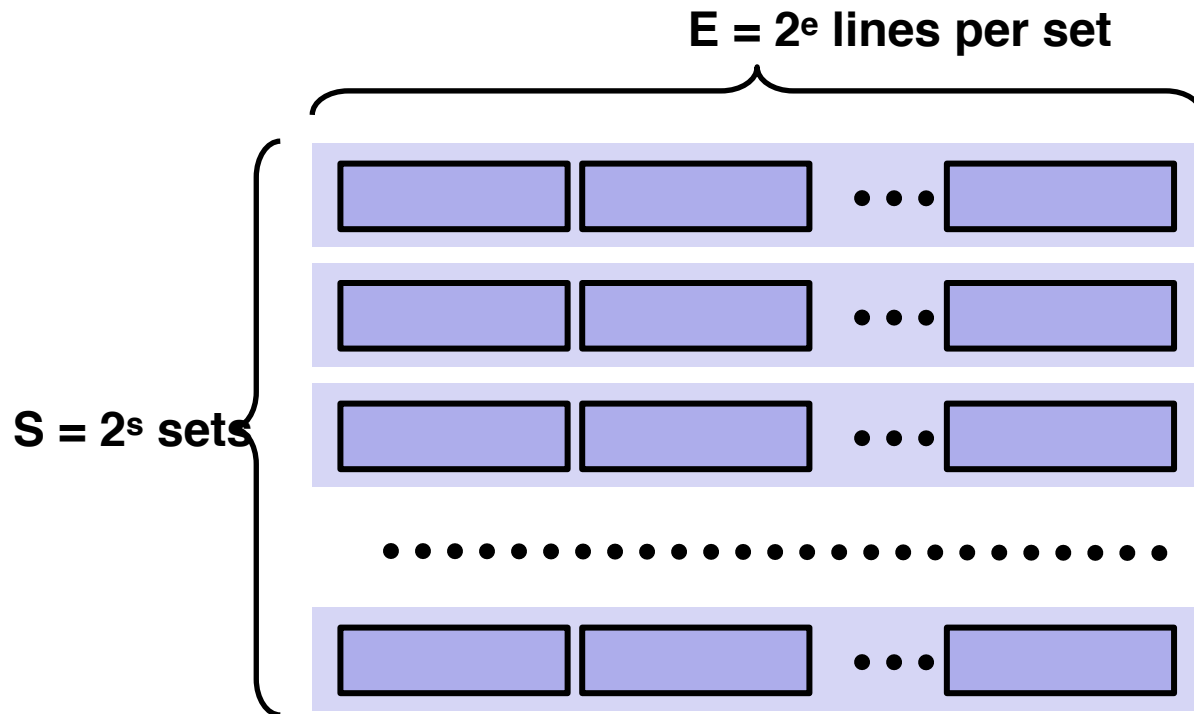
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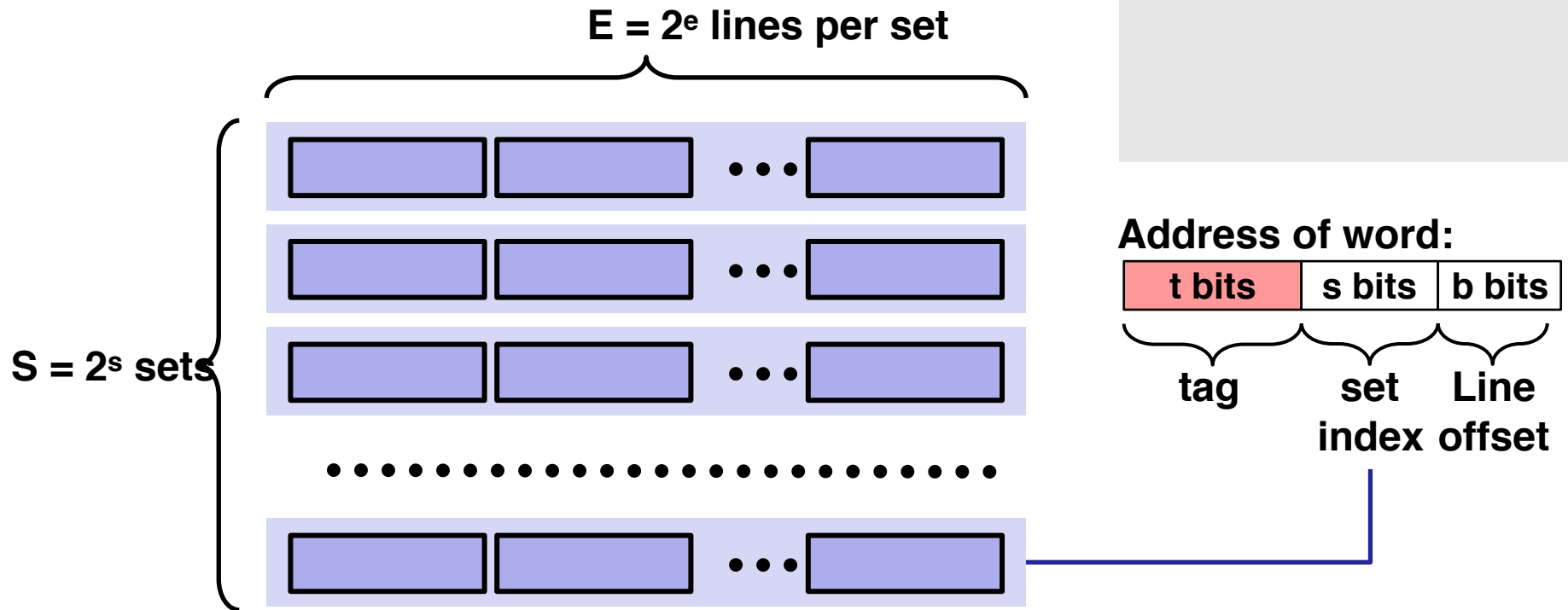


Cache Access



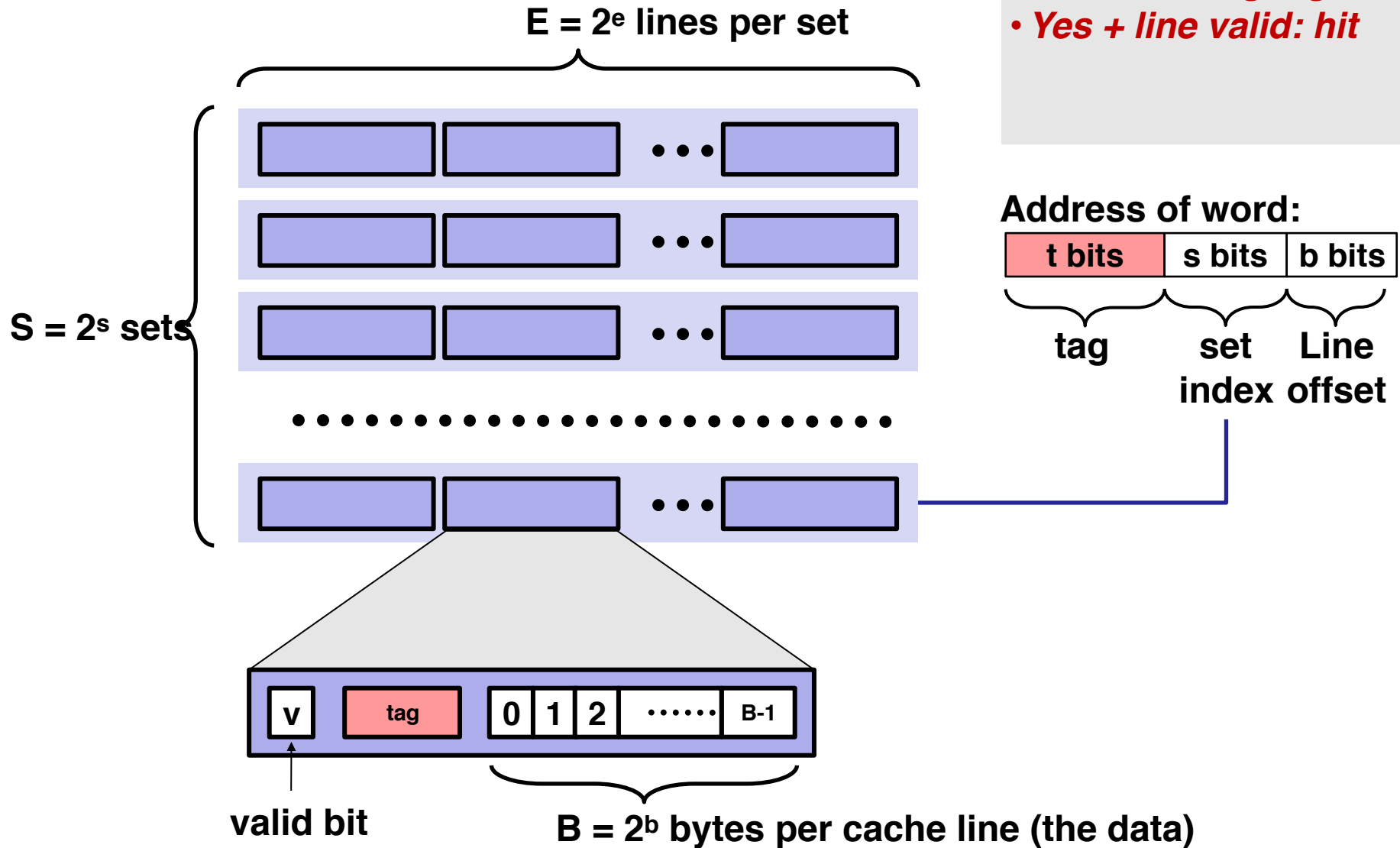
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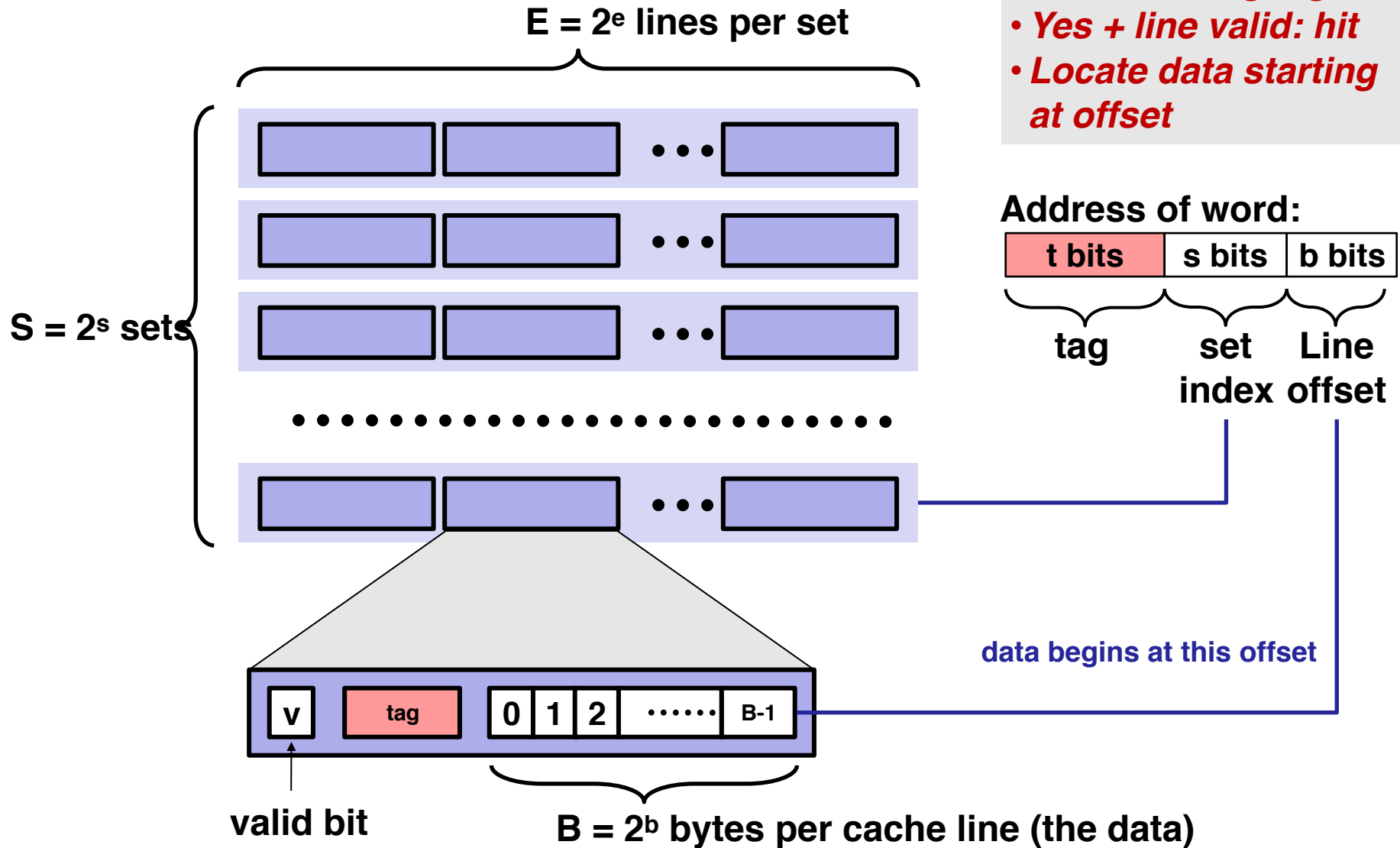
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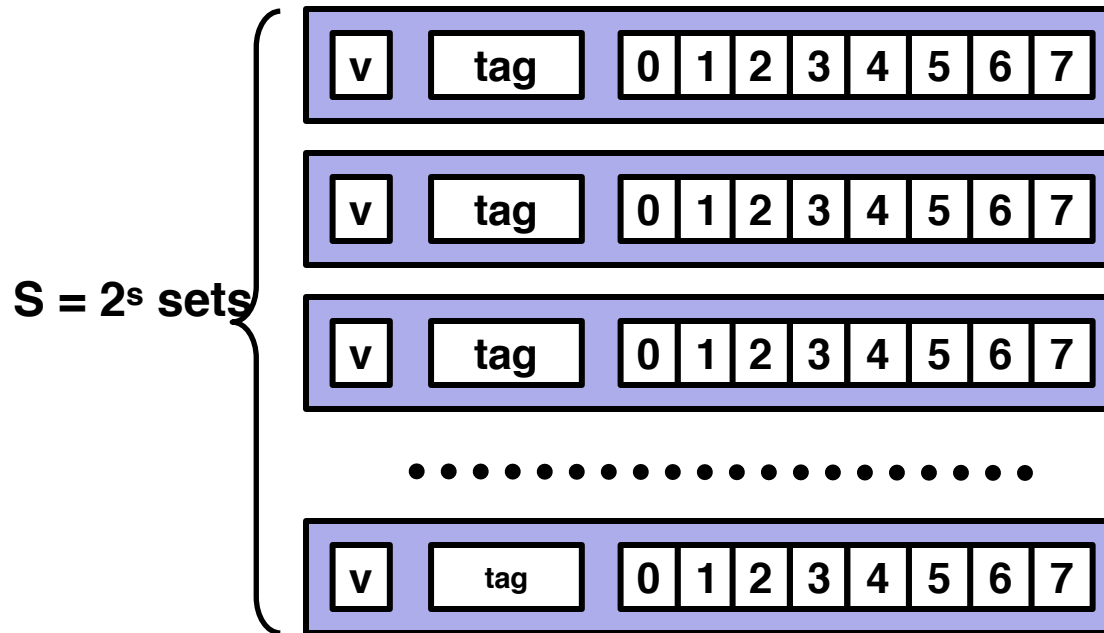
- *Locate set*
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- *Locate data starting at offset*



Example: Direct Mapped Cache

Direct mapped: One line per set

Assume: cache line size 8 bytes



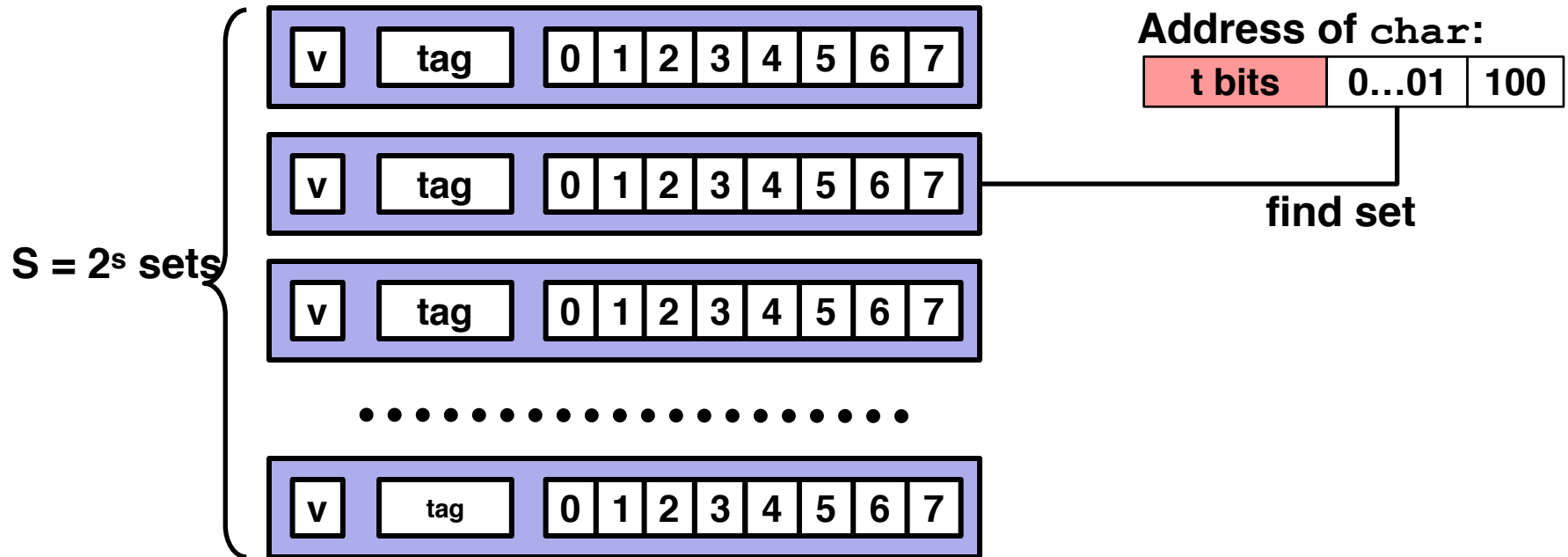
Address of char:

t bits	0...01	100
--------	--------	-----

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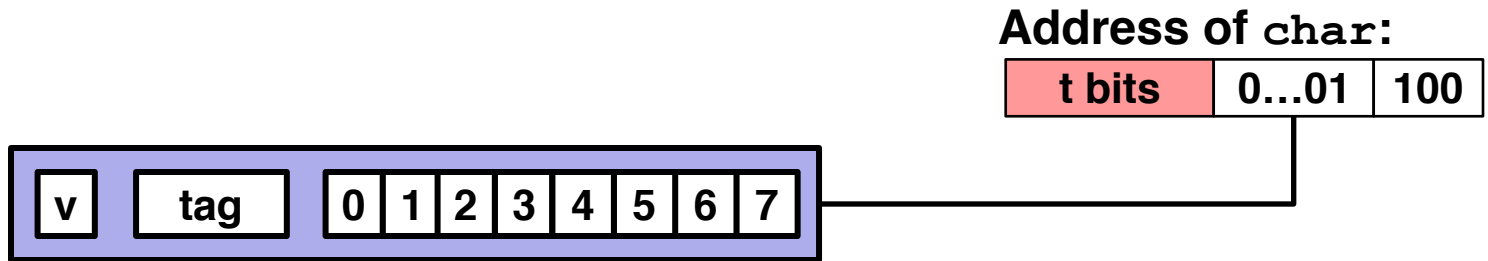
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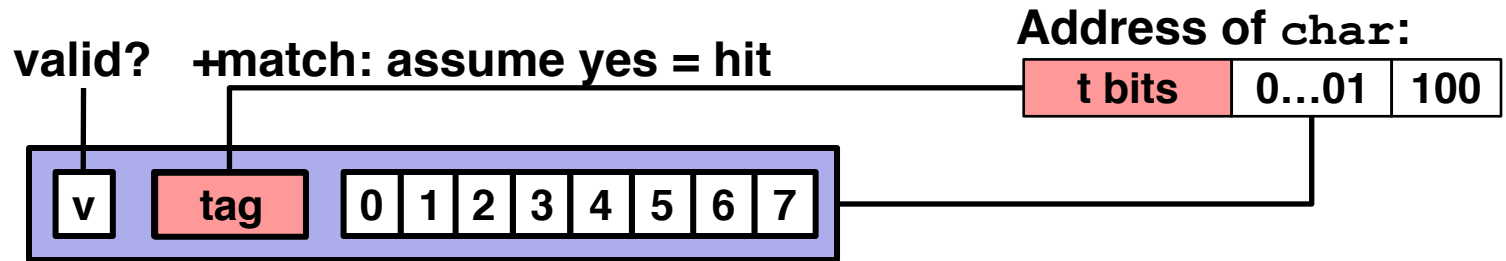
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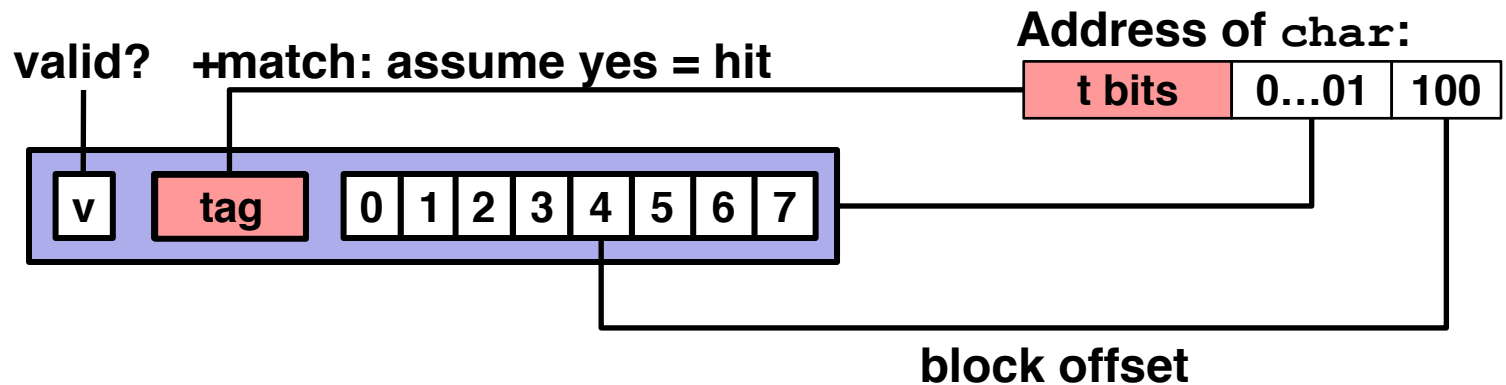
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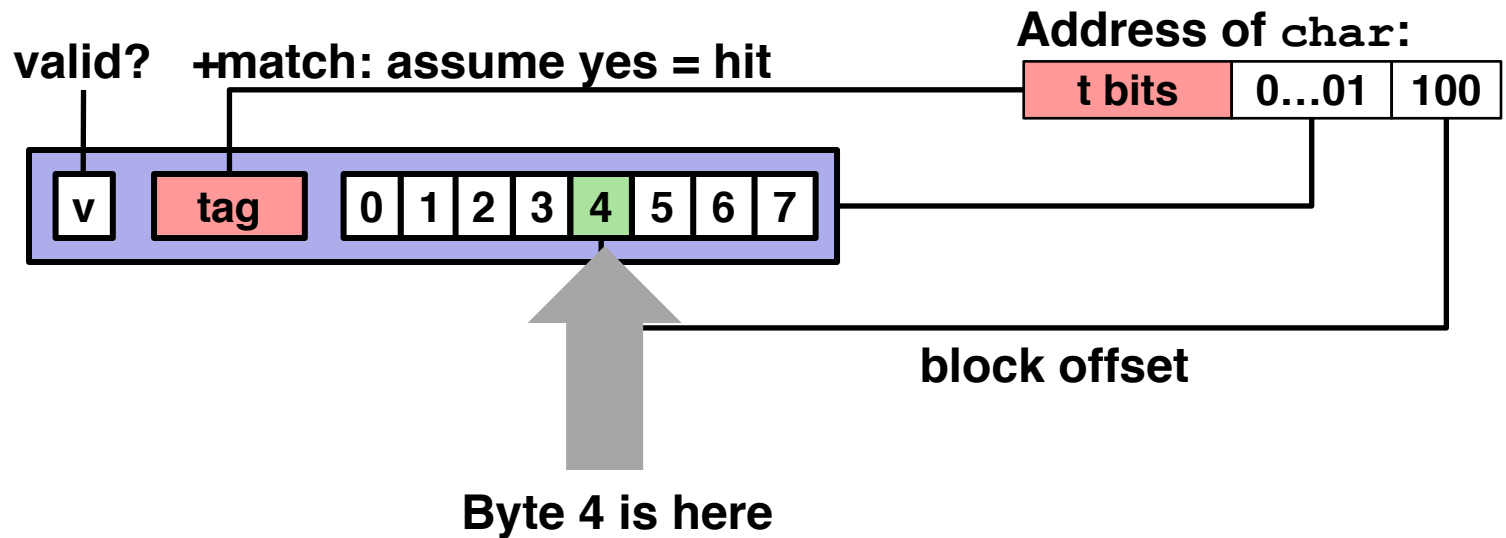
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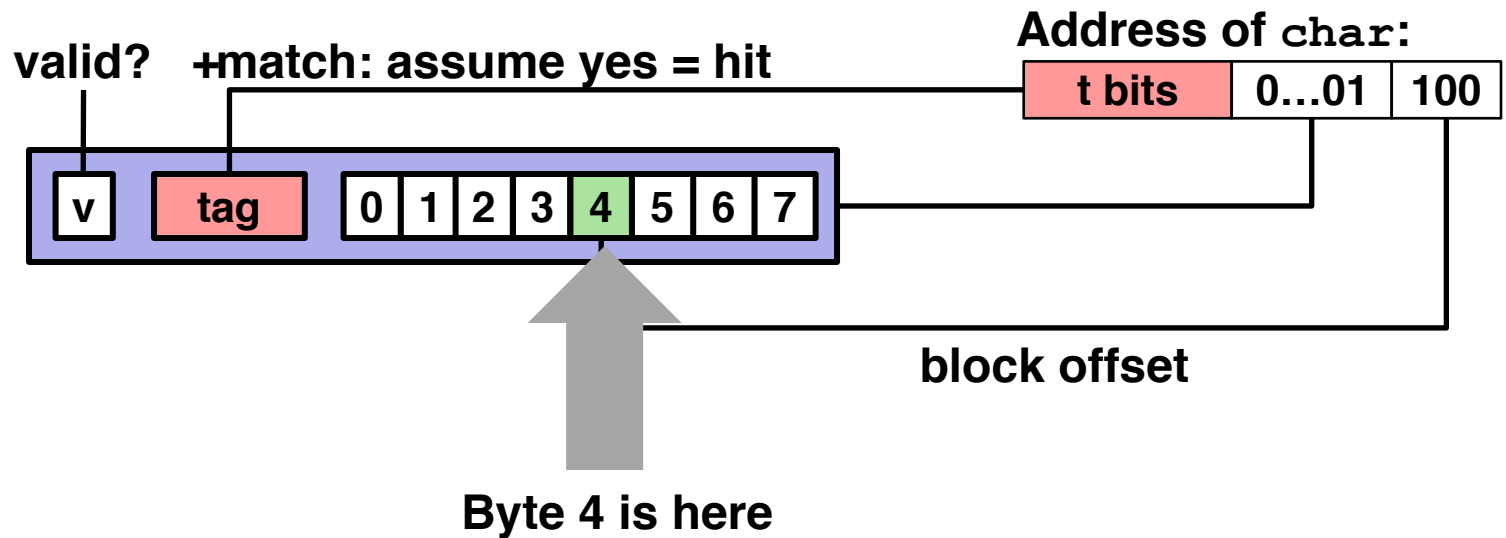
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If tag doesn't match: old line is evicted and replaced

Direct-Mapped Cache Simulation

t=1	s=2	b=1
x	xx	x

4-bit address space, i.e., Memory = 16 bytes

B=2 bytes/line, S=4 sets, E=1 line/set

Address trace (reads, one byte per read):

0 [0000₂],
 1 [0001₂],
 7 [0111₂],
 8 [1000₂],
 0 [0000₂]

	v	Tag	Line
Set 0	0	?	?
Set 1			
Set 2			
Set 3			

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Set 2			
Set 3	1	0	M[6-7]

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0	[<u>0000</u> ₂]	

	v	Tag	Line	
Set 0	1	0	M[0-1]	← The two bytes at memory address 0 and 1
Set 1				
Set 2				
Set 3	1	0	M[6-7]	← The two bytes at memory address 6 and 7

Direct-Mapped Cache Simulation

t=1	s=2	b=1
x	xx	x

4-bit address space, i.e., Memory = 16 bytes

B=2 bytes/line, S=4 sets, E=1 line/set

Address trace (reads, one byte per read):

0	[<u>0000</u> ₂],	miss
1	[<u>0001</u> ₂],	hit
7	[<u>0111</u> ₂],	miss
8	[<u>1000</u> ₂],	miss
0	[<u>0000</u> ₂]	

	v	Tag	Line	
Set 0	1	0	M[0-1]	← The two bytes at memory address 0 and 1
Set 1				
Set 2				
Set 3	1	0	M[6-7]	← The two bytes at memory address 6 and 7

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1	[<u>0001</u> ₂],	hit
7	[<u>0111</u> ₂],	miss
8	[<u>1000</u> ₂],	miss
0	[<u>0000</u> ₂]	

	v	Tag	Line	
Set 0	1	1	M[8-9]	← The two bytes at memory address 8 and 9
Set 1				
Set 2				
Set 3	1	0	M[6-7]	← The two bytes at memory address 6 and 7

Direct-Mapped Cache Simulation

t=1	s=2	b=1
x	xx	x

4-bit address space, i.e., Memory = 16 bytes

B=2 bytes/line, S=4 sets, E=1 line/set

Address trace (reads, one byte per read):

0	[<u>0000</u> ₂],	miss
1	[<u>0001</u> ₂],	hit
7	[<u>0111</u> ₂],	miss
8	[<u>1000</u> ₂],	miss
0	[<u>0000</u> ₂]	miss

	v	Tag	Line	
Set 0	1	1	M[8-9]	← The two bytes at memory address 8 and 9
Set 1				
Set 2				
Set 3	1	0	M[6-7]	← The two bytes at memory address 6 and 7

Direct-Mapped Cache Simulation

t=1	s=2	b=1
x	xx	x

4-bit address space, i.e., Memory = 16 bytes

B=2 bytes/line, S=4 sets, E=1 line/set

Address trace (reads, one byte per read):

0	[<u>0000</u> ₂],	miss
1	[<u>0001</u> ₂],	hit
7	[<u>0111</u> ₂],	miss
8	[<u>1000</u> ₂],	miss
0	[<u>0000</u> ₂]	miss

	v	Tag	Line	
Set 0	1	0	M[0-1]	← The two bytes at memory address 0 and 1
Set 1				
Set 2				
Set 3	1	0	M[6-7]	← The two bytes at memory address 6 and 7

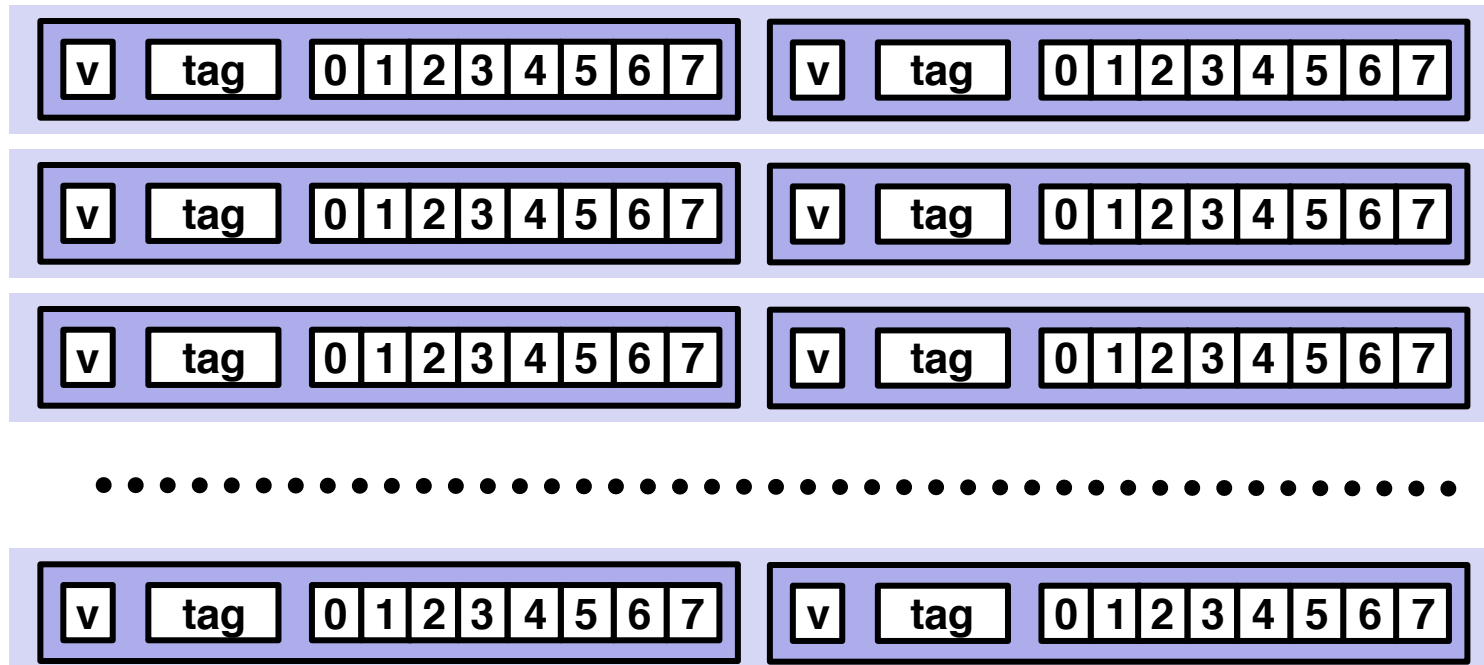
E-way Set Associative Cache (Here: E = 2)

E = 2: Two lines per set

Assume: cache line size 8 bytes

Address of short int:

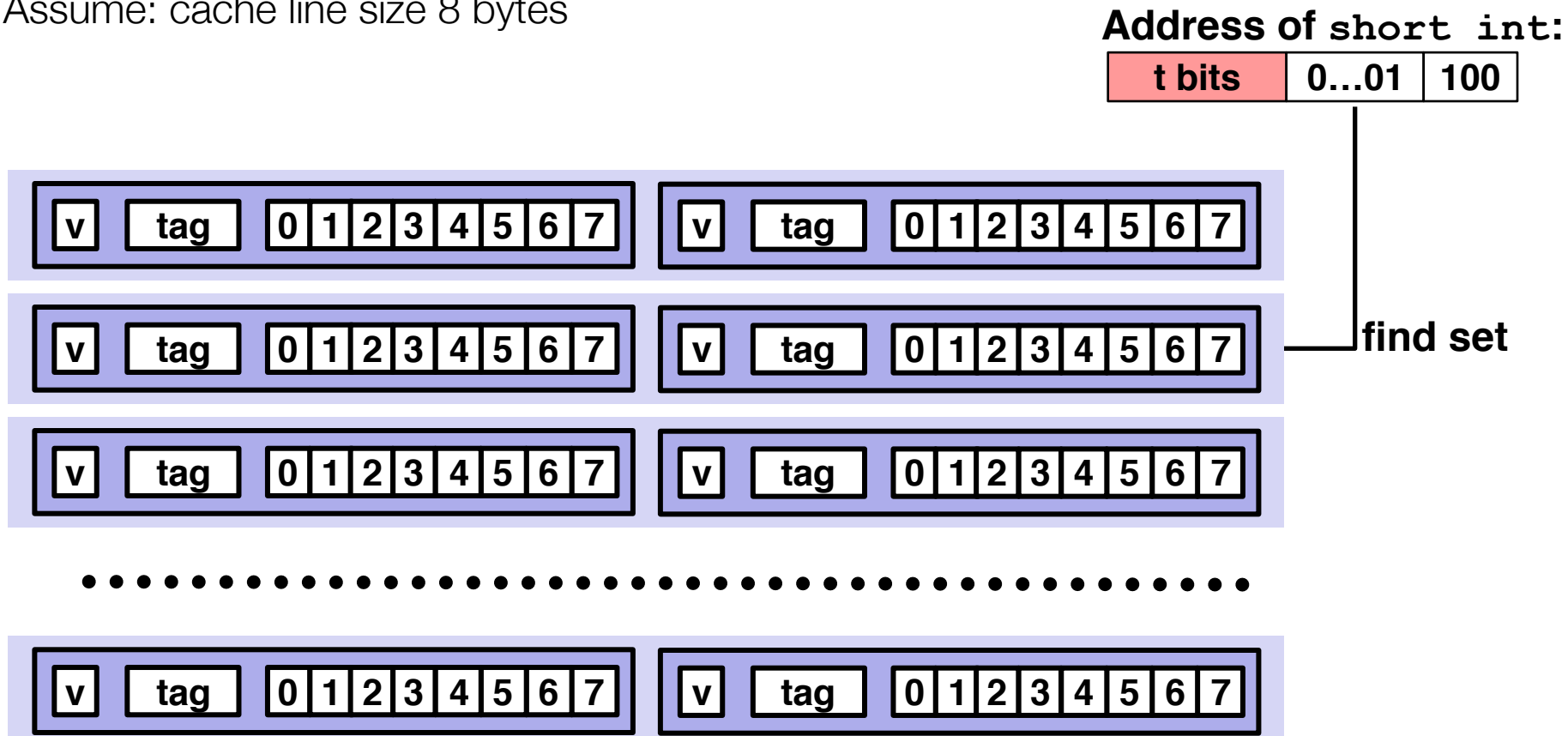
t bits	0...01	100
--------	--------	-----



E-way Set Associative Cache (Here: E = 2)

E = 2: Two lines per set

Assume: cache line size 8 bytes



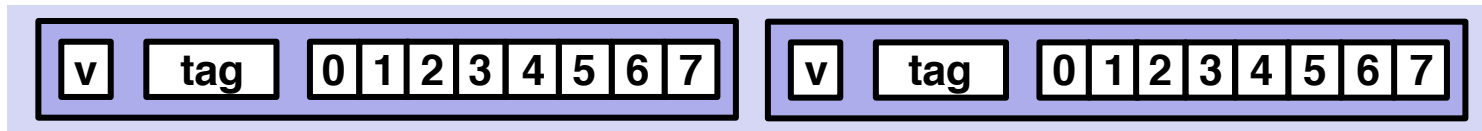
E-way Set Associative Cache (Here: E = 2)

E = 2: Two lines per set

Assume: cache line size 8 bytes

Address of short int:

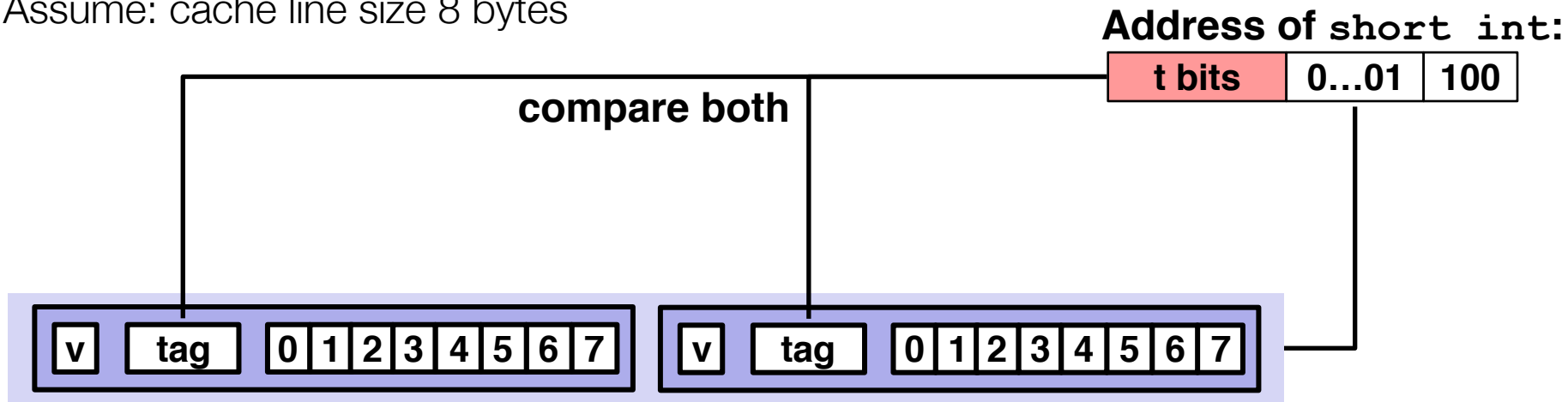
t bits	0...01	100
--------	--------	-----



E-way Set Associative Cache (Here: E = 2)

E = 2: Two lines per set

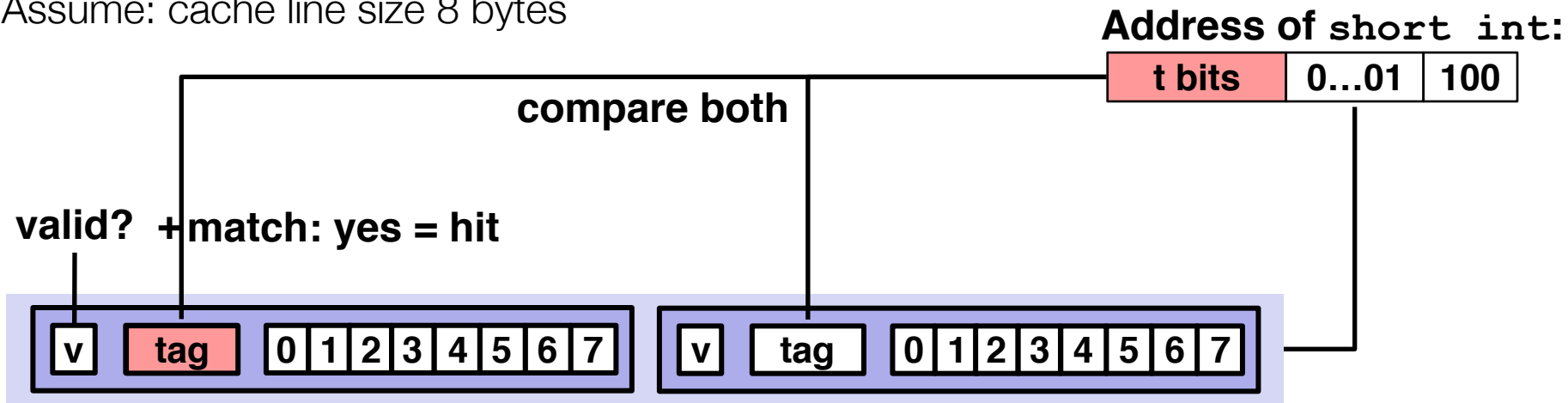
Assume: cache line size 8 bytes



E-way Set Associative Cache (Here: E = 2)

E = 2: Two lines per set

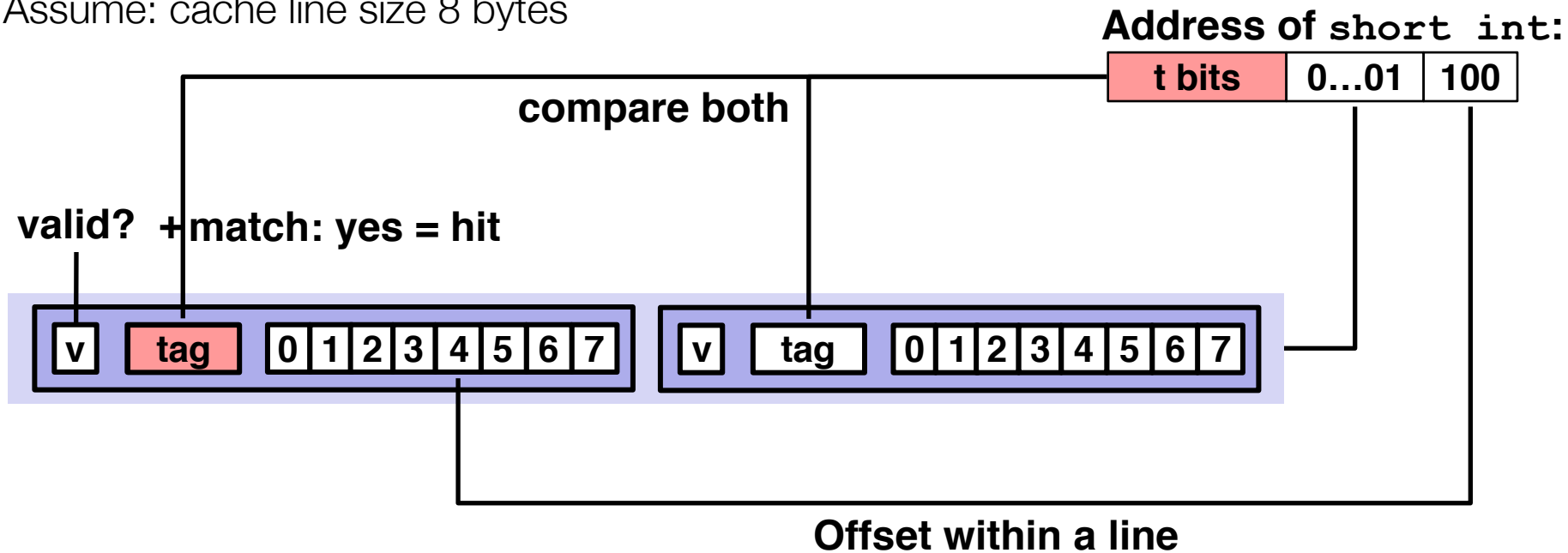
Assume: cache line size 8 bytes



E-way Set Associative Cache (Here: E = 2)

E = 2: Two lines per set

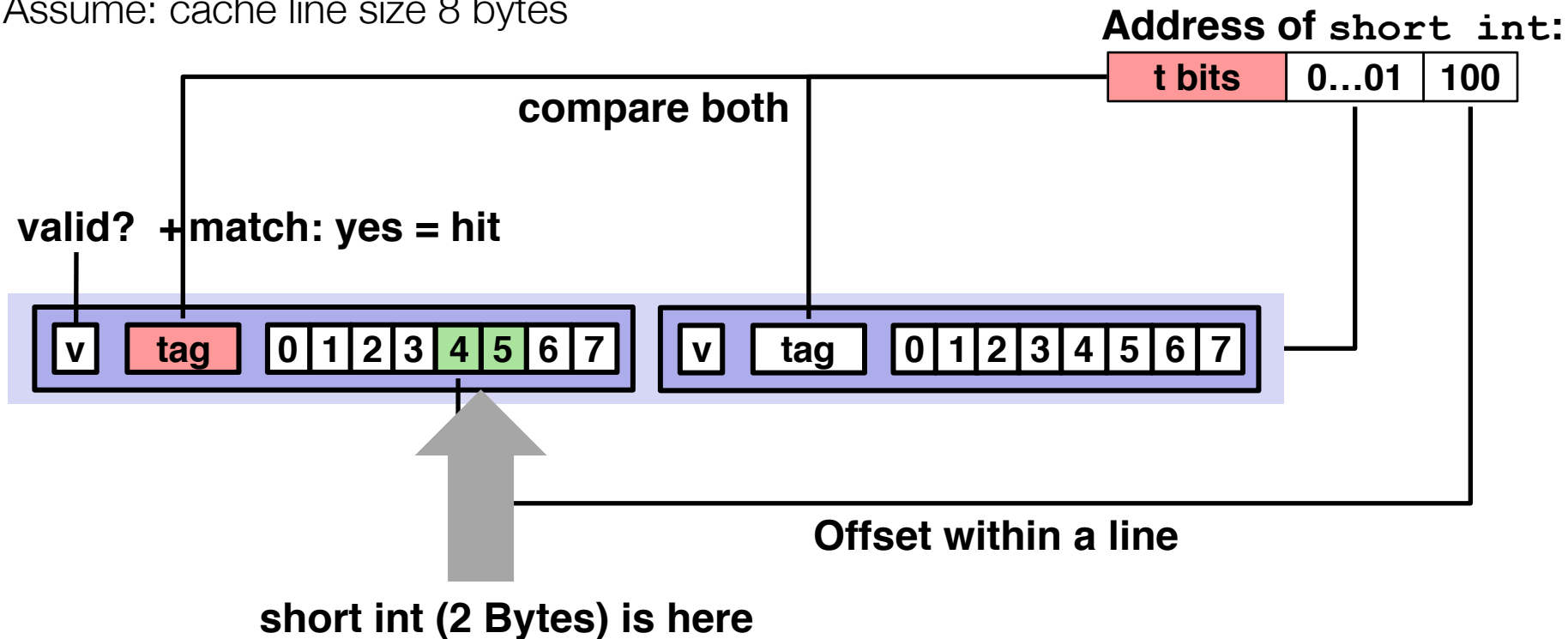
Assume: cache line size 8 bytes



E-way Set Associative Cache (Here: E = 2)

E = 2: Two lines per set

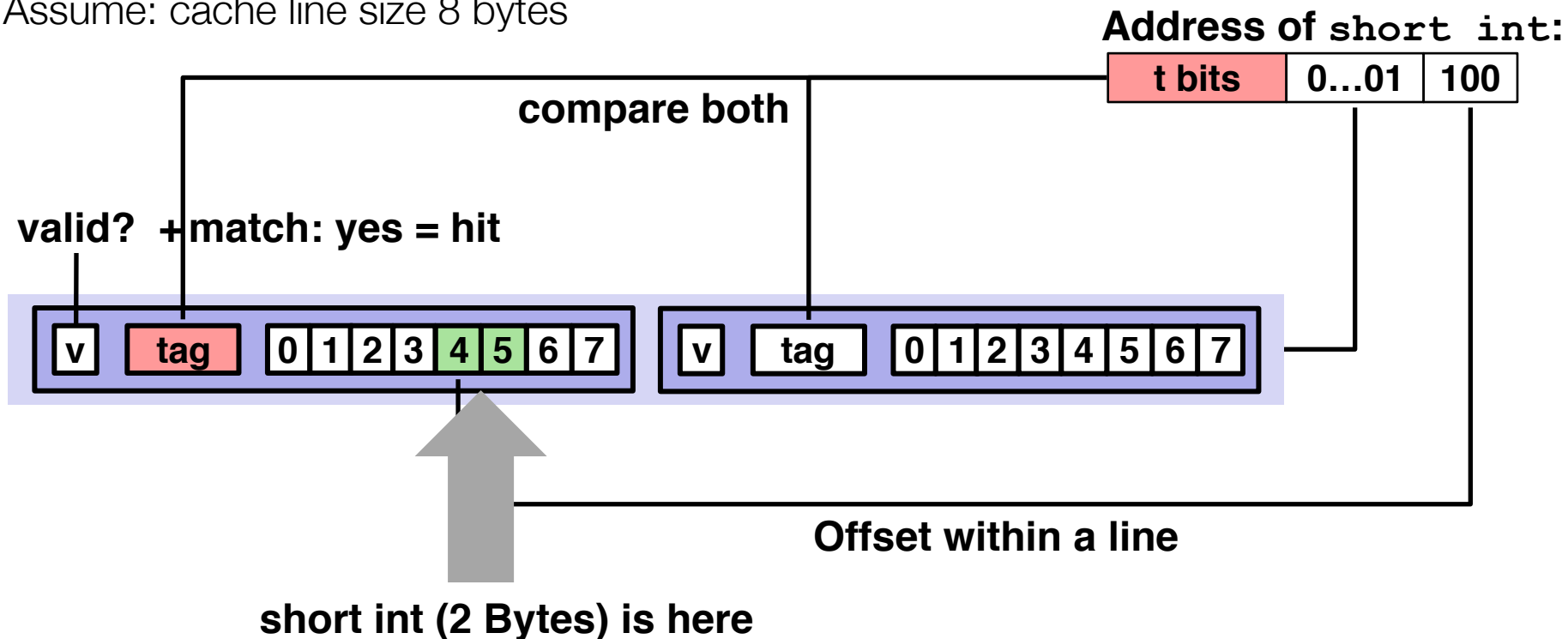
Assume: cache line size 8 bytes



E-way Set Associative Cache (Here: E = 2)

E = 2: Two lines per set

Assume: cache line size 8 bytes



No match:

- One line in set is selected for eviction and replacement
- Replacement policies: random, least recently used (LRU),

2-Way Set Associative Cache Simulation

t=2	s=1	b=1
xx	x	x

4-bit address space, i.e., Memory = 16 bytes
 S=2 sets, E=2 cache lines/set

Address trace (reads, one byte per read):

0 [0000₂],
 1 [0001₂],
 7 [0111₂],
 8 [1000₂],
 0 [0000₂]

	v	Tag	Line			
Set 0	0	?	?	0		
Set 1	0			0		

2-Way Set Associative Cache Simulation

t=2	s=1	b=1
xx	x	x

4-bit address space, i.e., Memory = 16 bytes
 S=2 sets, E=2 cache lines/set

Address trace (reads, one byte per read):

0 [0000₂], miss
 1 [0001₂],
 7 [0111₂],
 8 [1000₂],
 0 [0000₂]

	v	Tag	Line			
Set 0	0	?	?	0		
Set 1	0			0		

2-Way Set Associative Cache Simulation

t=2	s=1	b=1
xx	x	x

4-bit address space, i.e., Memory = 16 bytes
 S=2 sets, E=2 cache lines/set

Address trace (reads, one byte per read):

0 [0000₂], miss
 1 [0001₂],
 7 [0111₂],
 8 [1000₂],
 0 [0000₂]

	v	Tag	Line			
Set 0	1	00	M[0-1]	0		
Set 1	0			0		

2-Way Set Associative Cache Simulation

t=2	s=1	b=1
xx	x	x

4-bit address space, i.e., Memory = 16 bytes
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1	[0001 ₂],	hit
7	[0111 ₂],	
8	[1000 ₂],	
0	[0000 ₂]	

	v	Tag	Line			
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Set 1	0			0		

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8	[1000 ₂],	
0	[0000 ₂]	

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Set 0	1	00	M[0-1]	0		
Set 1	0			0		

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8	[1000 ₂],	
0	[0000 ₂]	

	v	Tag	Line			
Set 0	1	00	M[0-1]	0		
Set 1	1	01	M[6-7]	0		

2-Way Set Associative Cache Simulation

t=2	s=1	b=1
xx	x	x

4-bit address space, i.e., Memory = 16 bytes
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0	[0000 ₂]	

	v	Tag	Line			
Set 0	1	00	M[0-1]	0		
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8	[1000 ₂],	miss
0	[0000 ₂]	

	v	Tag	Line			
Set 0	1	00	M[0-1]	1	10	M[8-9]
Set 1	1	01	M[6-7]	0		

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	v	Tag	Line			
Set 0	1	00	M[0-1]	1	10	M[8-9]
Set 1	1	01	M[6-7]	0		