

# **CSC 252: Computer Organization**

## **Spring 2022: Lecture 5**

Instructor: Yuhao Zhu

Department of Computer Science  
University of Rochester

# Announcement

- Programming Assignment 1 is out
  - Details: <https://www.cs.rochester.edu/courses/252/spring2022/labs/assignment1.html>
  - Due on Jan. 30, 11:59 PM (extended)
  - You have 3 slip days

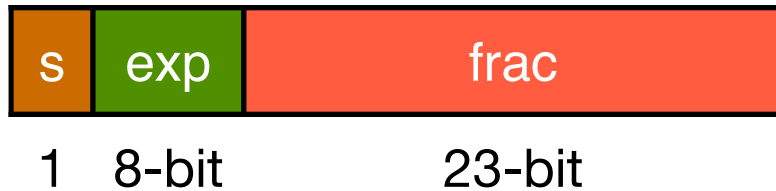
23	24	25	26	27 Today	28	29
30 Due	31	Feb 1	2	3	4	5

# Announcement

- Programming assignment 1 is in C language. Seek help from TAs.
- TAs are best positioned to answer your questions about programming assignments!!!
- Programming assignments do NOT repeat the lecture materials. They ask you to synthesize what you have learned from the lectures and work out something new.

# IEEE 754 Floating Point Standard

- Single precision: 32 bits



- Double precision: 64 bits



- In C language

- `float`      single precision
- `double`    double precision

# Floating Point in C

## 32-bit Machine

Fixed point  
(implicit binary point)



SP floating point

DP floating point

C Data Type	Bits	Max Value	Max Value (Decimal)
<b>char</b>	8	$2^7 - 1$	127
<b>short</b>	16	$2^{15} - 1$	32767
<b>int</b>	32	$2^{31} - 1$	2147483647
<b>long</b>	64	$2^{63} - 1$	$\sim 9.2 \times 10^{18}$
<b>float</b>	32	$(2 - 2^{-23}) \times 2^{127}$	$\sim 3.4 \times 10^{38}$
<b>double</b>	64	$(2 - 2^{-52}) \times 2^{1023}$	$\sim 1.8 \times 10^{308}$

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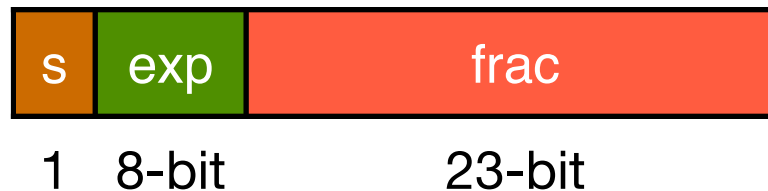
- To represent  $2^{31}$  in fixed-point, you need at least 32 bits
  - Because fixed-point is a *weighted positional* representation
- In floating-point, we directly encode the exponent
  - Floating point is based on scientific notation
  - Encoding 31 only needs 7 bits in the *exp* field

# Floating Point Conversions/Casting in C

- **double/float → int**
  - Truncates fractional part
  - Like rounding toward zero
  - Not defined when out of range or NaN

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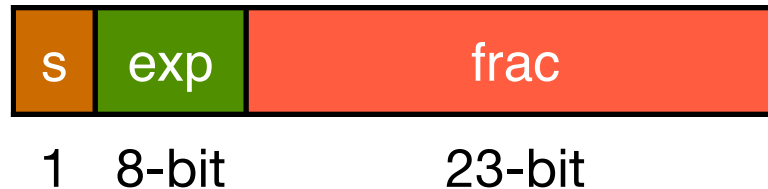
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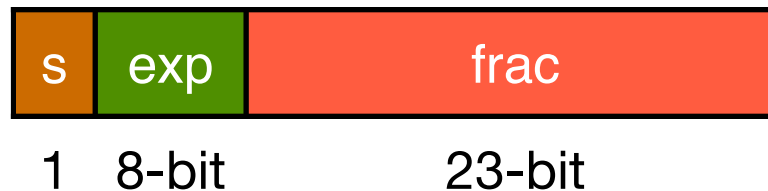
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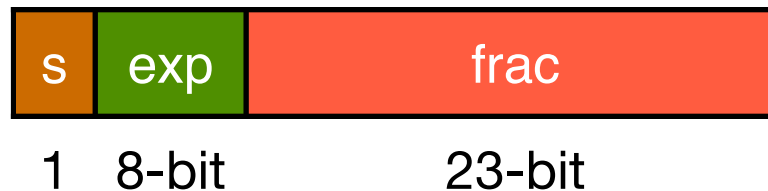
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- Exact conversion

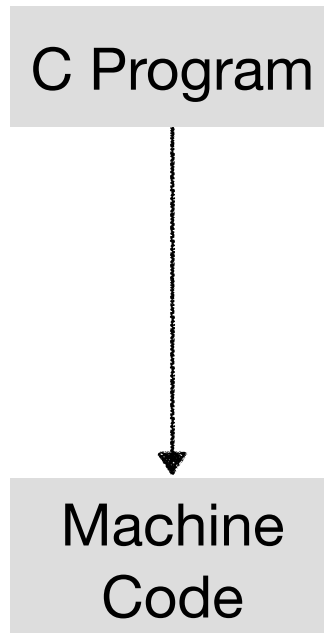


# So far in 252...

C Program

**int, float**  
if, else  
+, -, >>

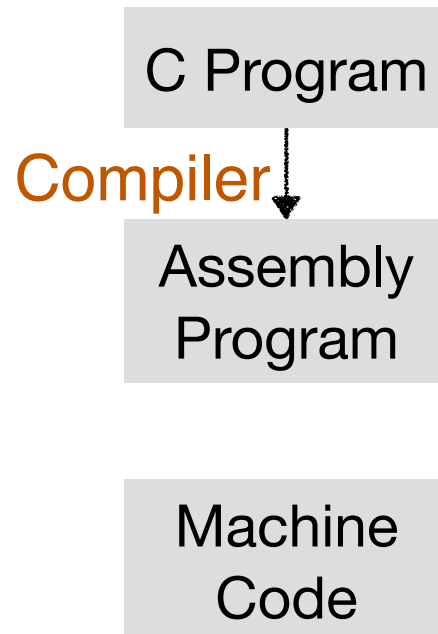
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if, else  
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00001111  
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11110000

# So far in 252...

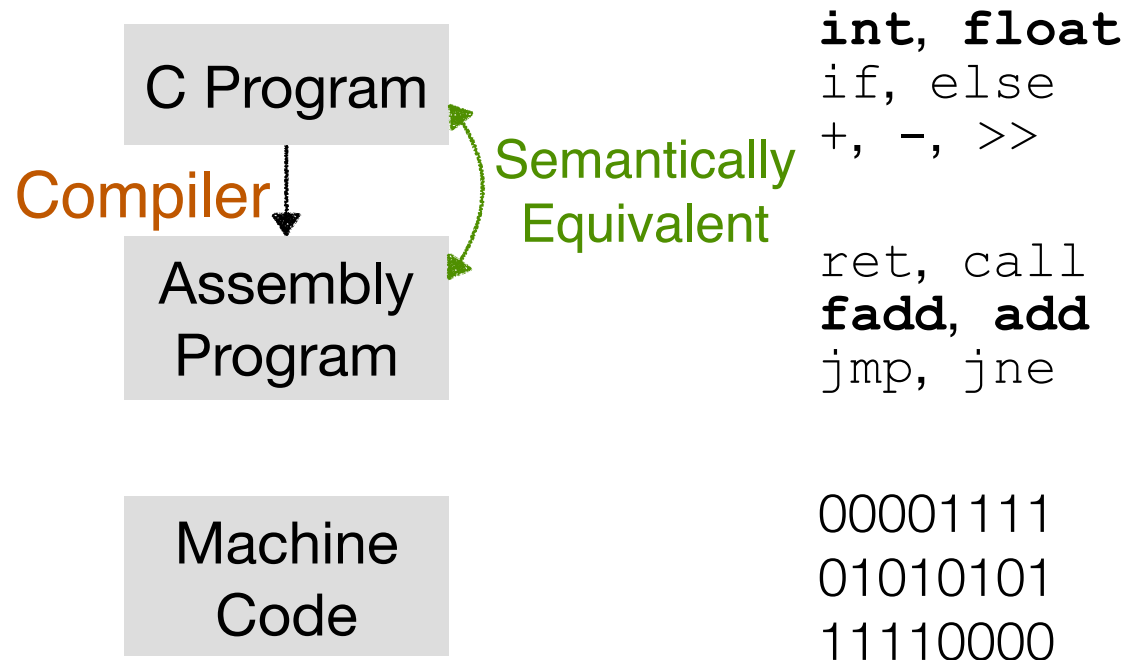


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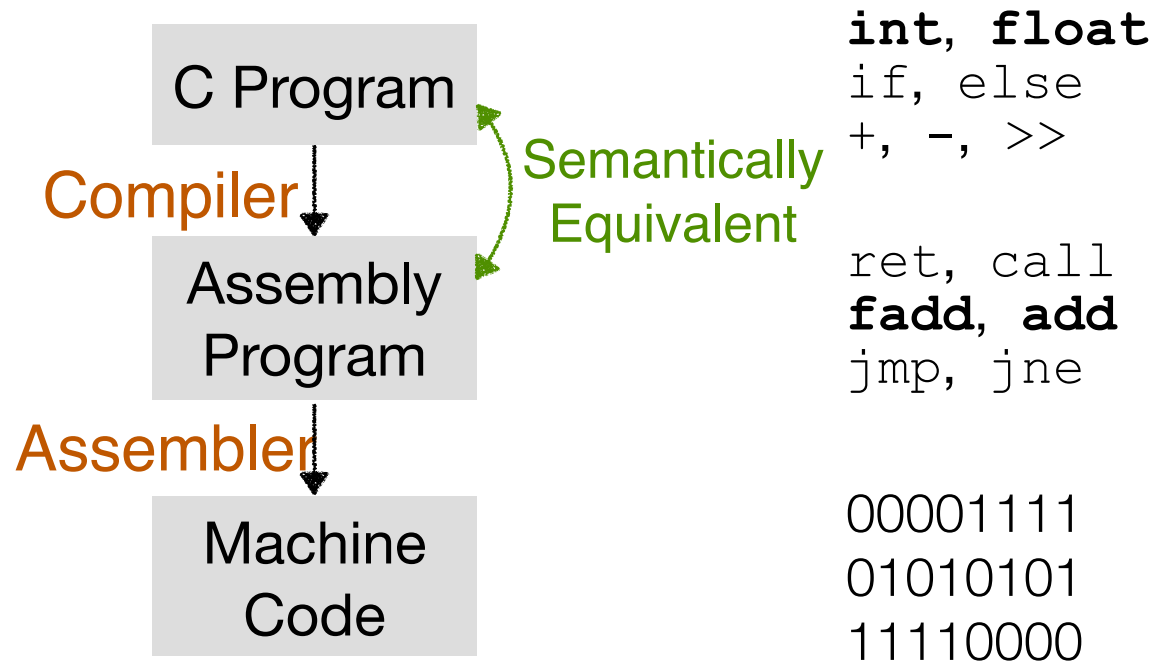
ret, call  
**fadd, add**  
jmp, jne

00001111  
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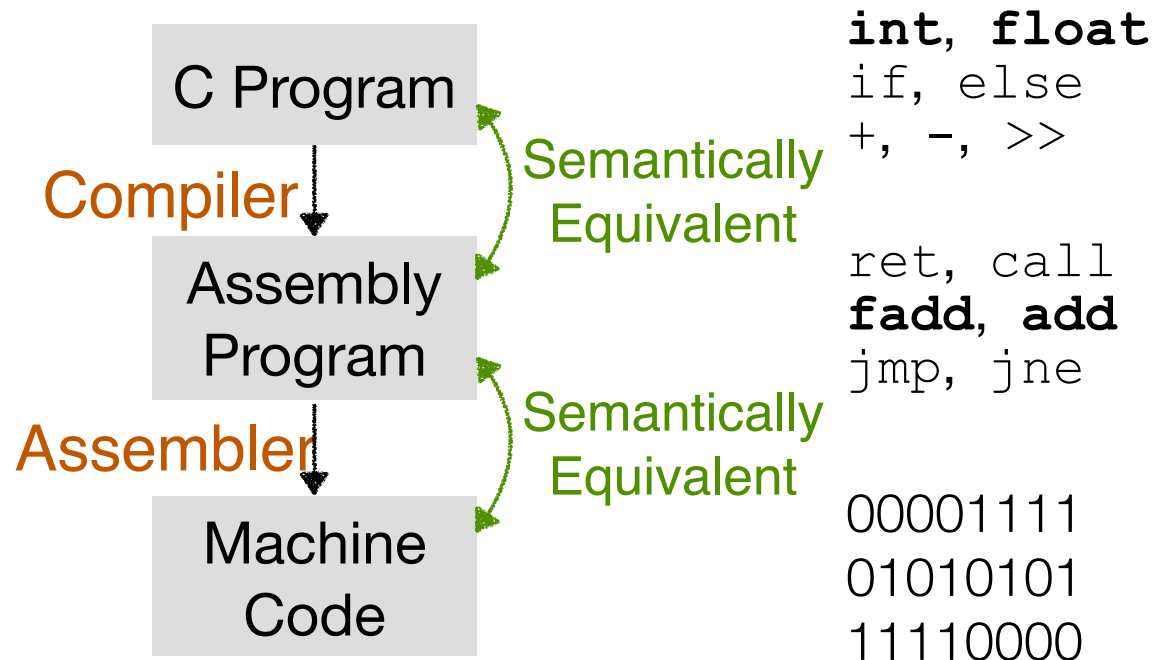


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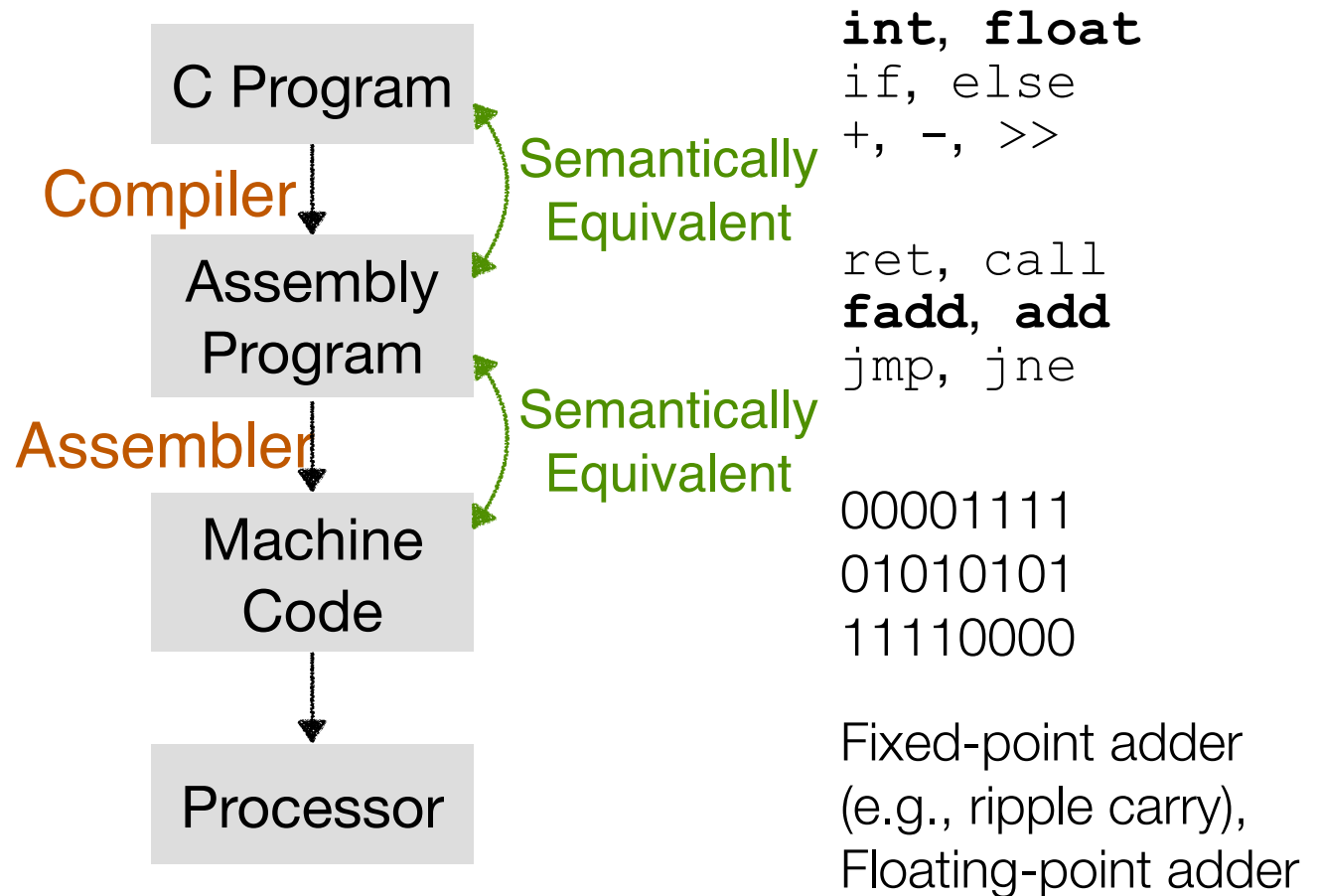




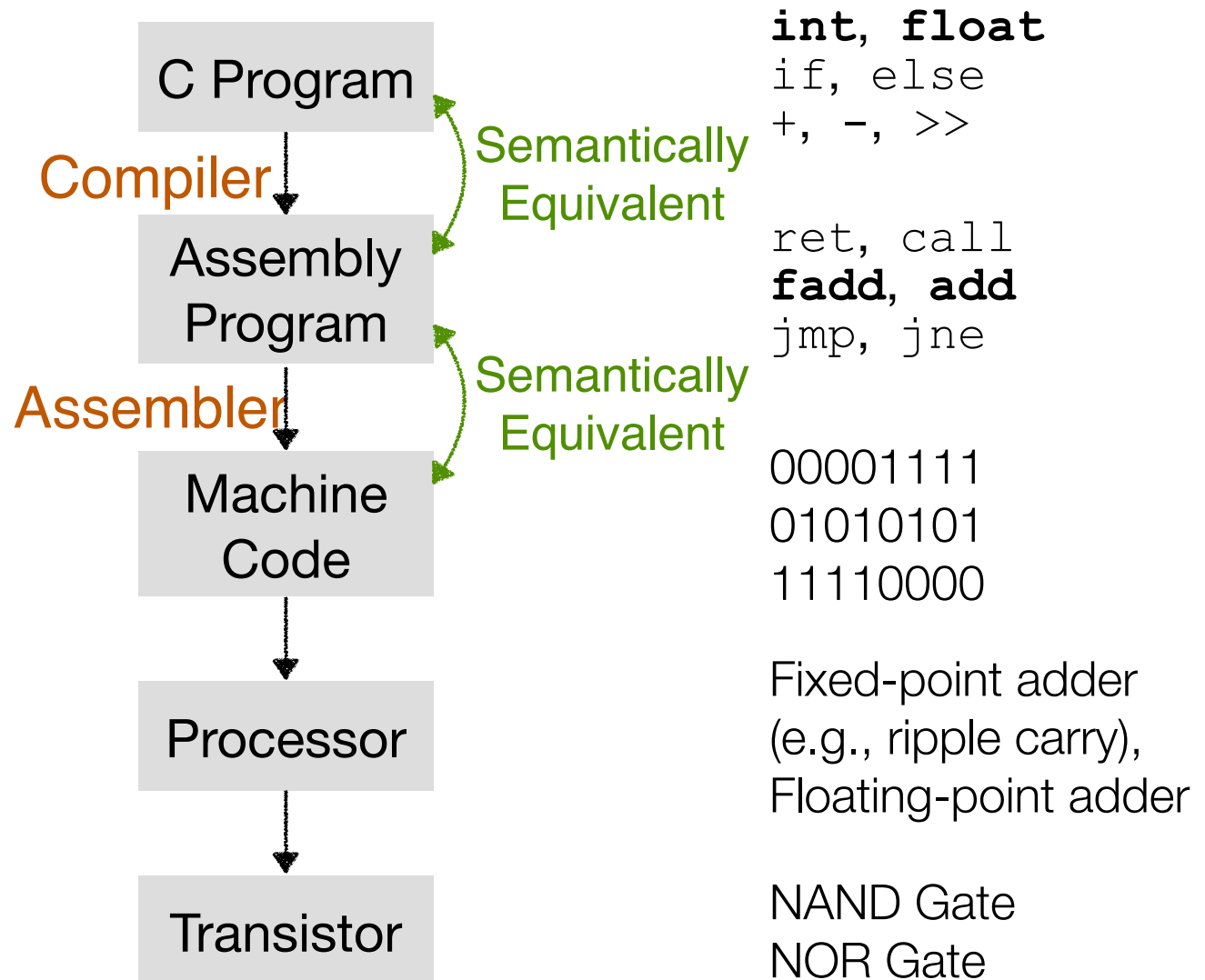
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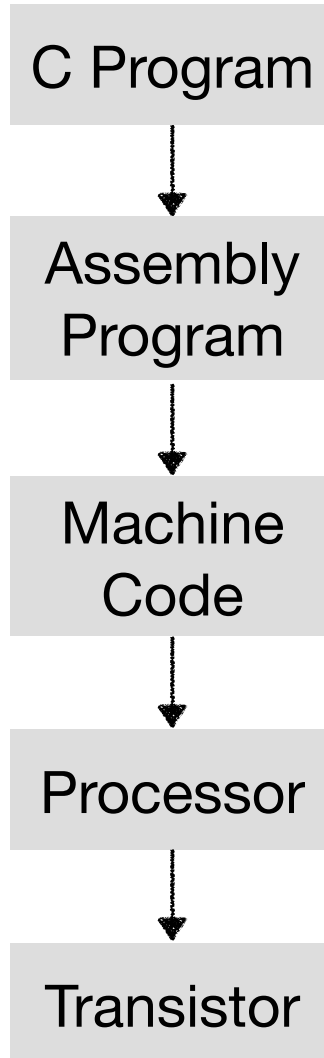
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**High-Level  
Language**

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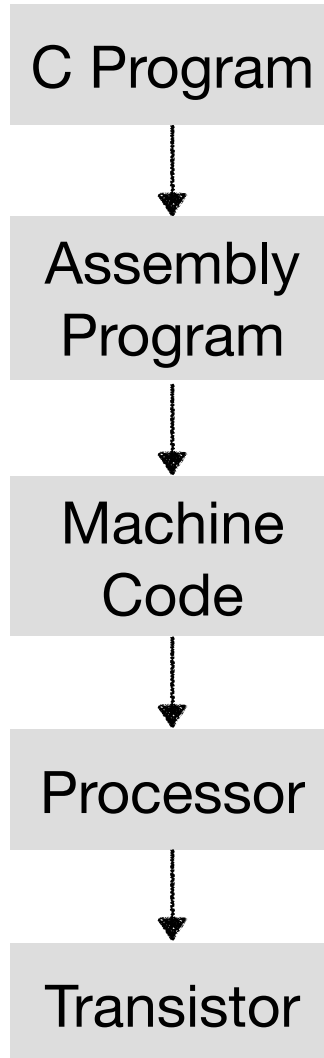
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High-Level  
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Instruction Set  
Architecture  
(ISA)

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- **ISA:** Software programmers' view of a computer
  - Provide all info for someone wants to write assembly/machine code
  - “Contract” between assembly/machine code and processor

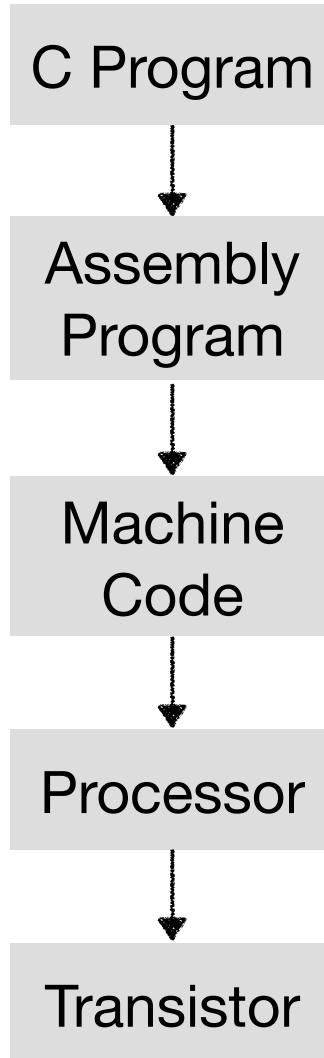
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Instruction Set  
Architecture  
(ISA)

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Microarchitecture

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Circuit

C Program



Assembly  
Program



Machine  
Code



Processor



Transistor

- **ISA**: Software programmers' view of a computer
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- Processors execute machine code (binary). Assembly program is merely a text representation of machine code
- **Microarchitecture**: Hardware implementation of the ISA (with the help of circuit technologies)

# This Module (4 Lectures)

High-Level  
Language

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Instruction Set  
Architecture  
(ISA)

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Microarchitecture

---

Circuit

C Program

Assembly  
Program

Machine  
Code

Processor

Transistor

- **Assembly Programming**

- Explain how various C constructs are implemented in assembly code
- Effectively translating from C to assembly program manually
- Helps us understand how compilers work
- Helps us understand how assemblers work

- **Microarchitecture is the topic of the next module**



# Today: Assembly Programming I: Basics

- Different ISAs and history behind them
- C, assembly, machine code
- Move operations (and addressing modes)

# Instruction Set Architecture

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  - x86, ARM, Power/PowerPC, Sparc, MIPS, IA64, z
  - Very consolidated today: ARM for mobile, x86 for others

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  - Intel and AMD have different microarchitectures for x86

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  - Apple/Samsung/Qualcomm have their own microarchitecture (implementation) of the ARM ISA
  - Intel and AMD have different microarchitectures for x86
- ISA is lucrative business: ARM's Business Model
  - Patent the ISA, and then license the ISA
  - Every implementer pays a royalty to ARM
  - Apple/Samsung pays ARM whenever they sell a smartphone

The ARM Diaries, Part 1: How ARM's Business Model Works: <https://www.anandtech.com/show/7112/the-arm-diaries-part-1-how-arms-business-model-works>

# Intel x86 ISA

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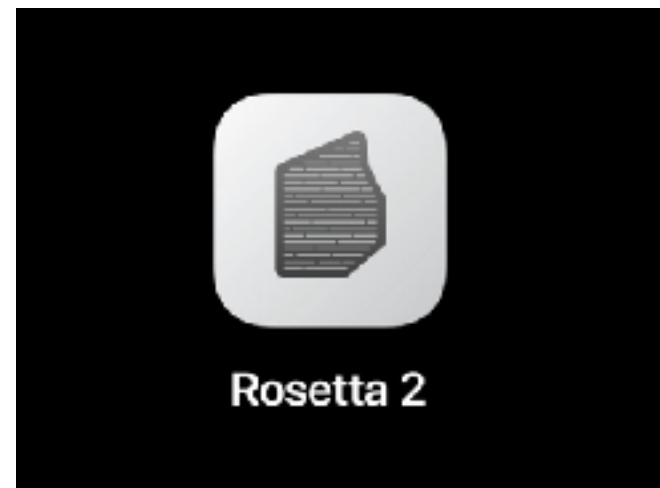
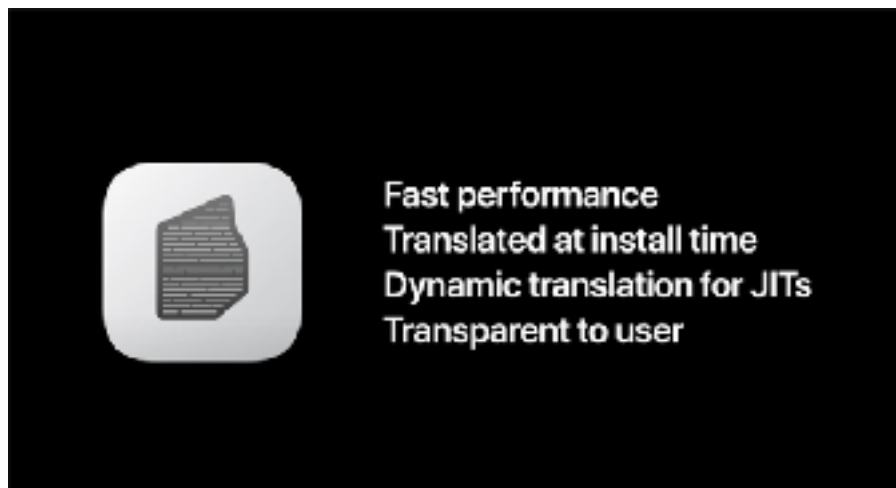




# Aside: Dynamic Binary Translation



- Apple M1 is based on the Arm ISA. A program compiled to x86 ISA is dynamically translated to Arm ISA by Rosetta.
- Not the first time Apple plays this trick.



# Aside: Dynamic Binary Translation

Circa 2006: PowerPC to x86 translation

# Rosetta

Translates PowerPC to Intel



# Intel x86 ISA Evolution (Milestones)

- Evolutionary design: Added more features as time goes on

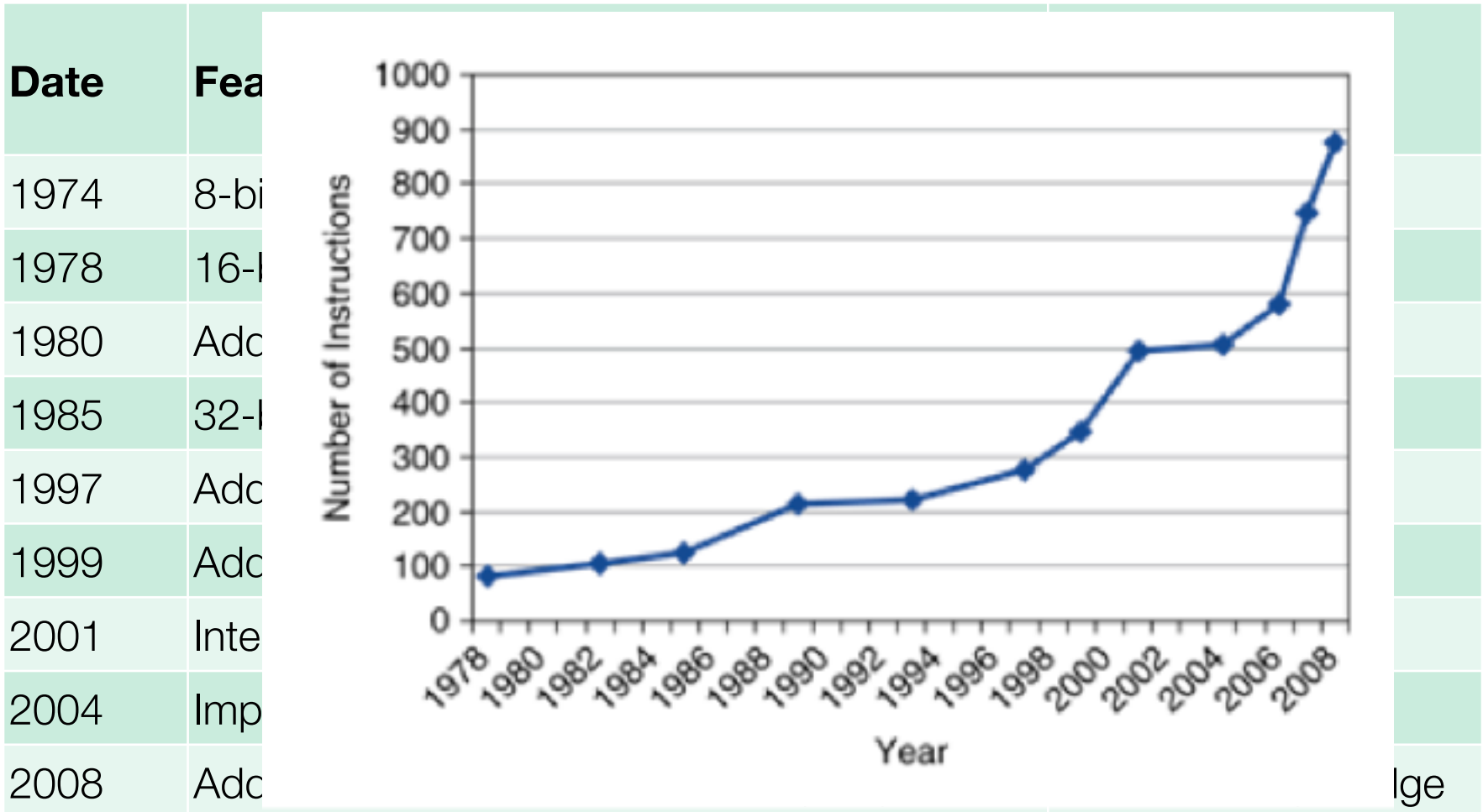
# Intel x86 ISA Evolution (Milestones)

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Date	Feature	Notable Implementation
1974	8-bit ISA	8080
1978	16-bit ISA (Basis for IBM PC & DOS)	8086
1980	Add Floating Point instructions	8087
1985	32-bit ISA (Refer to as IA32)	386
1997	Add Multi-Media eXtension (MMX)	Pentium/MMX
1999	Add Streaming SIMD Extension (SSE)	Pentium III
2001	Intel's first attempt at 64-bit ISA (IA64, failed)	Itanium
2004	Implement AMD's 64-bit ISA (x86-64, AMD64)	Pentium 4E
2008	Add Advanced Vector Extension (AVE)	Core i7 Sandy Bridge

# Intel x86 ISA Evolution (Milestones)

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# Backward Compatibility

- Binary executable generated for an older processor can execute on a newer processor
- Allows legacy code to be executed on newer machines
  - Buy new machines without changing the software
- **x86 is backward compatible up until 8086 (16-bit ISA)**
  - i.e., an 8086 binary executable can be executed on any of today's x86 machines
- **Great for users, nasty for processor implementers**
  - Every instruction you put into the ISA, you are stuck with it *FOREVER*

# x86 Clones: Advanced Micro Devices (AMD)



- **Historically**

- AMD build processors for x86 ISA
- A little bit slower, a lot cheaper

- **Then**

- Recruited top circuit designers from Digital Equipment Corp. and other downward trending companies
- Developed x86-64, their own 64-bit x86 extension to IA32
- Built first 1 GHz CPU
- **Intel felt hard to admit mistake or that AMD was better**
- **2004: Intel Announces EM64T extension to IA32**
  - Almost identical to x86-64!
  - Today's 64-bit x86 ISA is basically AMD's original proposal

# x86 Clones: Advanced Micro Devices (AMD)

- Today: Holding up not too badly



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# Our Coverage

- **IA32**

- The traditional x86
- 2<sup>nd</sup> edition of the textbook

- **x86-64**

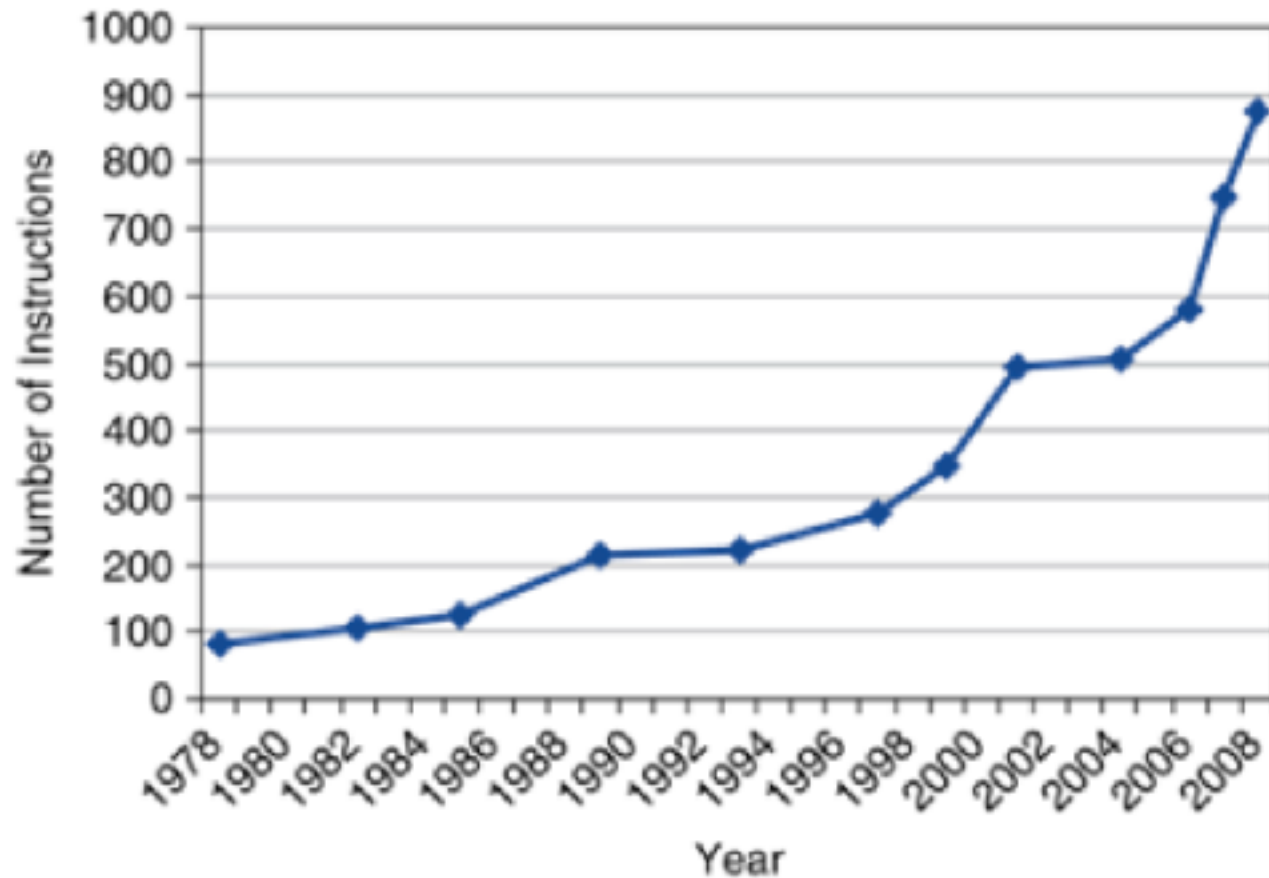
- The standard
- CSUG machine
- 3<sup>rd</sup> edition of the textbook
- Our focus

# Moore's Law

- More instructions typically require more transistors to implement

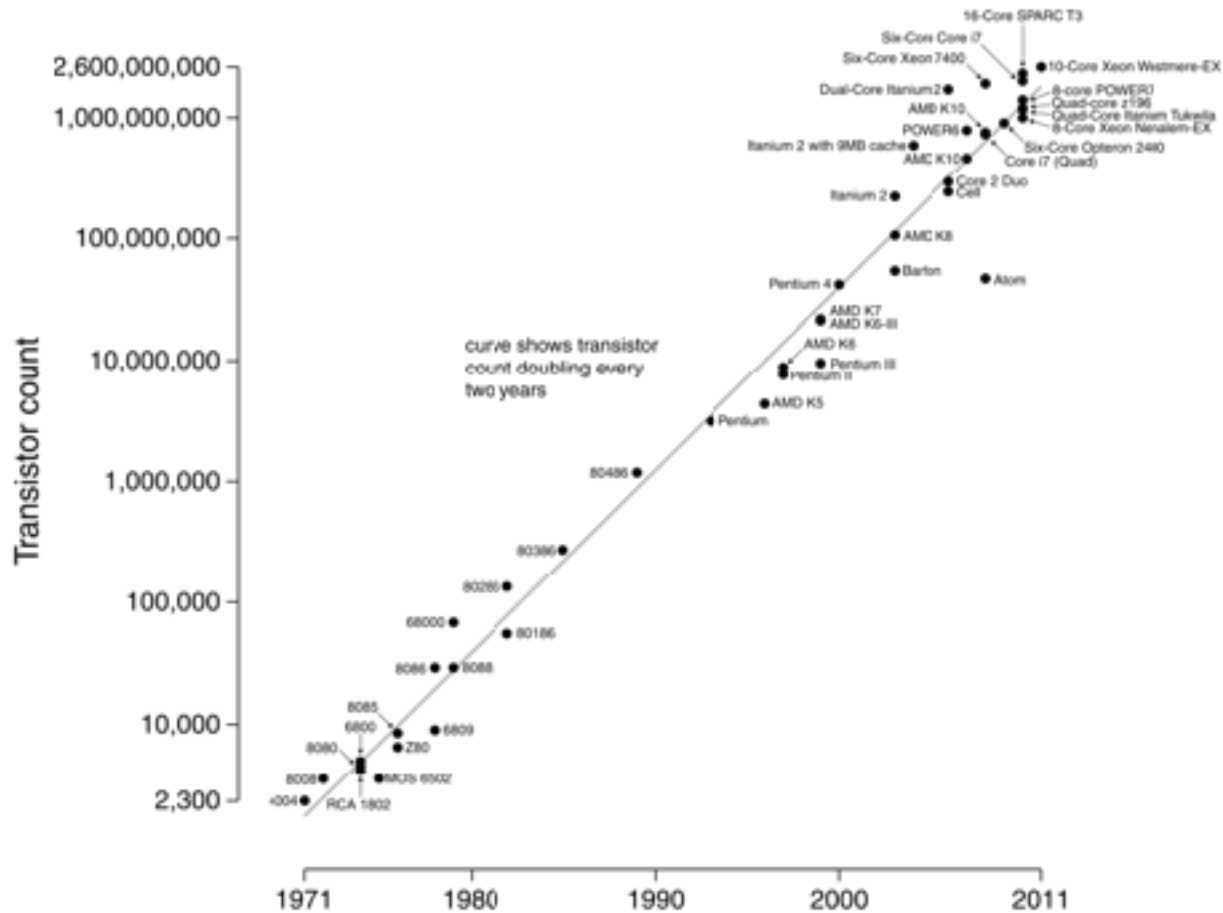
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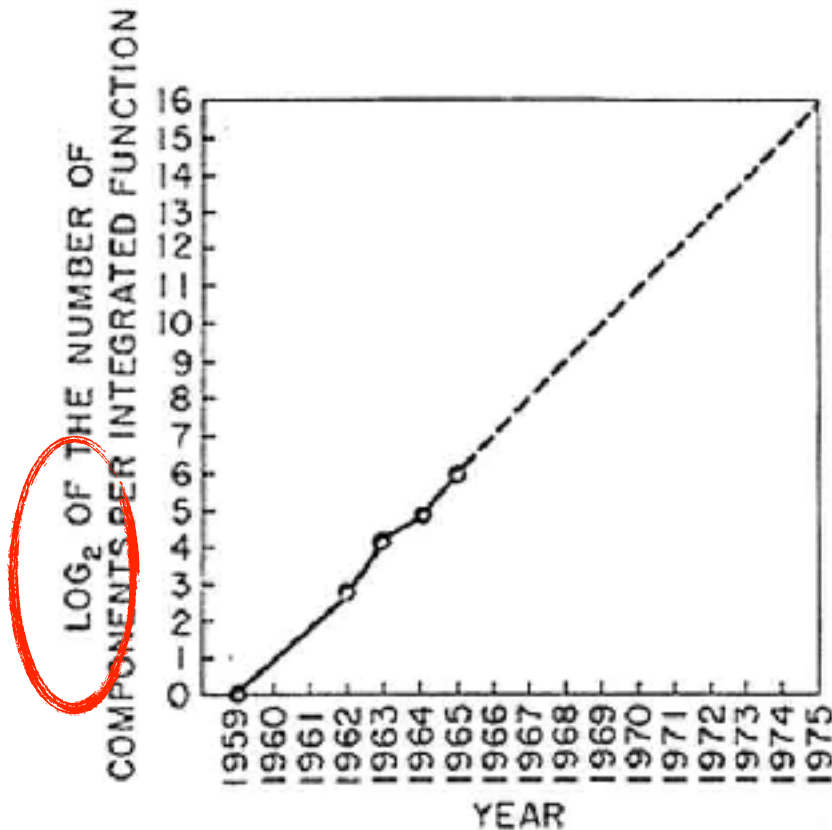
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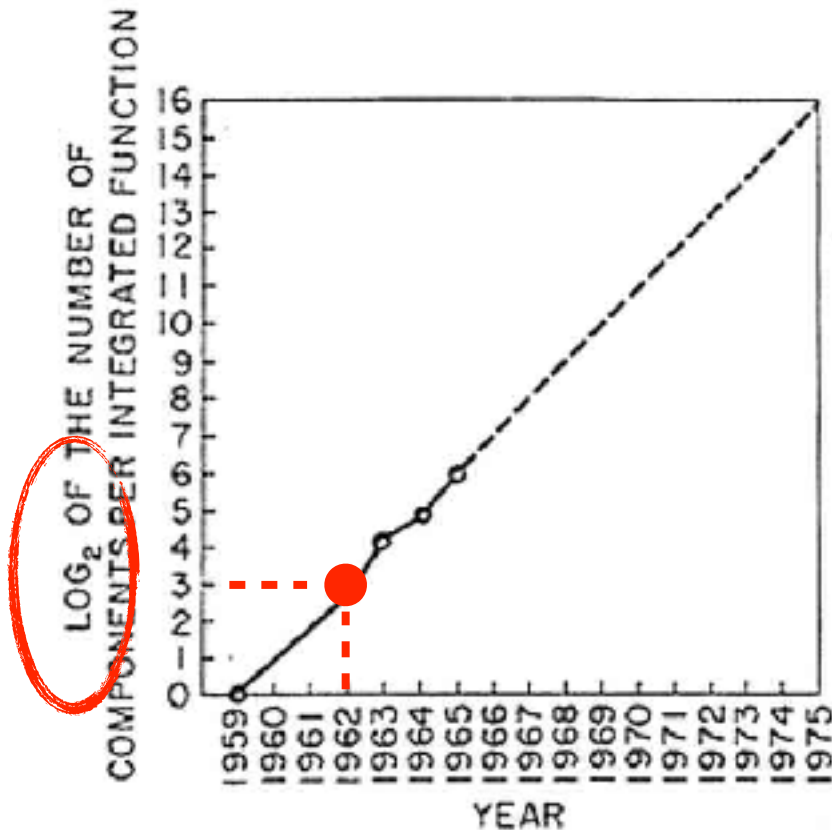
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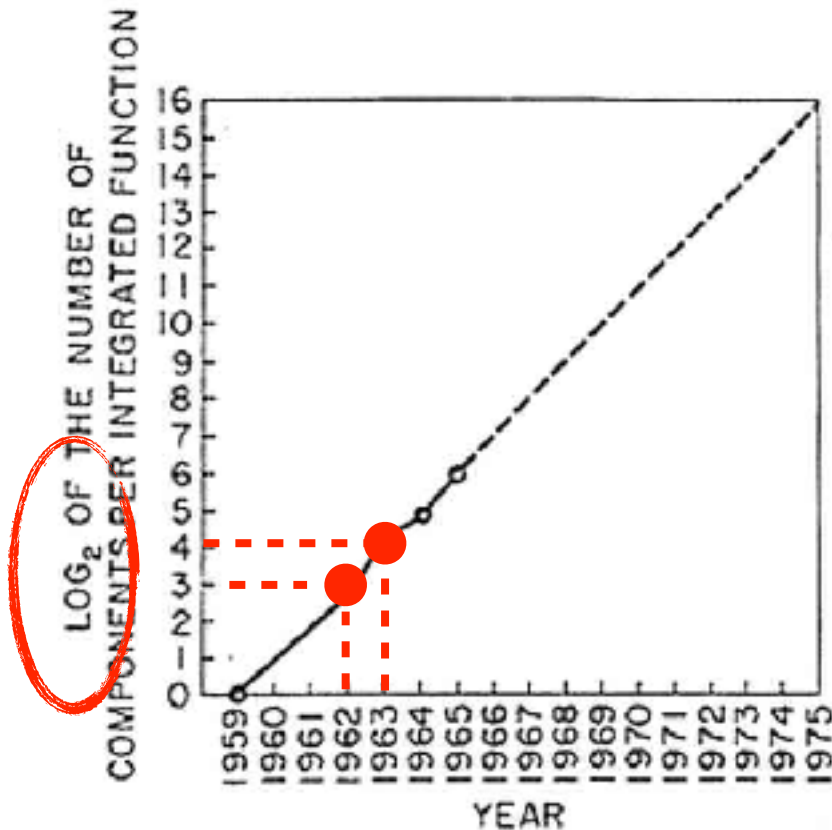
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- In 1975 he revised the prediction to doubling every 2 years
- Today's widely-known Moore's Law: number of transistors double about every 18 months
  - Moore never used the number 18...

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# Moore's Law



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TECH —

## Transistors will stop shrinking in 2021, but Moore's law will live on

Final semiconductor industry roadmap says the future is 3D packaging and cooling.

The first problem has been known about for a long while. Basically, starting at around the 65nm node in 2006, the economic gains from moving to smaller transistors have been slowly dribbling away. Previously, moving to a smaller node meant you could cram tons more chips onto a single silicon wafer, at a reasonably small price increase. With recent nodes like 22 or 14nm, though, there are so many additional steps required that it costs a lot more to manufacture a completed wafer—not to mention additional costs for things like package-on-package (PoP) and through-silicon vias (TSV) packaging.



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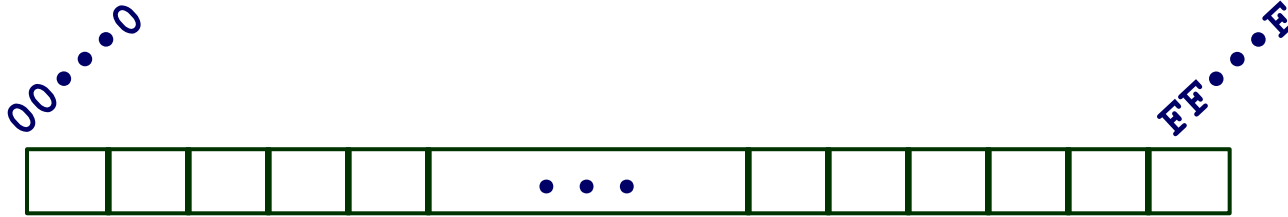
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# Today: Assembly Programming I: Basics

- Different ISAs and history behind them
- Memory, C, assembly, machine code
- Move operations (and addressing modes)

# Byte-Oriented Memory Organization



- Data in computers are stored in “memory”
  - Conceptually, envision it as a very large array of bytes: **byte-addressable**
- Each byte has an address
  - An address is like an index into that array
  - A pointer variable is a variable that stores an address

# How Does Pointer Work in C???

```
char a = 4;
```

```
char b = 3;
```

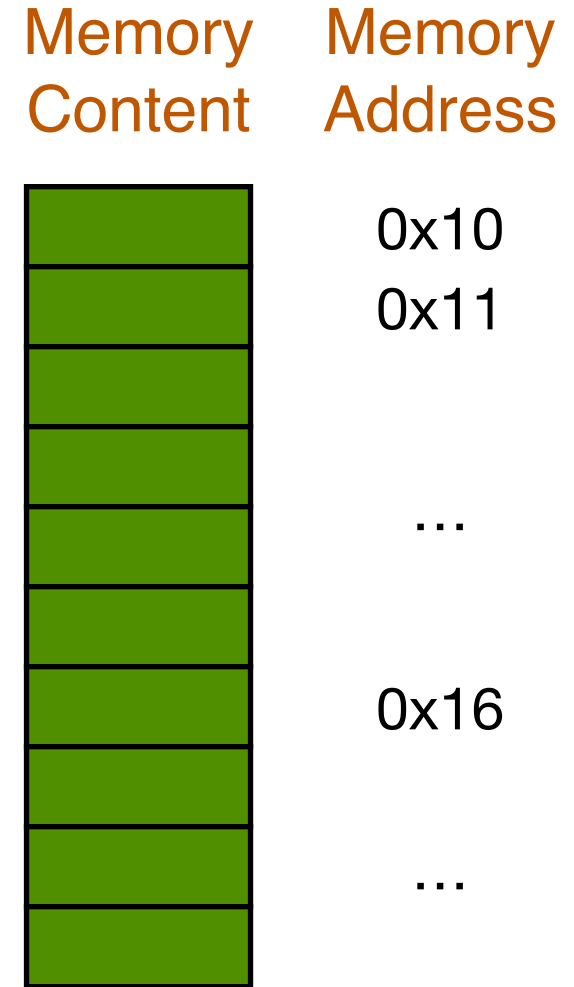
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char* c;
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c = &a;
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b += (*c);
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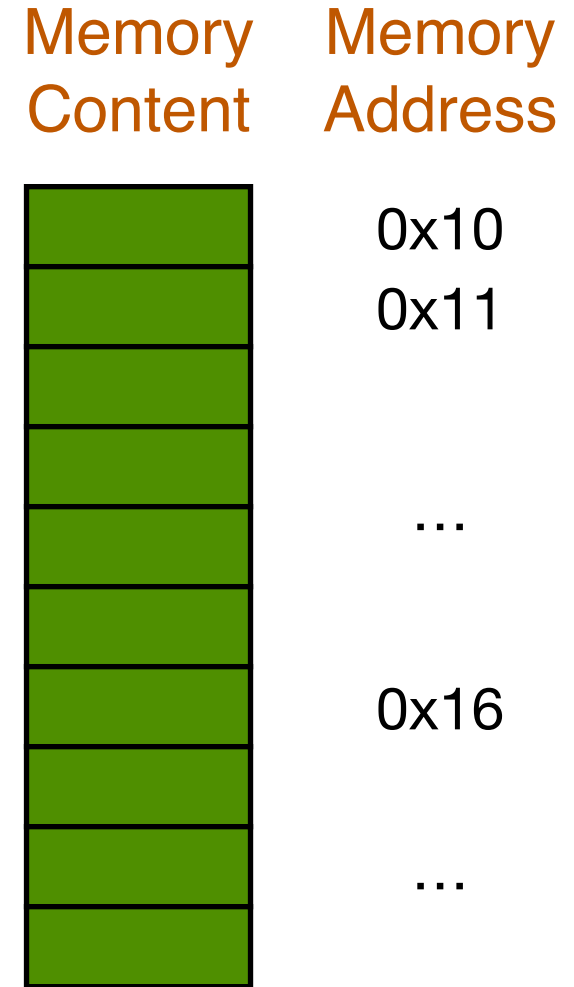
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C Variable	Memory Content	Memory Address
a	4	0x10
		0x11
		...
		0x16
		...

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		0x16
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c	random	0x16
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```
→ c = &a;
```

```
b += (*c);
```

- The content of a pointer variable is memory address.
- The '**&**' operator (address-of operator) returns the memory address of a variable.

C Variable	Memory Content	Memory Address
a	4	0x10
b	3	0x11
		...
c	random	0x16
		...



# How Does Pointer Work in C???

```
char a = 4;
```

```
char b = 3;
```

```
char* c;
```

```
→ c = &a;
```

```
b += (*c);
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C Variable	Memory Content	Memory Address
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		...

# How Does Pointer Work in C???

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```

```
char* c;
```

```
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```

→ 

```
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C Variable	Memory Content	Memory Address
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b	3	0x11
		...
c	0x10	0x16
		...

# How Does Pointer Work in C???

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char a = 4;
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```
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```

```
char* c;
```

```
c = &a;
```

→ 

```
b += (*c);
```

- The content of a pointer variable is memory address.
- The '**&**' operator (address-of operator) returns the memory address of a variable.
- The '**\***' operator returns the content stored at the memory location pointed by the pointer variable (dereferencing)

C Variable	Memory Content	Memory Address
a	4	0x10
b	3	0x11
		...
c	0x10	0x16
		...

# How Does Pointer Work in C???

```
char a = 4;
```

```
char b = 3;
```

```
char* c;
```

```
c = &a;
```

→ 

```
b += (*c);
```

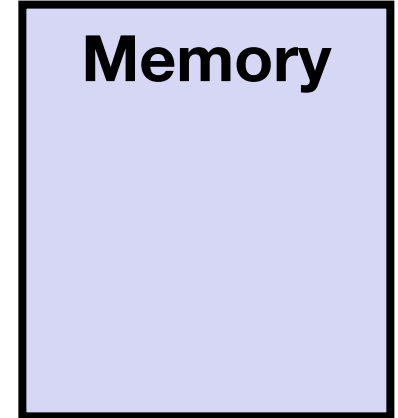
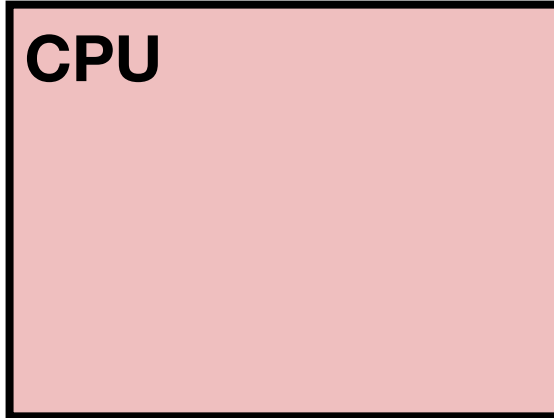
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C Variable	Memory Content	Memory Address
a	4	0x10
b	7	0x11
		...
c	0x10	0x16
		...

# Assembly Code's View of Computer: ISA

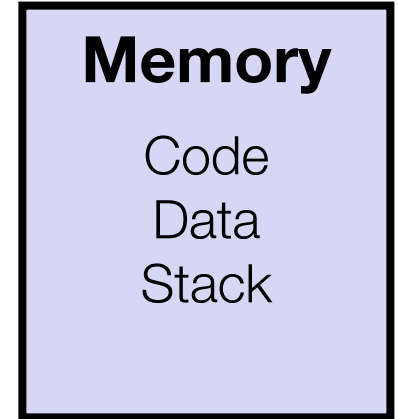
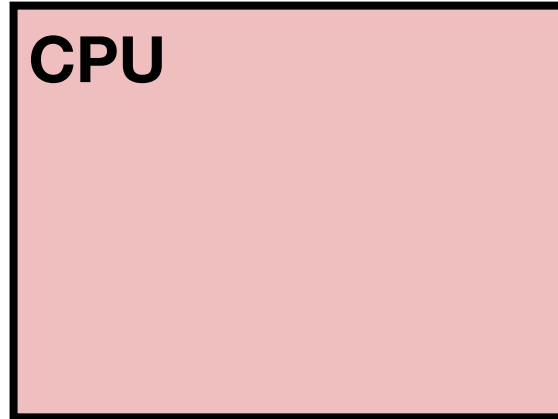
# Assembly Code's View of Computer: ISA

Assembly  
Programmer's  
Perspective  
of a Computer



# Assembly Code's View of Computer: ISA

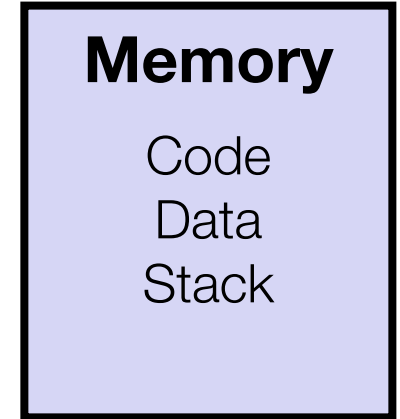
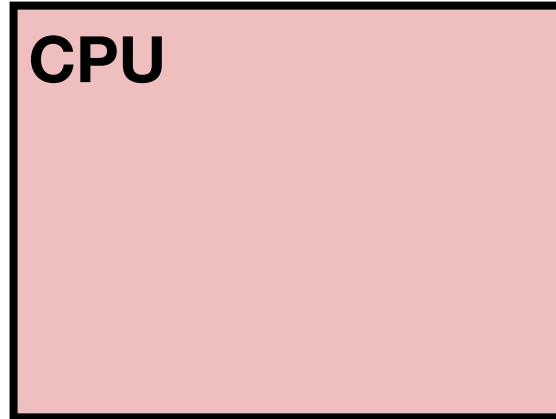
Assembly  
Programmer's  
Perspective  
of a Computer



- (Byte Addressable) Memory
  - Code: instructions
  - Data
  - Stack to support function call

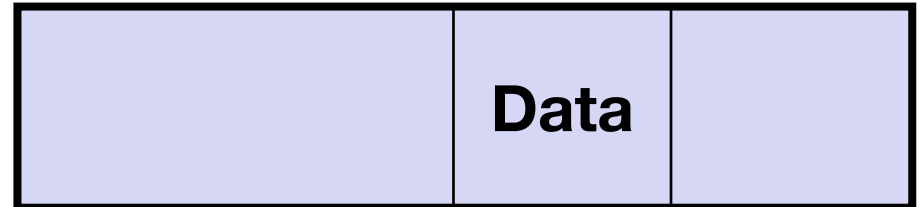
# Assembly Code's View of Computer: ISA

Assembly  
Programmer's  
Perspective  
of a Computer



- (Byte Addressable) Memory

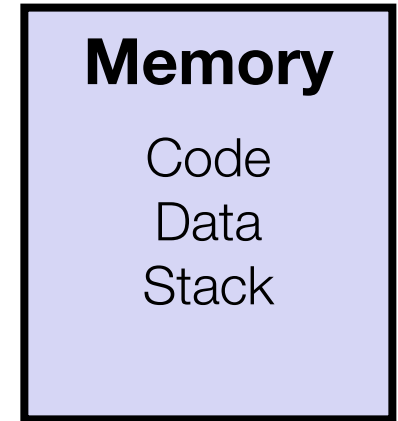
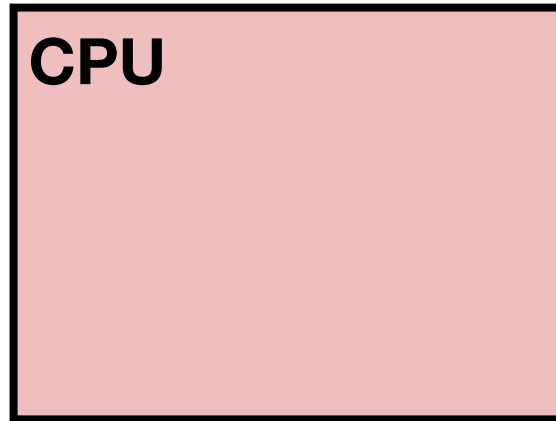
- Code: instructions
- Data
- Stack to support function call





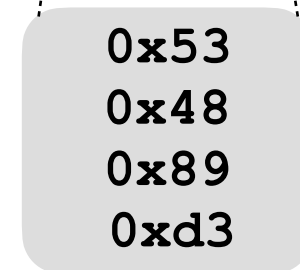
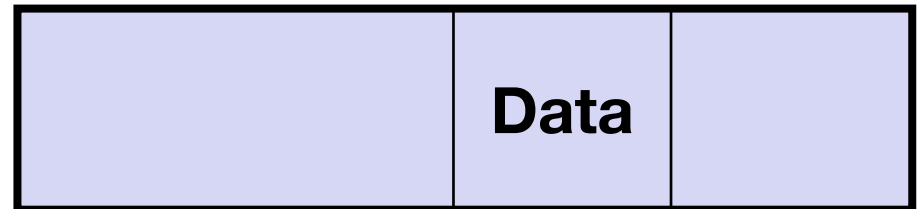
# Assembly Code's View of Computer: ISA

## Assembly Programmer's Perspective of a Computer



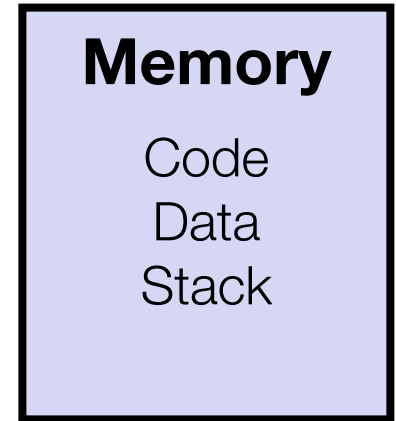
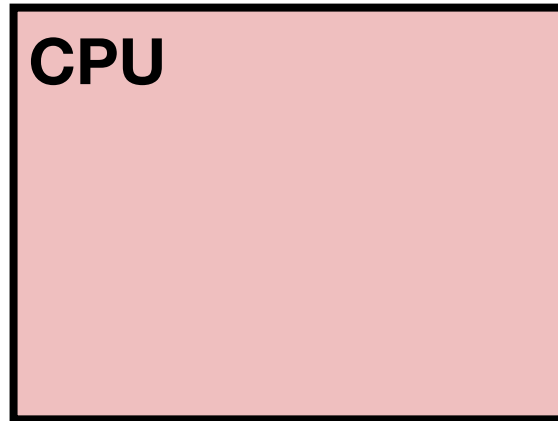
- (Byte Addressable) Memory

- Code: instructions
- Data
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# Assembly Code's View of Computer: ISA

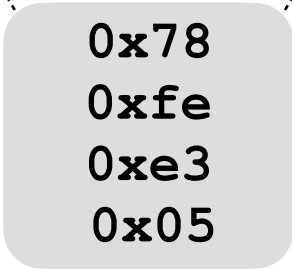
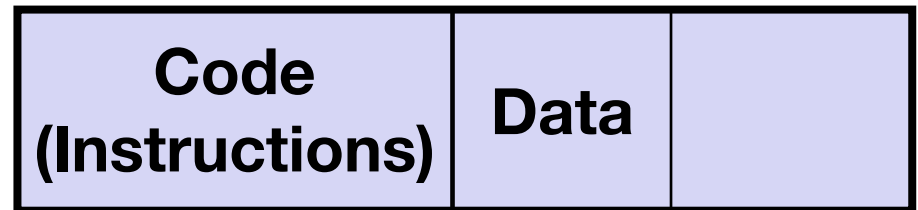
## Assembly Programmer's Perspective of a Computer



- (Byte Addressable) Memory

- Code: instructions
- Data
- Stack to support function call

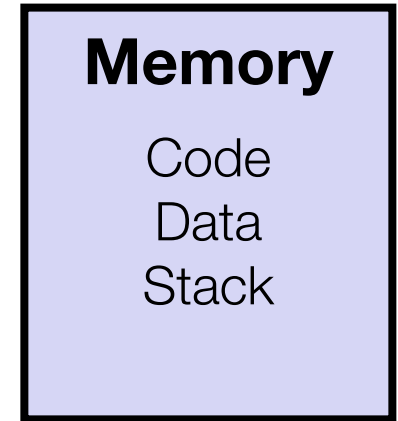
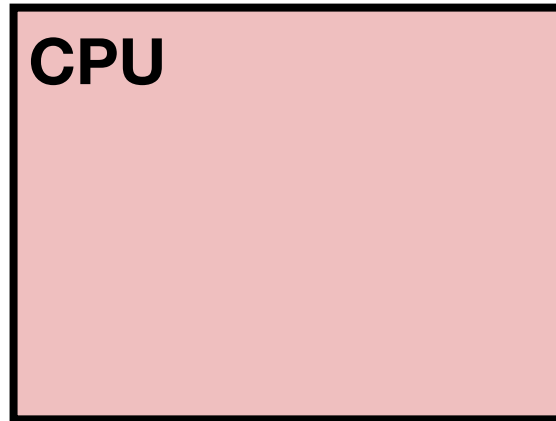
Instruction is the fundamental unit of work.  
All instructions are encoded as bits (just like data!)



A light gray rounded rectangle containing four lines of hexadecimal text: **0x78**, **0xfe**, **0xe3**, and **0x05**. Dotted lines connect the top-left and bottom-right corners of this rectangle to the corners of the 'Code (Instructions)' section in the diagram above.

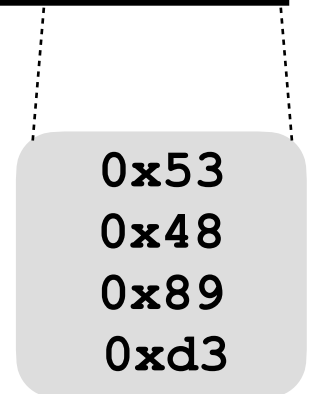
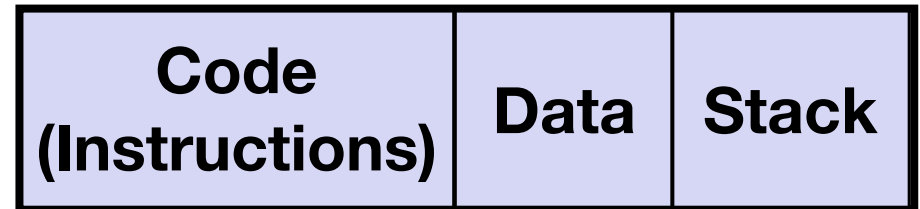
# Assembly Code's View of Computer: ISA

Assembly  
Programmer's  
Perspective  
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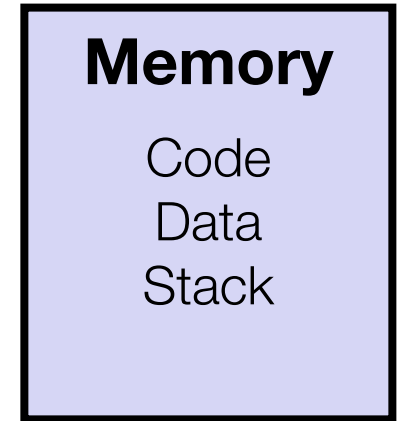
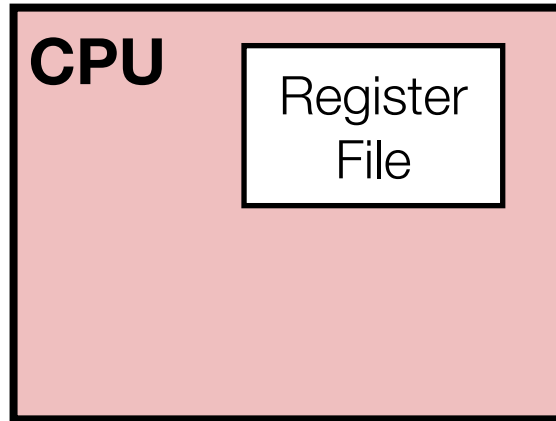
- (Byte Addressable) Memory

- Code: instructions
- Data
- Stack to support function call



# Assembly Code's View of Computer: ISA

## Assembly Programmer's Perspective of a Computer



- (Byte Addressable) Memory
  - Code: instructions
  - Data
  - Stack to support function call
- Register file
  - Faster memory (e.g., 0.5 ns vs. 15 ns)
  - Small memory (e.g., 128 B vs. 16 GB)
  - Heavily used program data

# x86-64 Integer Register File

← 8 Bytes →

**%rax**

**%rbx**

**%rcx**

**%rdx**

**%rsi**

**%rdi**

**%rsp**

**%rbp**

**%r8**

**%r9**

**%r10**

**%r11**

**%r12**

**%r13**

**%r14**

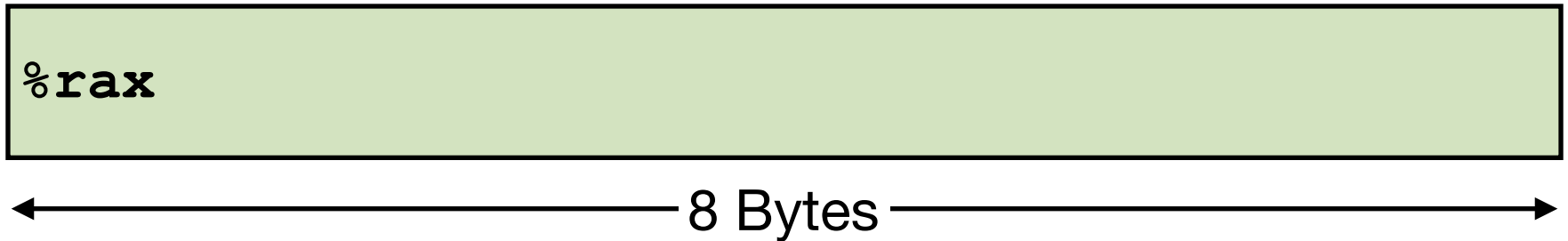
**%r15**

# x86-64 Integer Register File

- Lower-half of each register can be independently addressed (until 1 bytes)

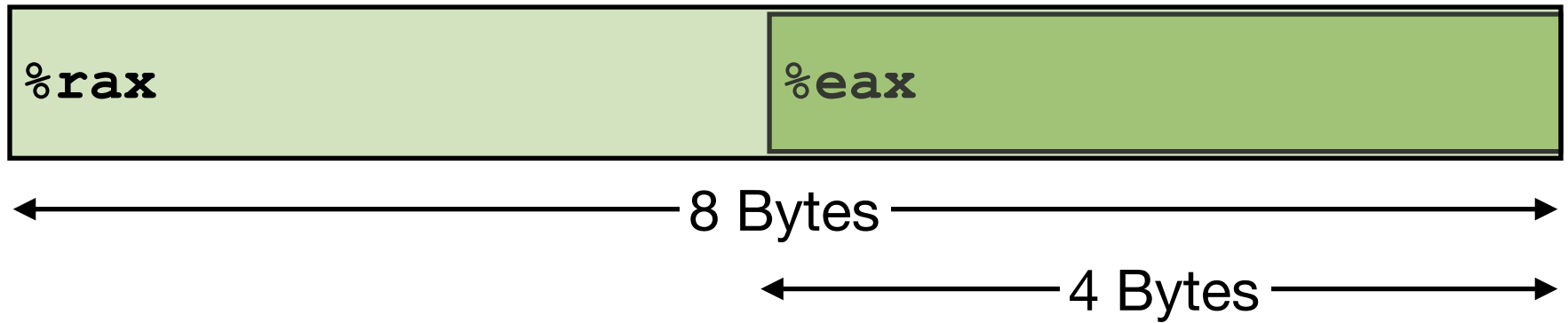
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- Lower-half of each register can be independently addressed (until 1 bytes)



# x86-64 Integer Register File

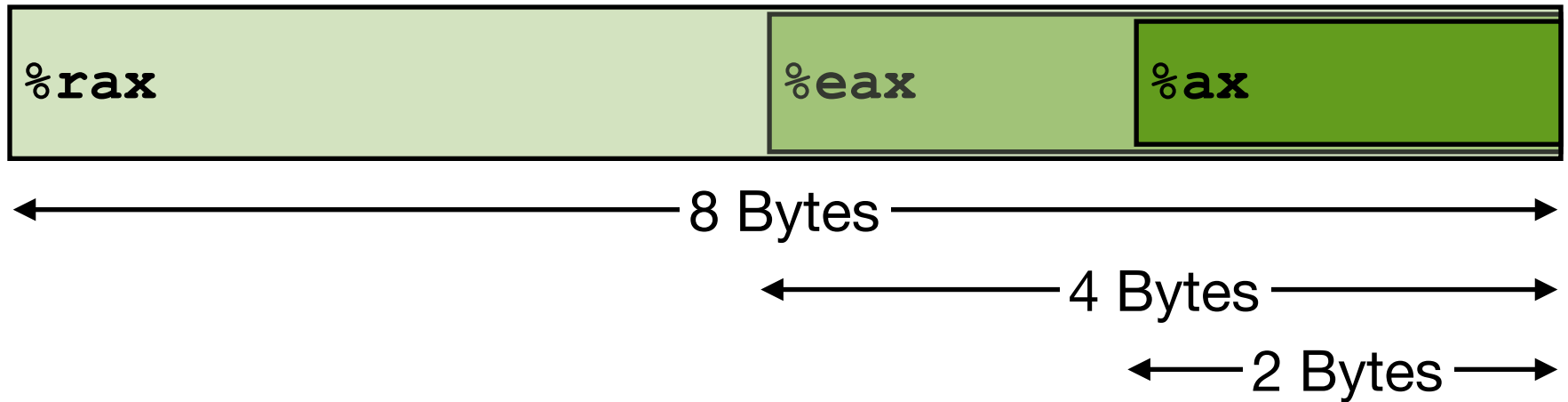
- Lower-half of each register can be independently addressed (until 1 bytes)





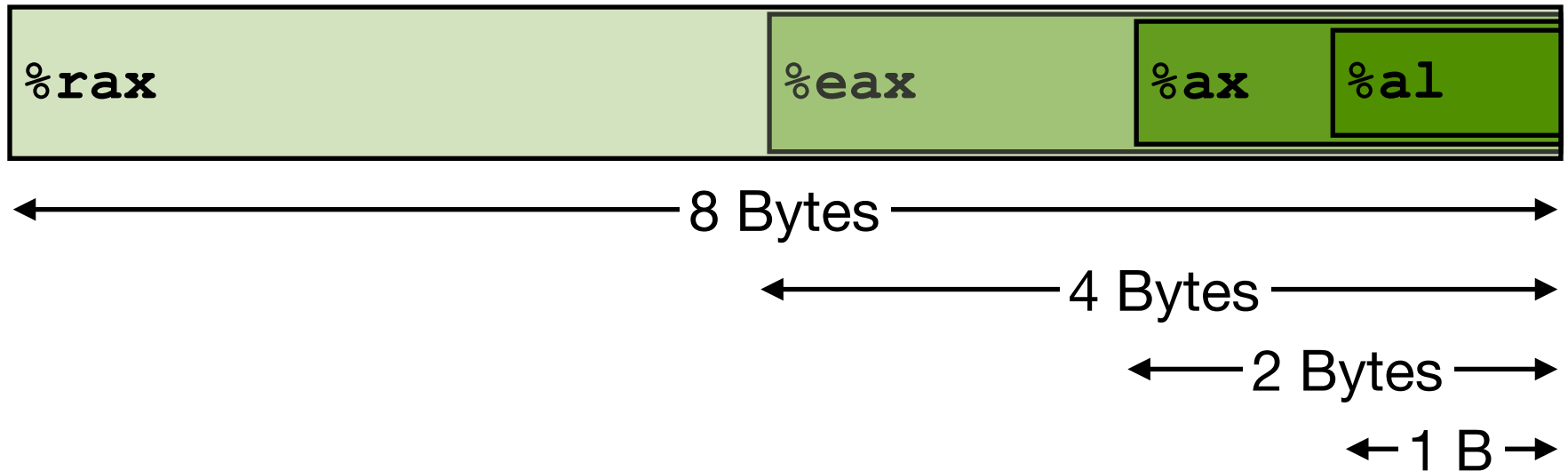
# x86-64 Integer Register File

- Lower-half of each register can be independently addressed (until 1 bytes)



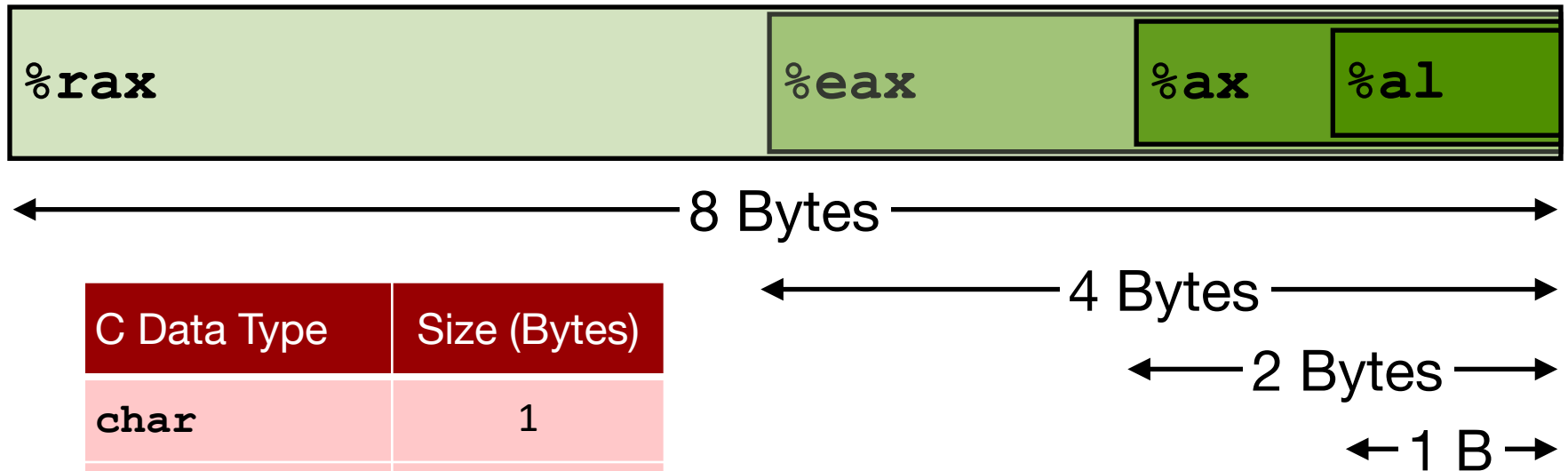
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# x86-64 Integer Register File

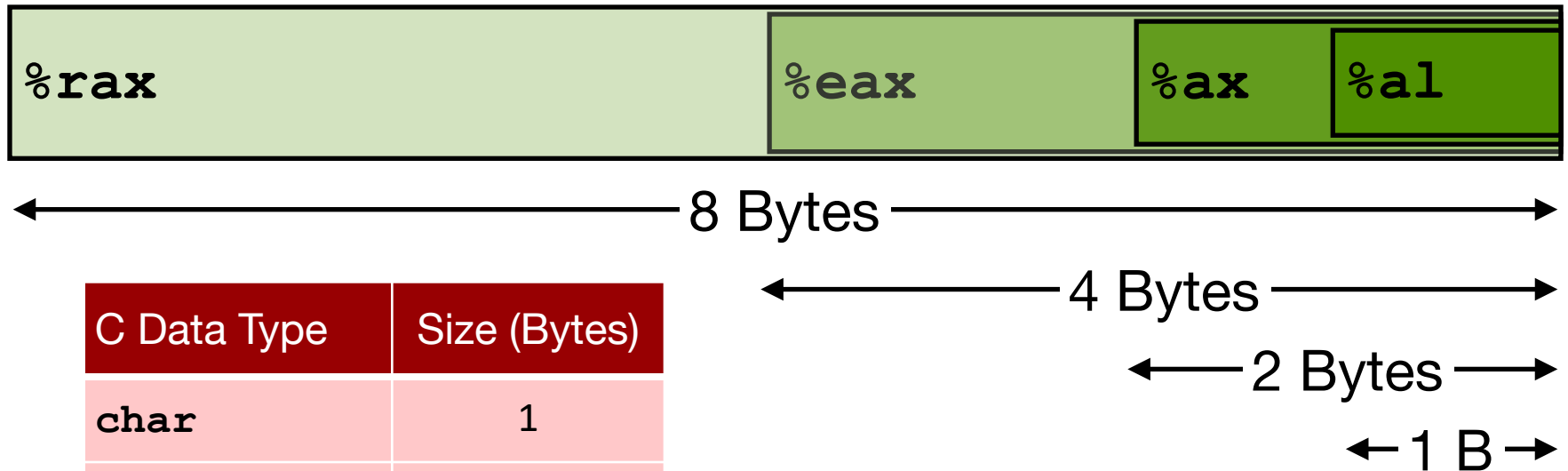
- Lower-half of each register can be independently addressed (until 1 bytes)



C Data Type	Size (Bytes)
<b>char</b>	1
<b>short</b>	2
<b>int</b>	4
<b>long</b>	8
<b>Pointer</b>	8

# x86-64 Integer Register File

- Lower-half of each register can be independently addressed (until 1 bytes)

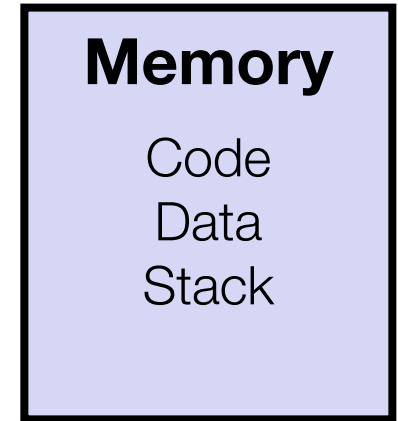
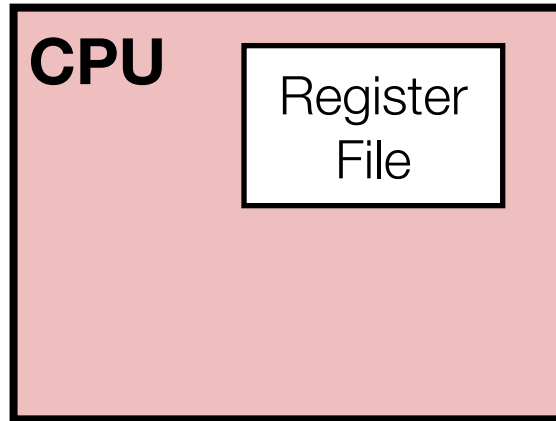


C Data Type	Size (Bytes)
char	1
short	2
int	4
long	8
Pointer	8

Floating point data is stored in a separate set of register file

# Assembly Code's View of Computer: ISA

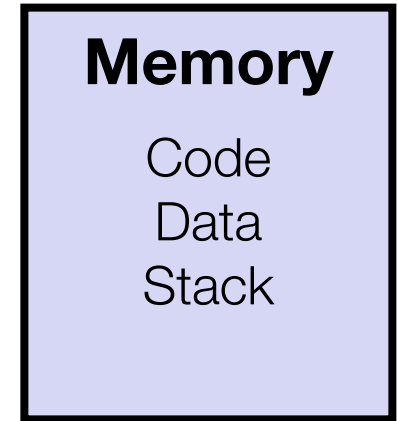
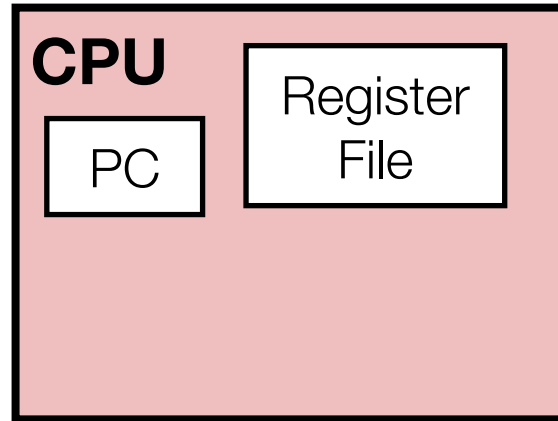
## Assembly Programmer's Perspective of a Computer



- (Byte Addressable) Memory
  - Code: instructions
  - Data
  - Stack to support function call
- Register file
  - Faster memory (e.g., 0.5 ns vs. 15 ns)
  - Small memory (e.g., 128 B vs. 16 GB)
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# Assembly Code's View of Computer: ISA

## Assembly Programmer's Perspective of a Computer



- (Byte Addressable) Memory

- Code: instructions
- Data
- Stack to support function call

- Register file

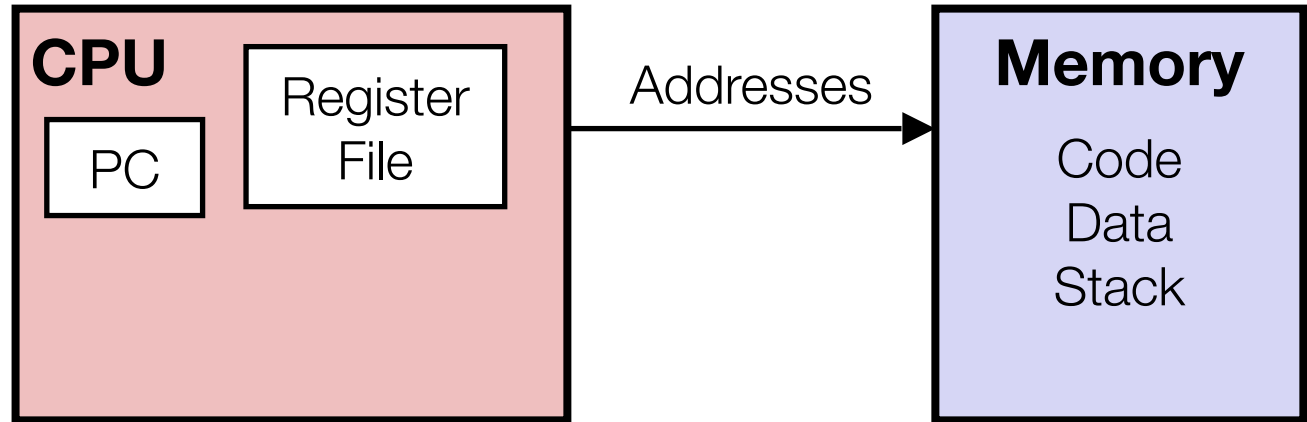
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- PC: Program counter

- A special register containing address of next instruction
- Called “RIP” in x86-64

# Assembly Code's View of Computer: ISA

## Assembly Programmer's Perspective of a Computer



- (Byte Addressable) Memory

- Code: instructions
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- Register file

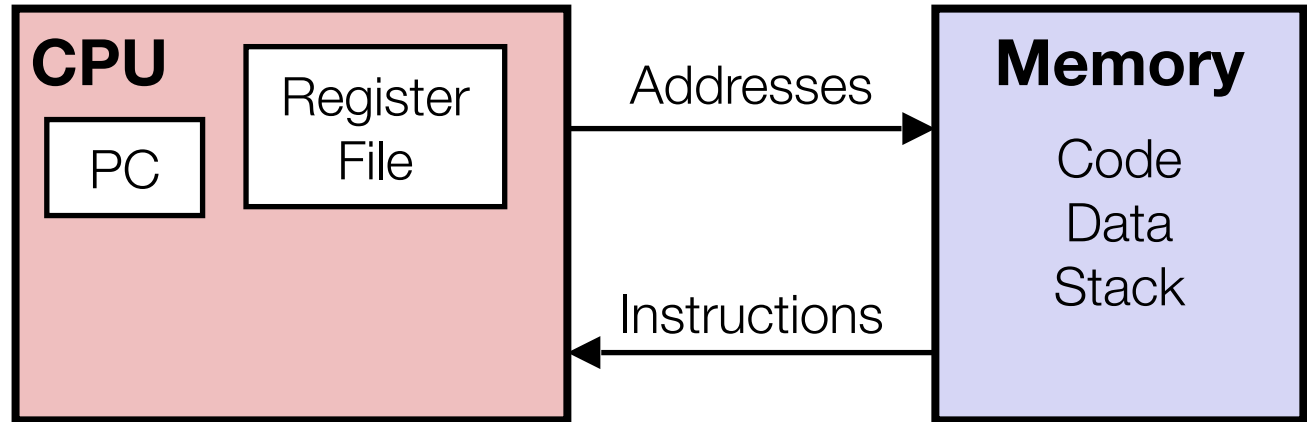
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# Assembly Code's View of Computer: ISA

## Assembly Programmer's Perspective of a Computer



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- Register file

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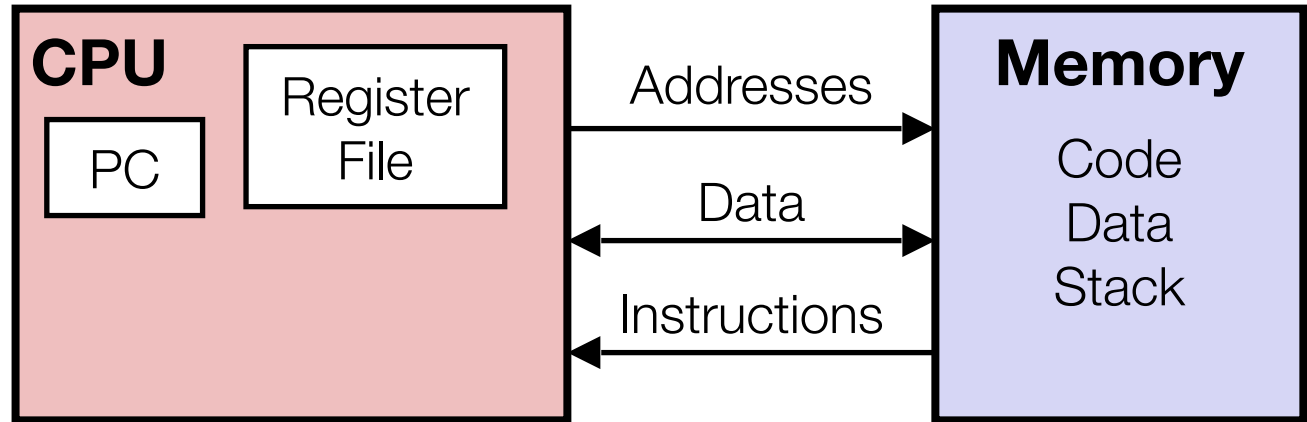
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# Assembly Code's View of Computer: ISA

## Assembly Programmer's Perspective of a Computer



- (Byte Addressable) Memory

- Code: instructions
- Data
- Stack to support function call

- Register file

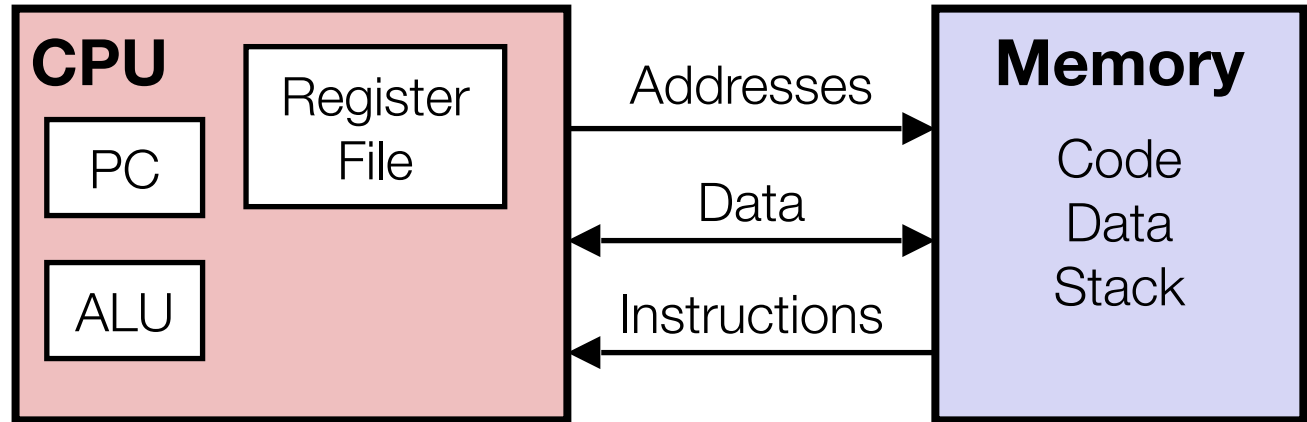
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# Assembly Code's View of Computer: ISA

## Assembly Programmer's Perspective of a Computer



- (Byte Addressable) Memory

- Code: instructions
- Data
- Stack to support function call

- Register file

- Faster memory (e.g., 0.5 ns vs. 15 ns)
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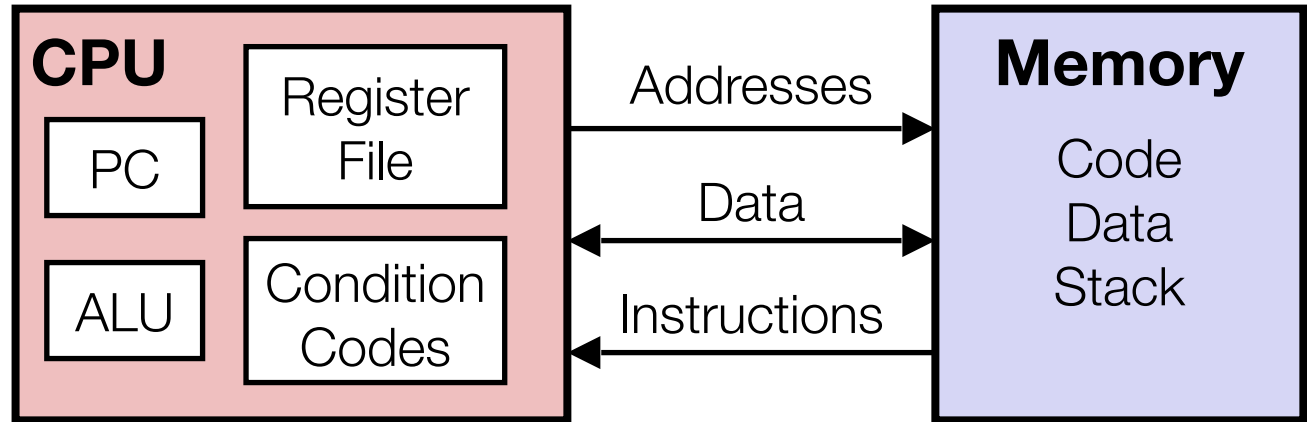
- A special register containing address of next instruction
- Called “RIP” in x86-64

- Arithmetic logic unit (ALU)

- Where computation happens

# Assembly Code's View of Computer: ISA

## Assembly Programmer's Perspective of a Computer



- (Byte Addressable) Memory

- Code: instructions
- Data
- Stack to support function call

- Register file

- Faster memory (e.g., 0.5 ns vs. 15 ns)
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- A special register containing address of next instruction
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- Arithmetic logic unit (ALU)

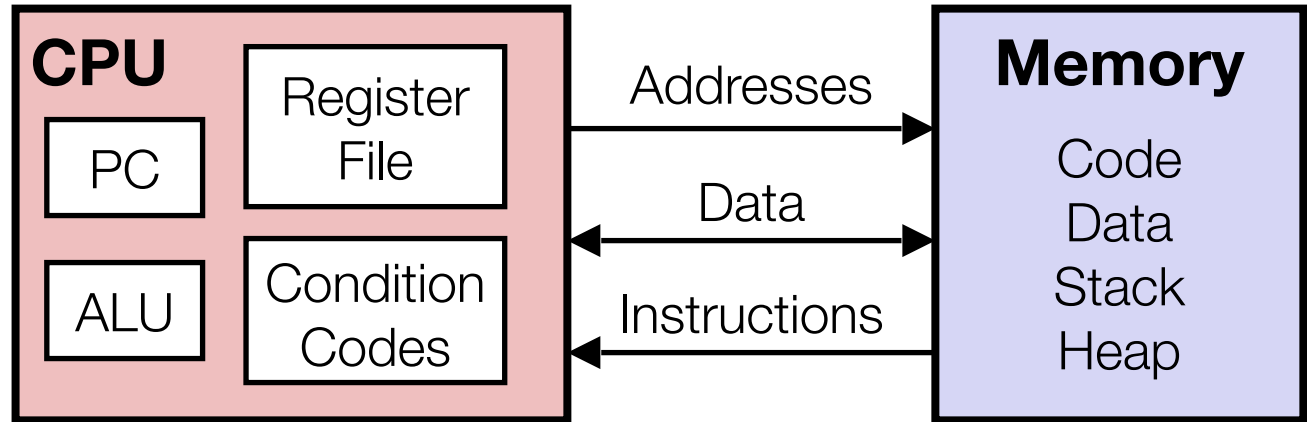
- Where computation happens

- Condition codes

- Store status information about most recent arithmetic or logical operation
- Used for conditional branch

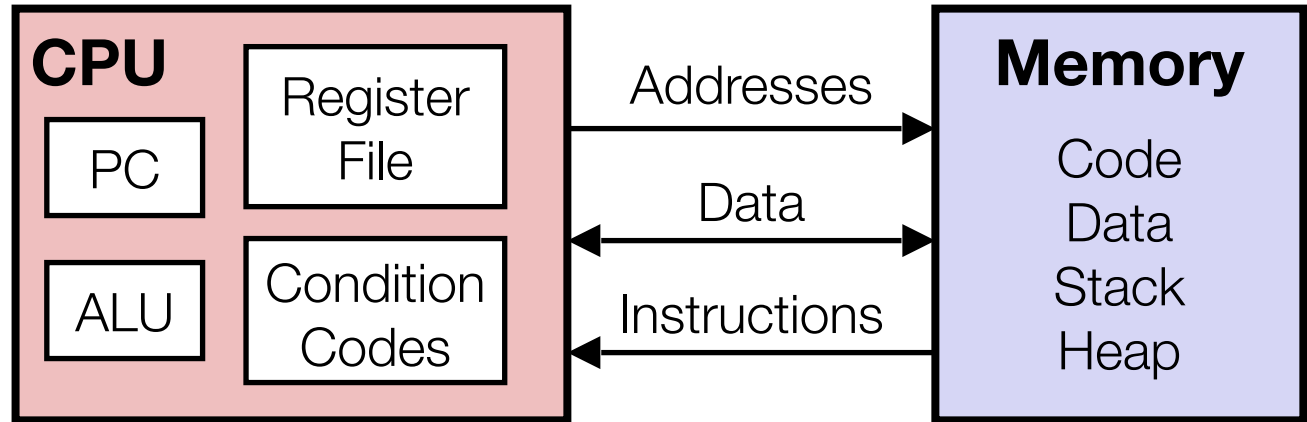
# Assembly Program Instructions

Assembly  
Programmer's  
Perspective  
of a Computer



# Assembly Program Instructions

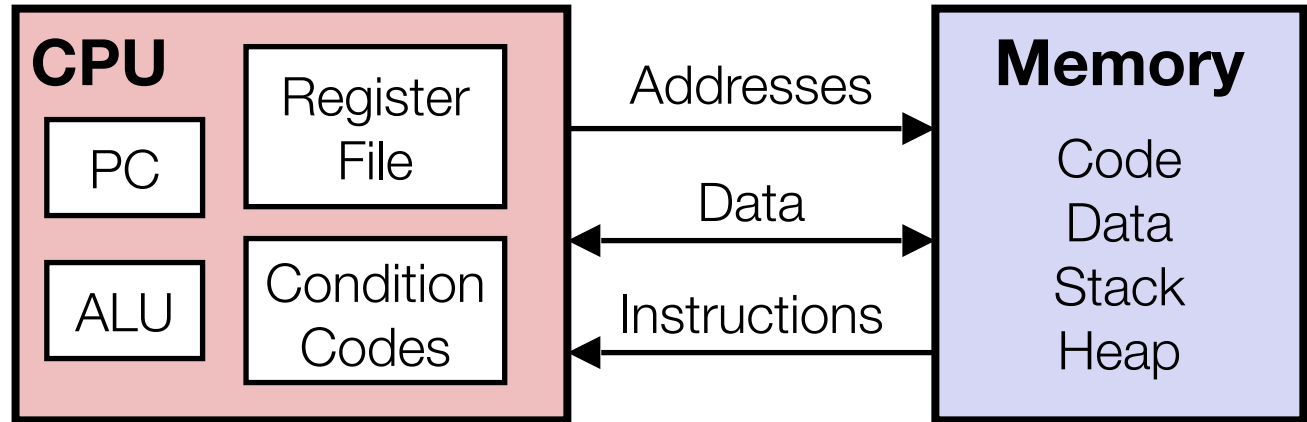
Assembly  
Programmer's  
Perspective  
of a Computer



- *Compute Instruction*: Perform arithmetics on register or memory data
  - **addq %eax, %ebx**
  - C constructs: +, -, >>, etc.

# Assembly Program Instructions

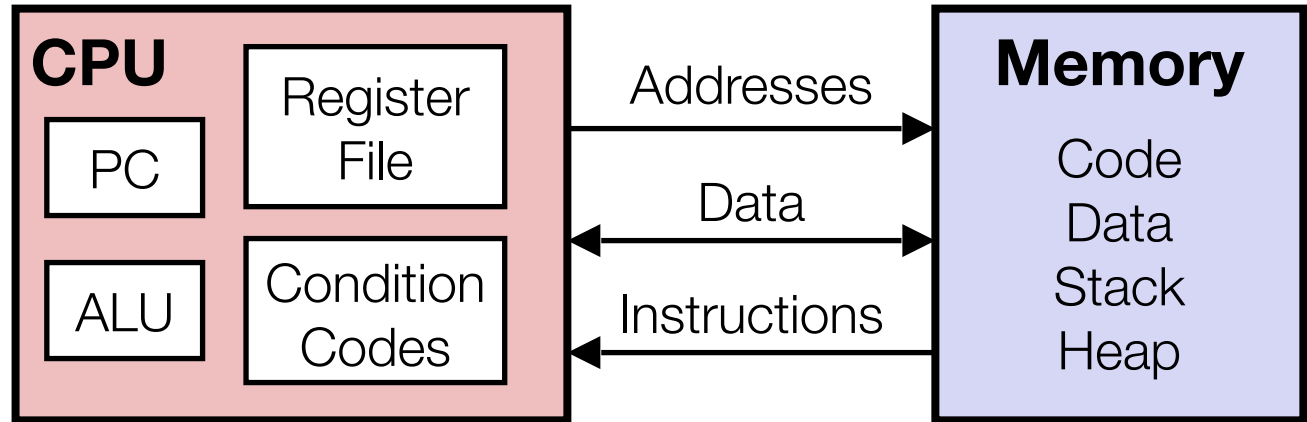
## Assembly Programmer's Perspective of a Computer



- *Compute Instruction*: Perform arithmetics on register or memory data
  - `addq %eax, %ebx`
  - C constructs: +, -, >>, etc.
- *Data Movement Instruction*: Transfer data between memory and register
  - `movq %eax, (%ebx)`

# Assembly Program Instructions

## Assembly Programmer's Perspective of a Computer



- *Compute Instruction*: Perform arithmetics on register or memory data
  - `addq %eax, %ebx`
  - C constructs: `+`, `-`, `>>`, etc.
- *Data Movement Instruction*: Transfer data between memory and register
  - `movq %eax, (%ebx)`
- *Control Instruction*: Alter the sequence of instructions (by changing PC)
  - `jmp, call`
  - C constructs: `if-else`, `do-while`, function call, etc.

# Turning C into Object Code

C Code (sum.c)

```
long plus(long x, long y);  
  
void sumstore(long x, long y,  
              long *dest)  
{  
    long t = plus(x, y);  
    *dest = t;  
}
```



# Turning C into Object Code

C Code (sum.c)

```
long plus(long x, long y);  
  
void sumstore(long x, long y,  
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{  
    long t = plus(x, y);  
    *dest = t;  
}
```

Generated x86-64 Assembly

```
sumstore:  
    pushq    %rbx  
    movq     %rdx, %rbx  
    call     plus  
    movq     %rax, (%rbx)  
    popq     %rbx  
    ret
```

# Turning C into Object Code

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    call     plus  
    movq     %rax, (%rbx)  
    popq     %rbx  
    ret
```

Obtain (on CSUG machine) with command

```
gcc -Og -S sum.c -o sum.s
```

# Turning C into Object Code

Generated x86-64 Assembly

```
sumstore:  
    pushq    %rbx  
    movq     %rdx, %rbx  
    call     plus  
    movq     %rax, (%rbx)  
    popq     %rbx  
    ret
```

# Turning C into Object Code

Generated x86-64 Assembly

Binary Code for **sumstore**

```
sumstore:
    pushq    %rbx
    movq     %rdx, %rbx
    call     plus
    movq     %rax, (%rbx)
    popq     %rbx
    ret
```

Memory

```
0x53
0x48
0x89
0xd3
0xe8
0xf2
0xff
0xff
0xff
0x48
0x89
0x03
0x5b
0xc3
```

# Turning C into Object Code

Generated x86-64 Assembly

Binary Code for **sumstore**

```
sumstore:
    pushq    %rbx
    movq     %rdx, %rbx
    call     plus
    movq     %rax, (%rbx)
    popq     %rbx
    ret
```

Address	Memory
0x0400595	0x53
	0x48
	0x89
	0xd3
	0xe8
	0xf2
	0xff
	0xff
	0xff
	0x48
	0x89
	0x03
	0x5b
	0xc3

# Turning C into Object Code

Generated x86-64 Assembly

Binary Code for **sumstore**

```
sumstore:
    pushq    %rbx
    movq     %rdx, %rbx
    call     plus
    movq     %rax, (%rbx)
    popq     %rbx
    ret
```

Address      Memory

0x0400595

0x53  
0x48  
0x89  
0xd3  
0xe8  
0xf2  
0xff  
0xff  
0xff  
0x48  
0x89  
0x03  
0x5b  
0xc3

Obtain (on CSUG machine) with command

```
gcc -c sum.s -o sum.o
```

# Turning C into Object Code

Generated x86-64 Assembly

Binary Code for **sumstore**

```
sumstore:
    pushq    %rbx
    movq     %rdx, %rbx
    call     plus
    movq     %rax, (%rbx)
    popq     %rbx
    ret
```

Address      Memory

0x0400595

0x53  
0x48  
0x89  
0xd3  
0xe8  
0xf2  
0xff  
0xff  
0xff  
0x48  
0x89  
0x03  
0x5b  
0xc3

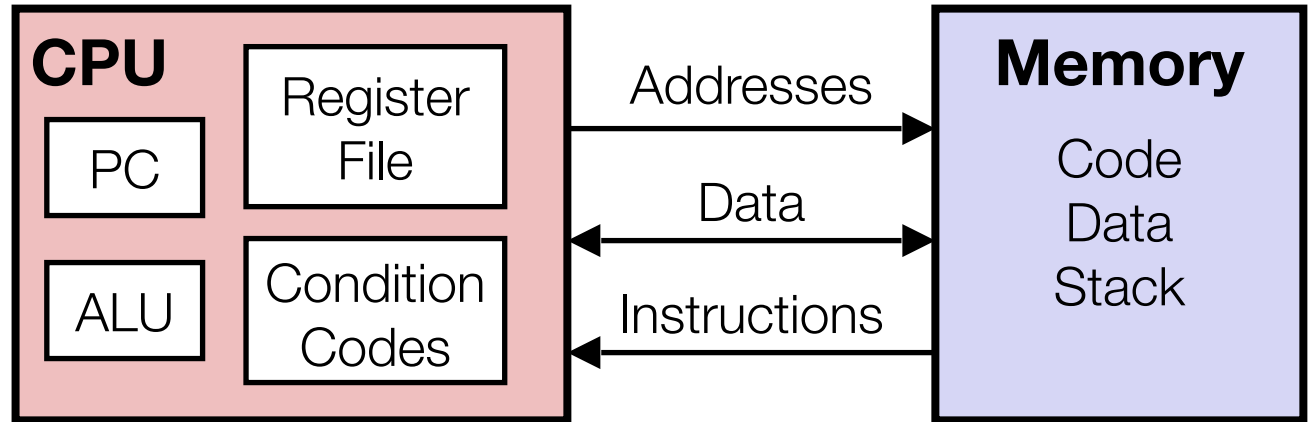
Obtain (on CSUG machine) with command

```
gcc -c sum.s -o sum.o
```

- Total of 14 bytes
- Instructions have variable lengths: e.g., 1, 3, or 5 bytes
- Code starts at memory address 0x0400595

# Instruction Processing Sequence

Assembly  
Programmer's  
Perspective  
of a Computer

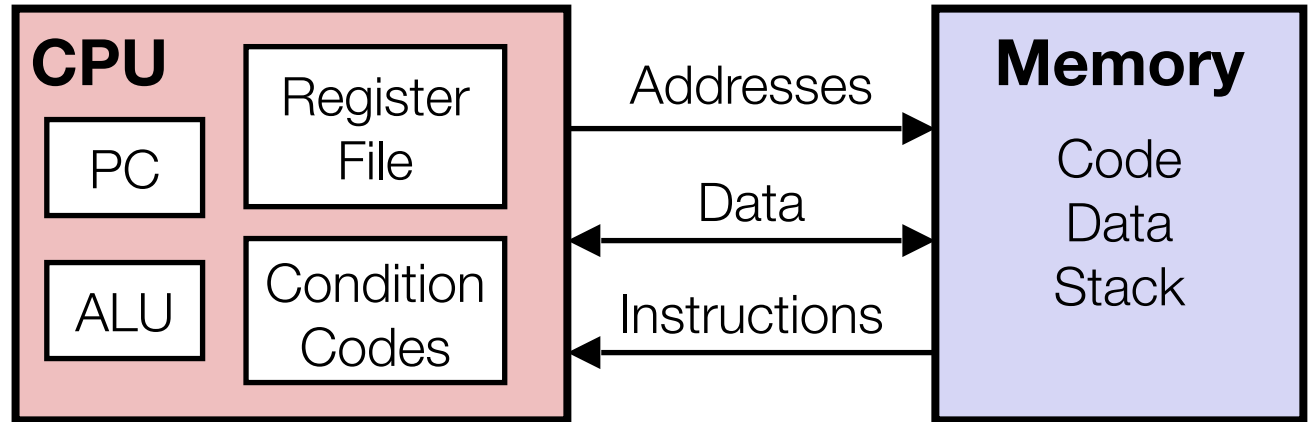


Fetch Instruction  
(According to PC)



# Instruction Processing Sequence

Assembly  
Programmer's  
Perspective  
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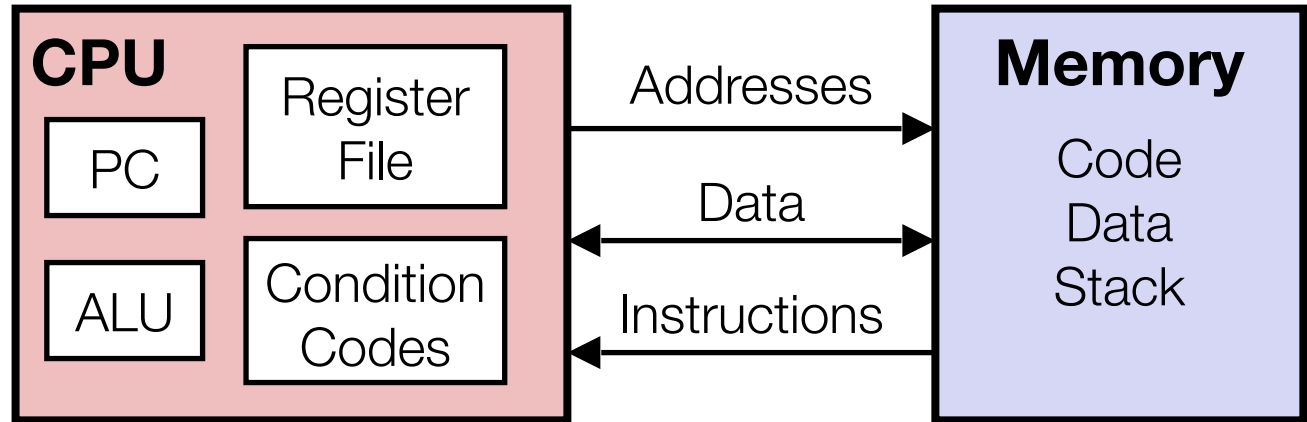


Fetch Instruction  
(According to PC)

**0x4801d8**

# Instruction Processing Sequence

Assembly  
Programmer's  
Perspective  
of a Computer

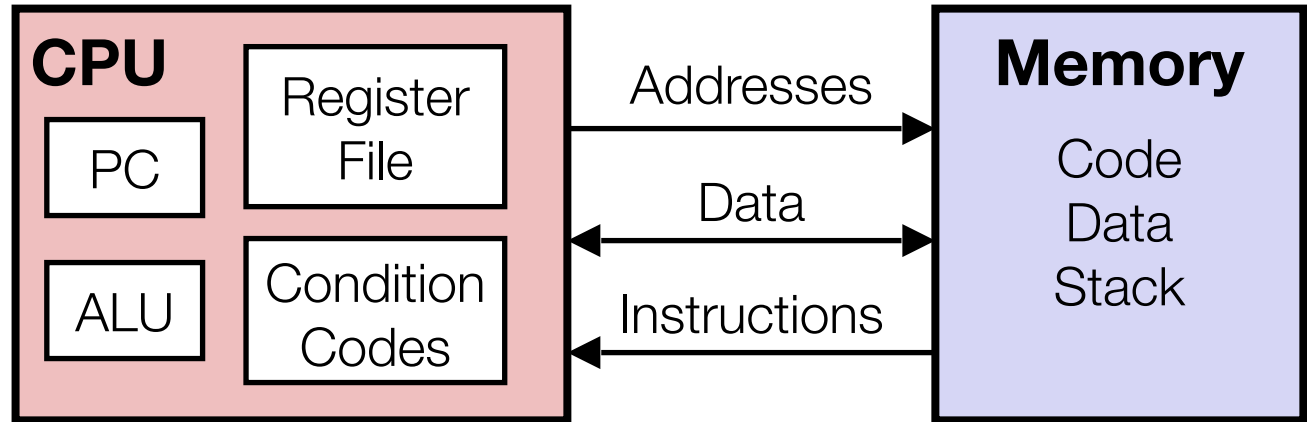


Fetch Instruction  
(According to PC) → Decode  
Instruction

**`addq %rax, (%rbx)`**

# Instruction Processing Sequence

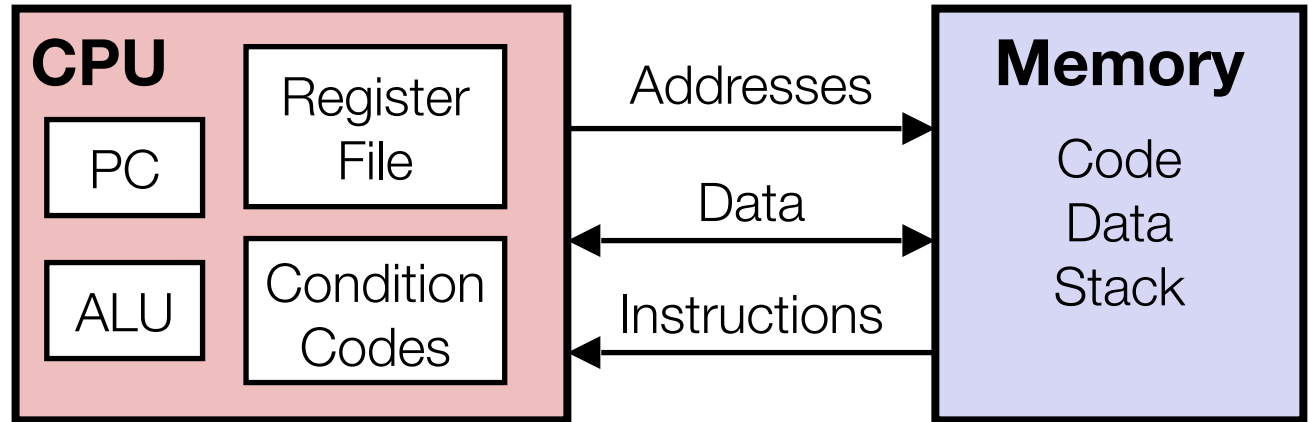
Assembly  
Programmer's  
Perspective  
of a Computer



Fetch Instruction (According to PC) → Decode Instruction → Fetch Operands

# Instruction Processing Sequence

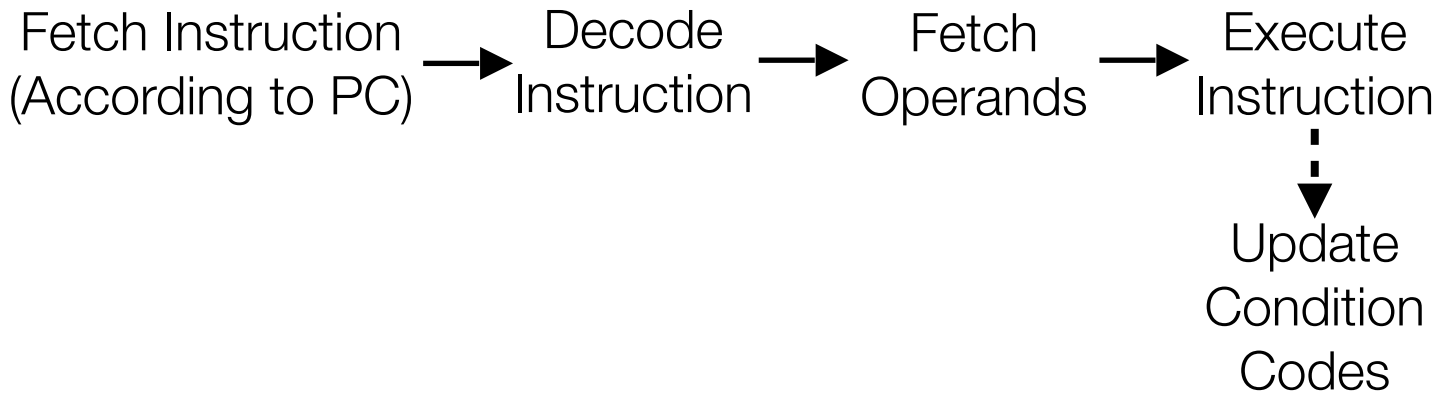
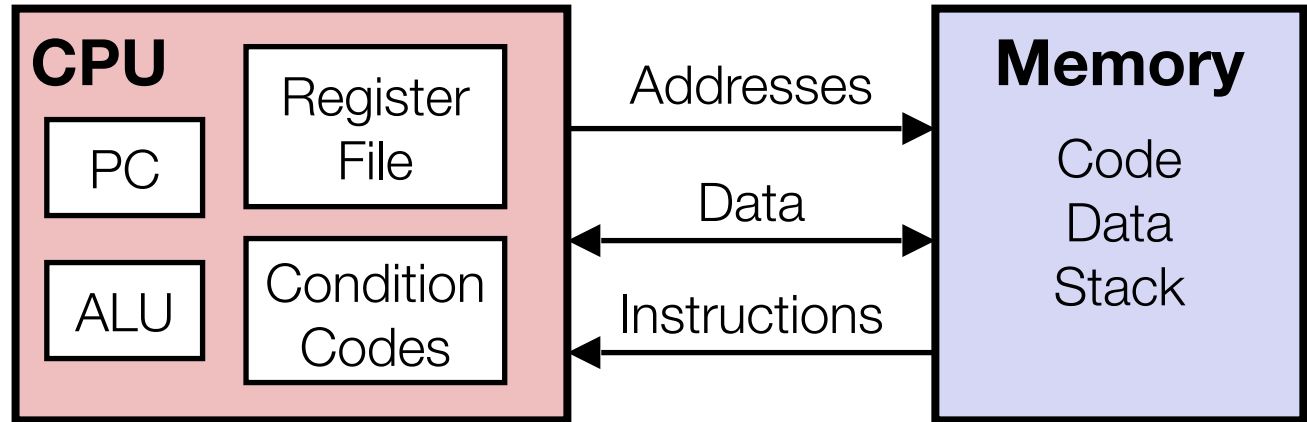
Assembly  
Programmer's  
Perspective  
of a Computer



Fetch Instruction (According to PC) → Decode Instruction → Fetch Operands → Execute Instruction

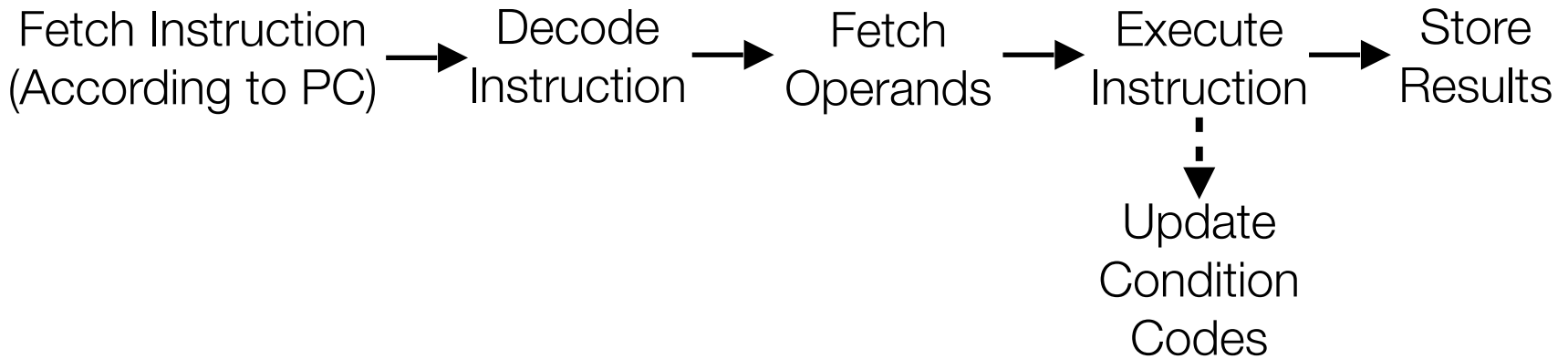
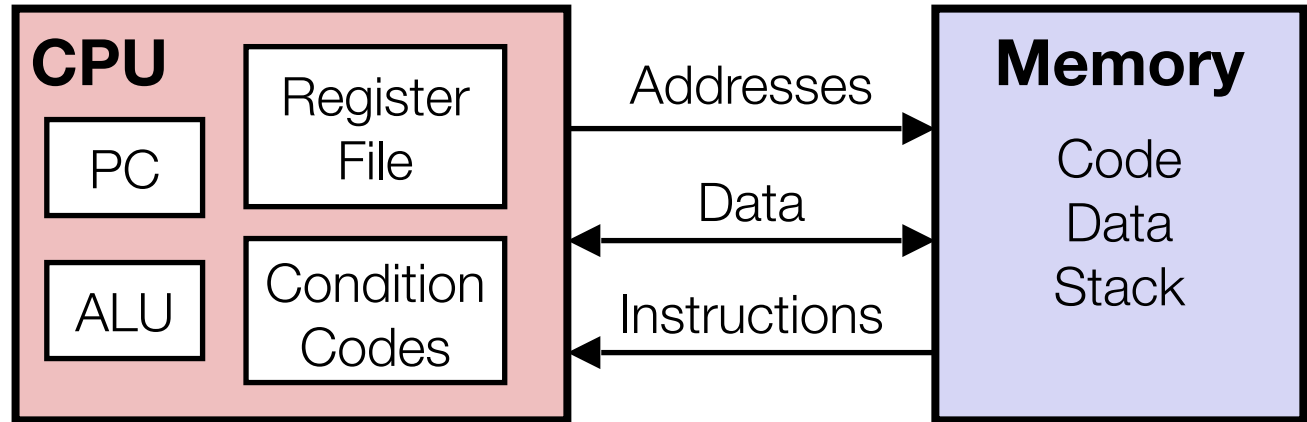
# Instruction Processing Sequence

Assembly  
Programmer's  
Perspective  
of a Computer



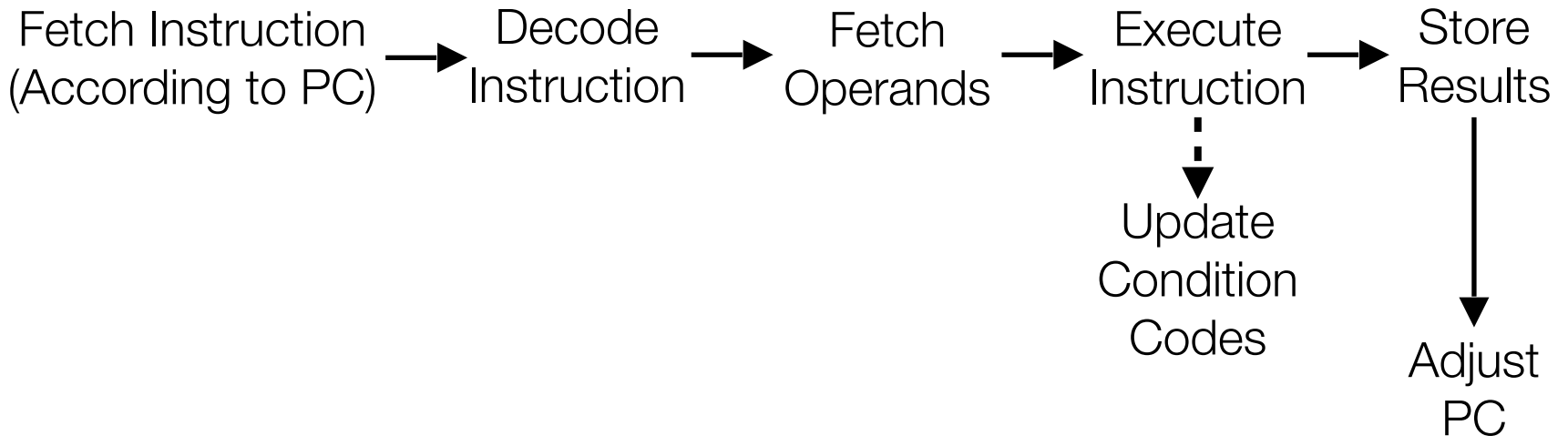
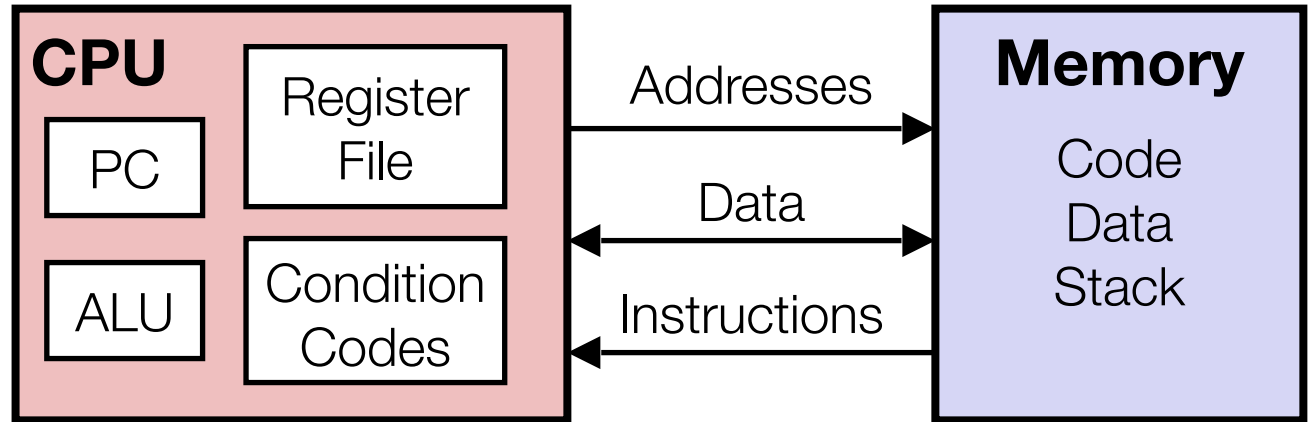
# Instruction Processing Sequence

Assembly  
Programmer's  
Perspective  
of a Computer



# Instruction Processing Sequence

Assembly  
Programmer's  
Perspective  
of a Computer



# Instruction Processing Sequence

Assembly  
Programmer's  
Perspective  
of a Computer

