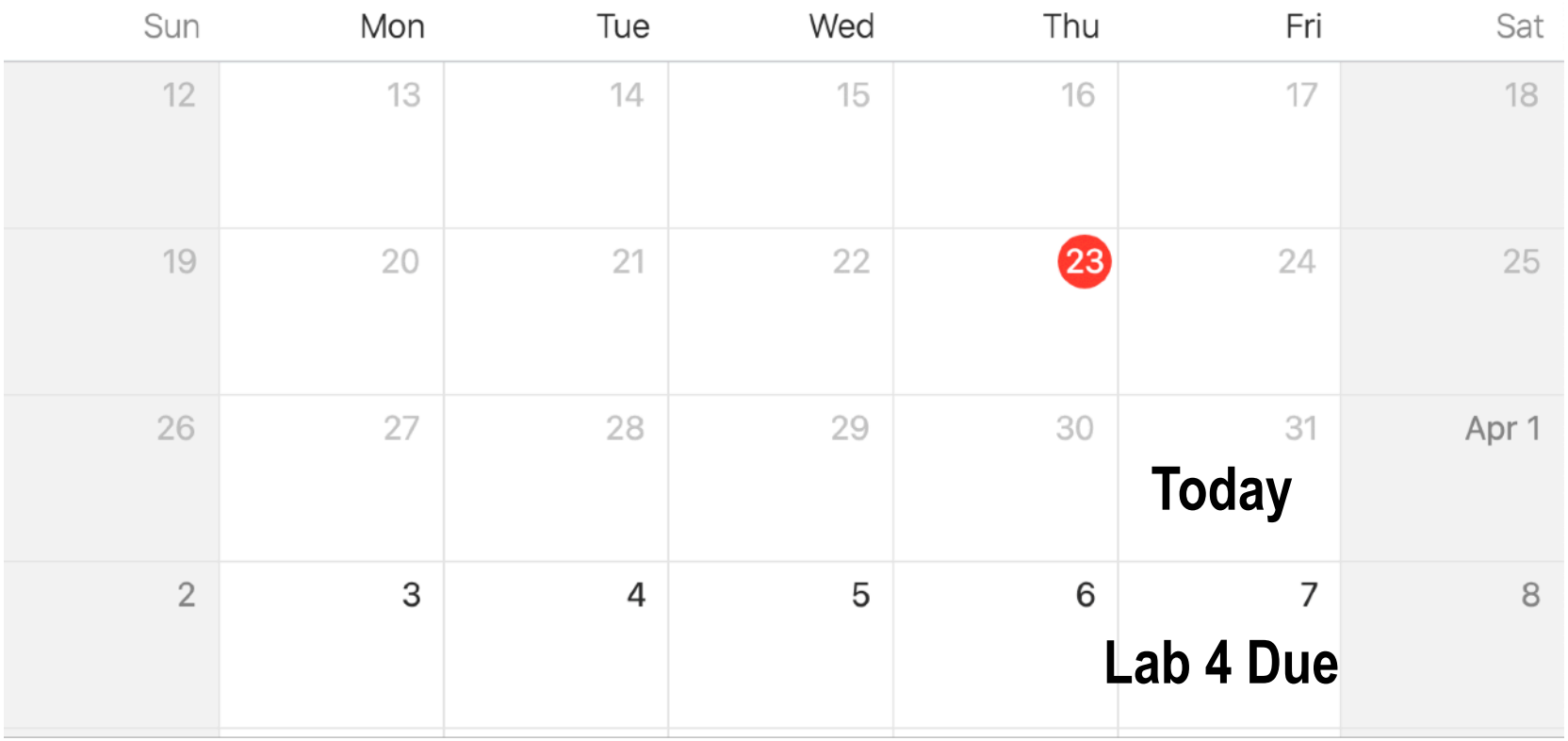
CSC 252: Computer Organization
Spring 2023: Lecture 21

Instructor: Yuhao Zhu

Department of Computer Science
University of Rochester

Announcements

- Cache problem set: https://www.cs.rochester.edu/courses/252/spring2023/handouts.html Won't be graded.
- Mid-term solution posted: https://www.cs.rochester.edu/courses/252/spring2023/handouts.html



Today

- VM basic concepts and operation
- Other critical benefits of VM
- Address translation

High Level Ideas

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  - Exploiting spatial locality: in what granularity are we moving data between physical memory and hard drive? One byte?
  - Exploiting temporal locality: replacement policy (e.g., LRU).

VM Concepts

- Divide the *virtual memory* to N contiguous *pages*.
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- Physical memory is also divided into pages. Each physical page (sometimes called *frames*) has the same size as a virtual page. Physical memory has way fewer pages.
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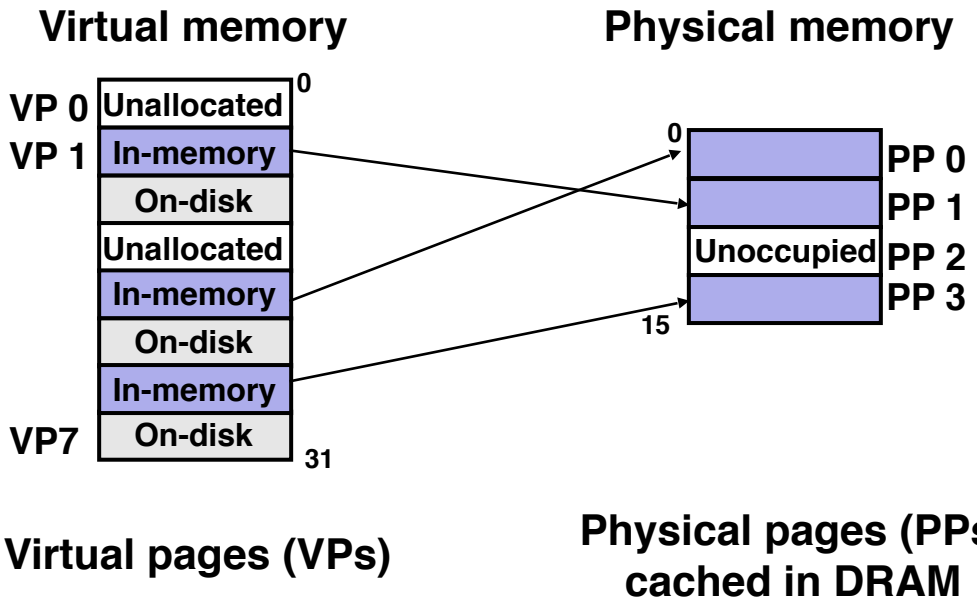

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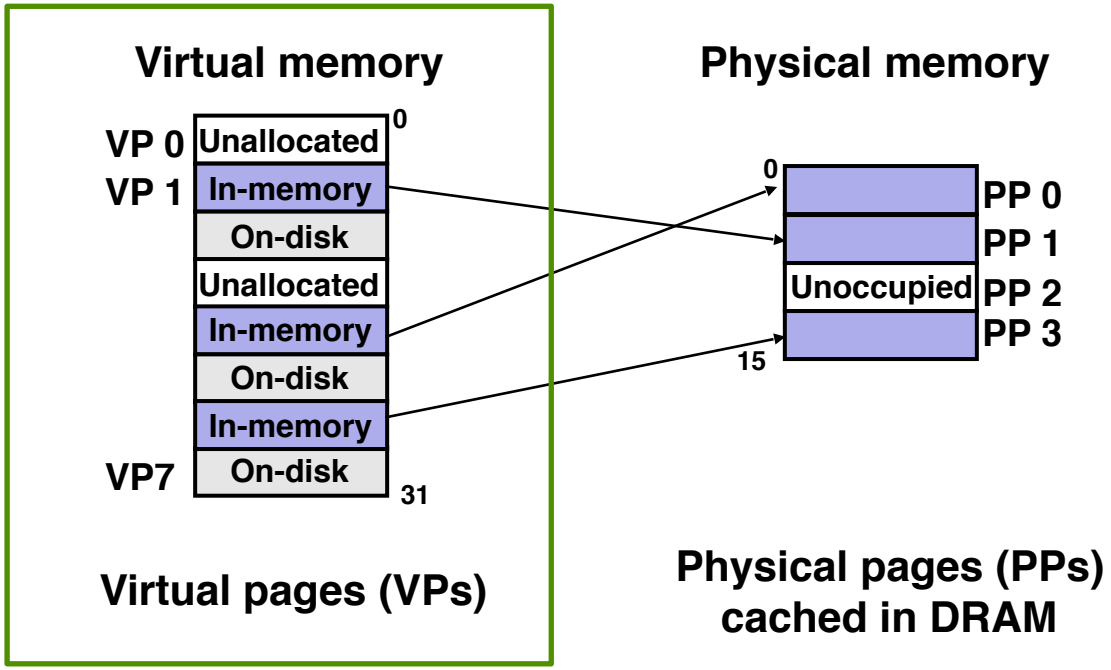

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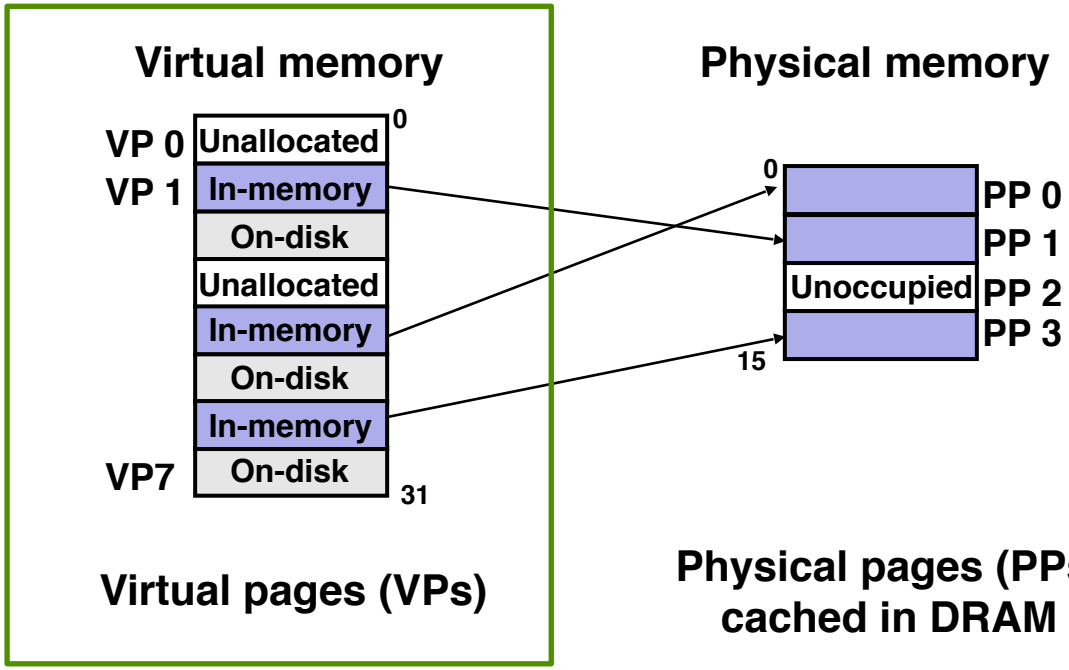

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Virtual memory size is 32B
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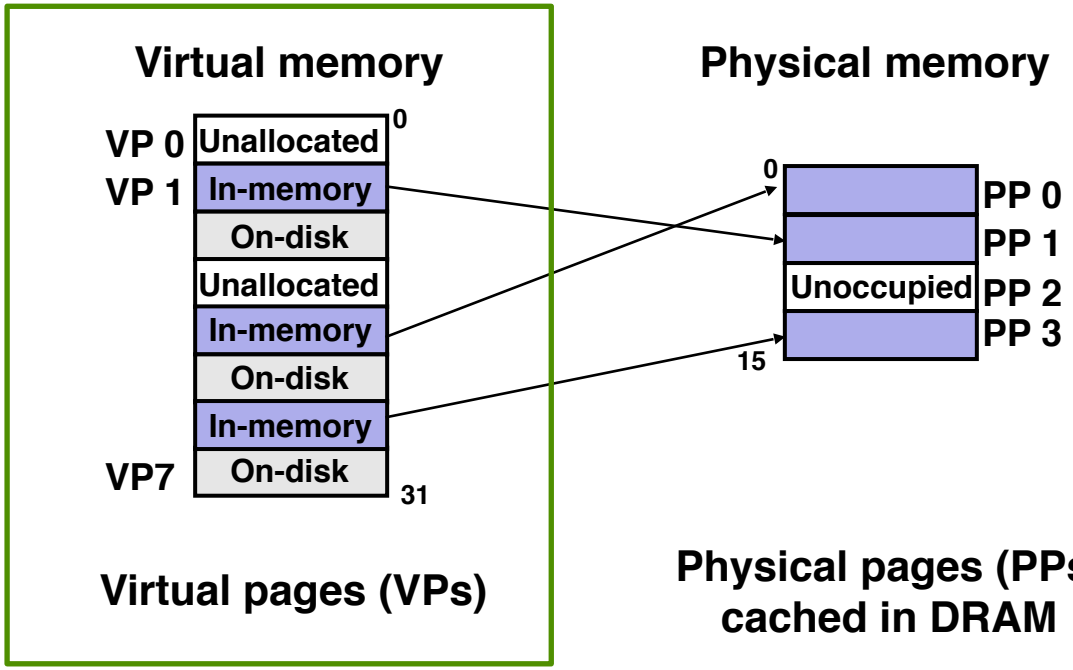

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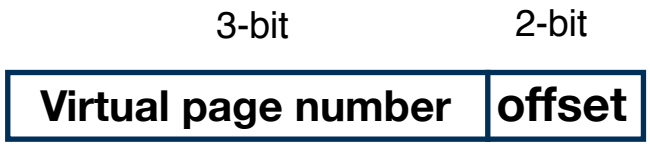

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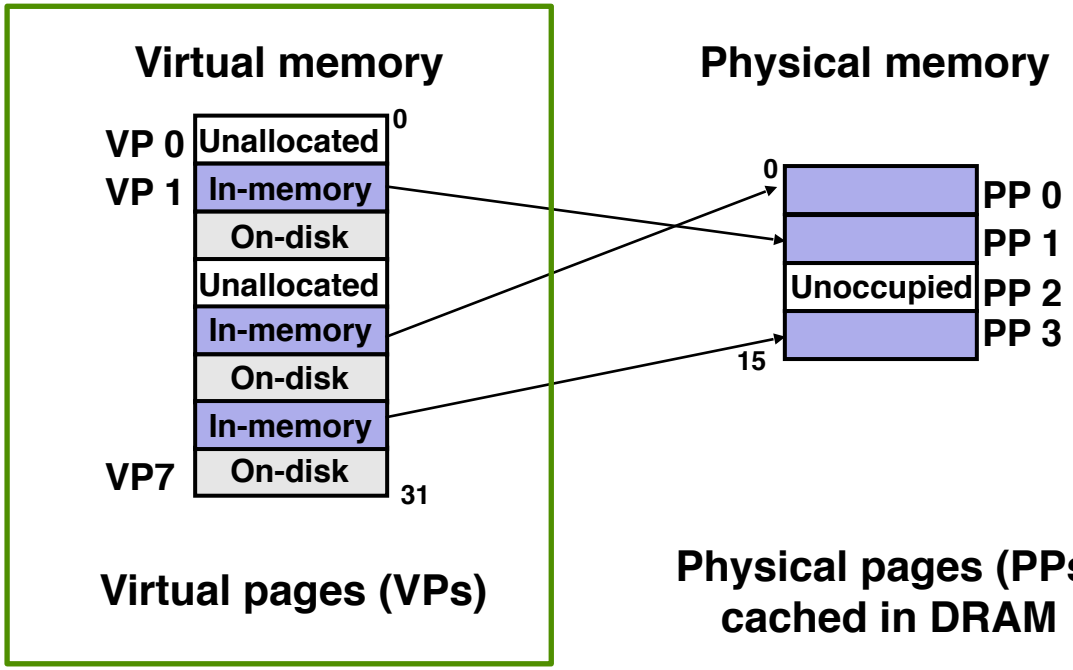

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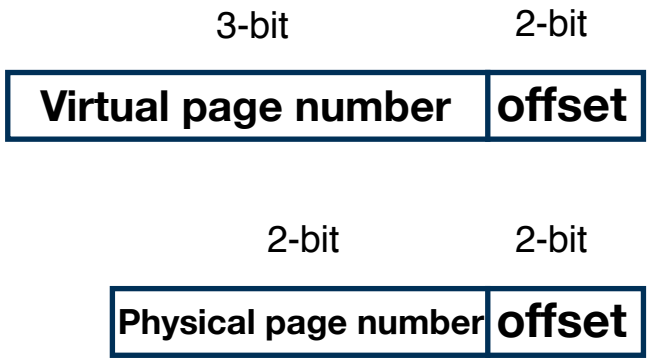

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  - Per-process data structure; managed by the OS kernel

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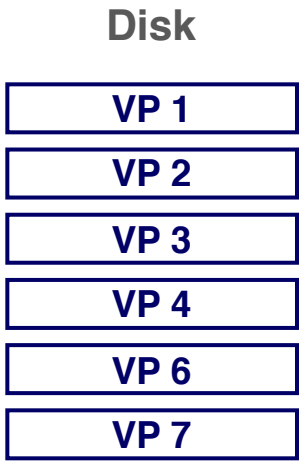

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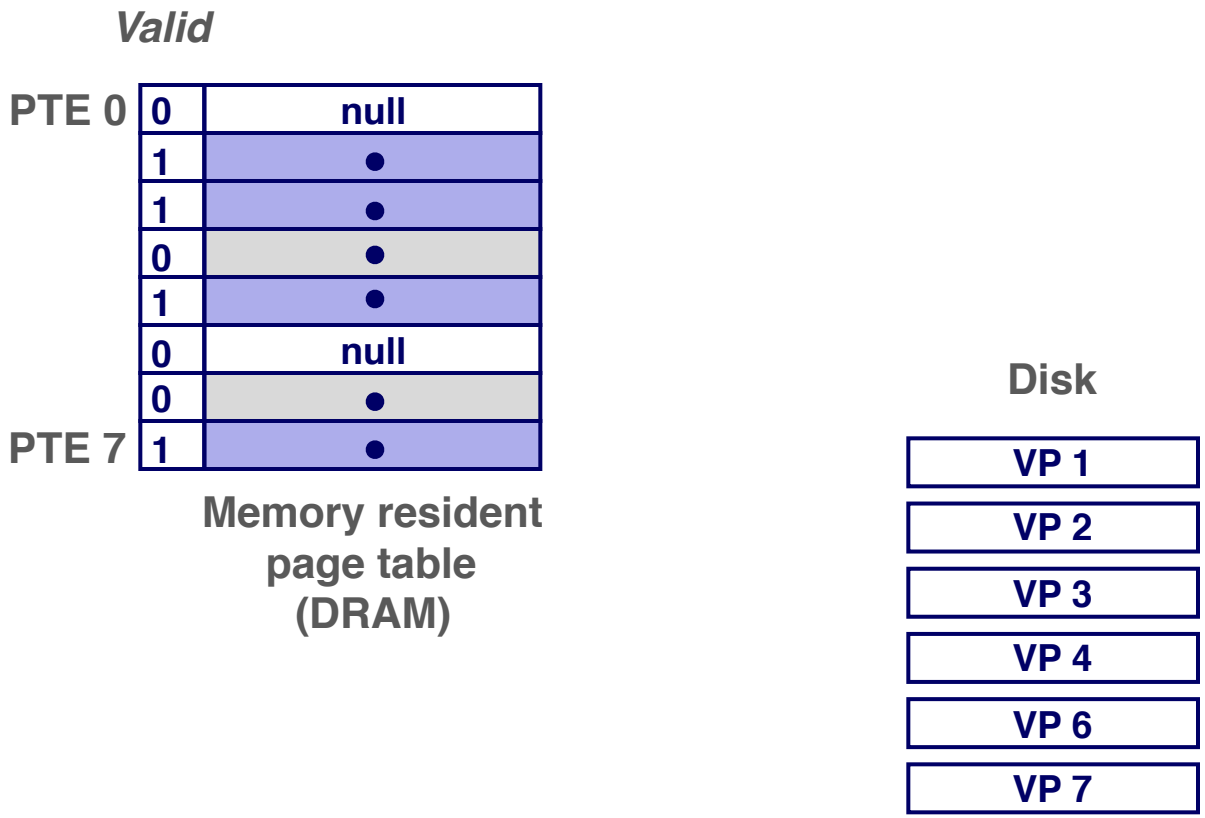

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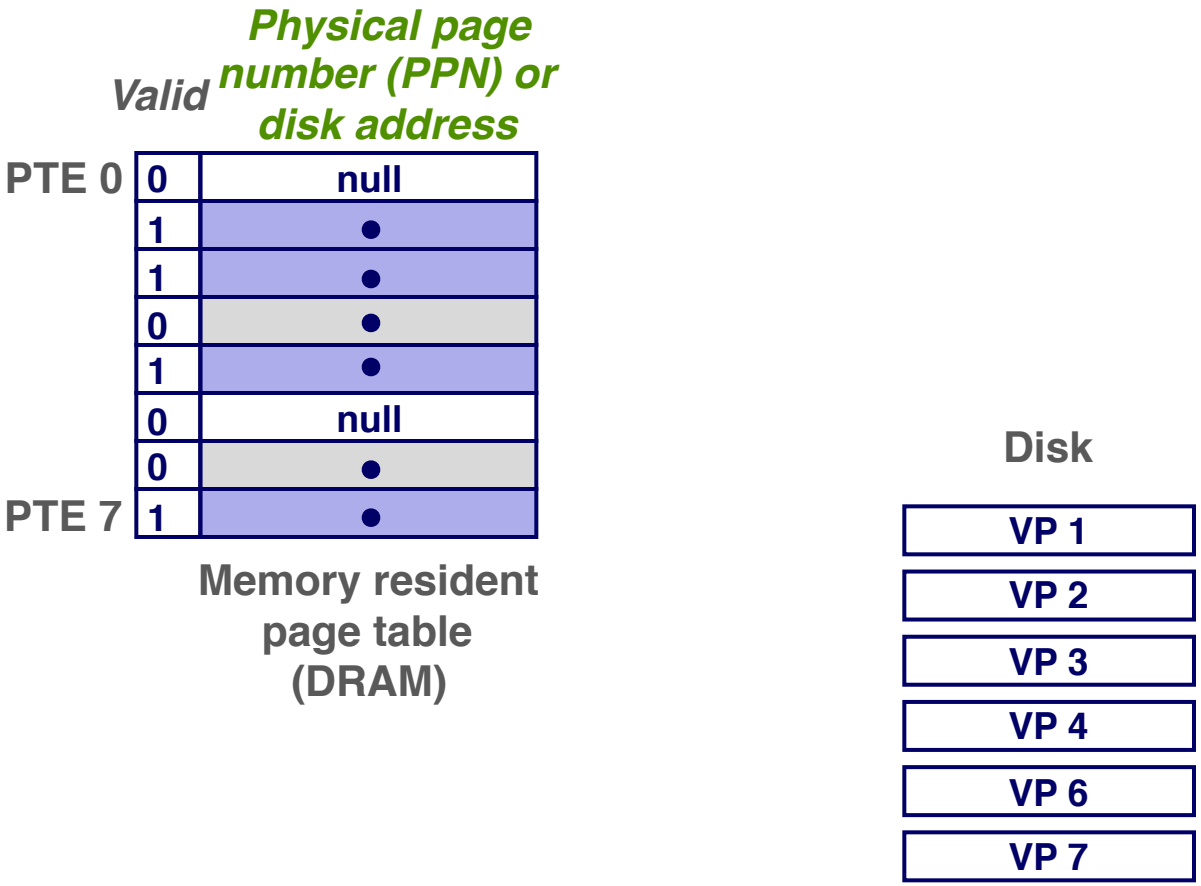

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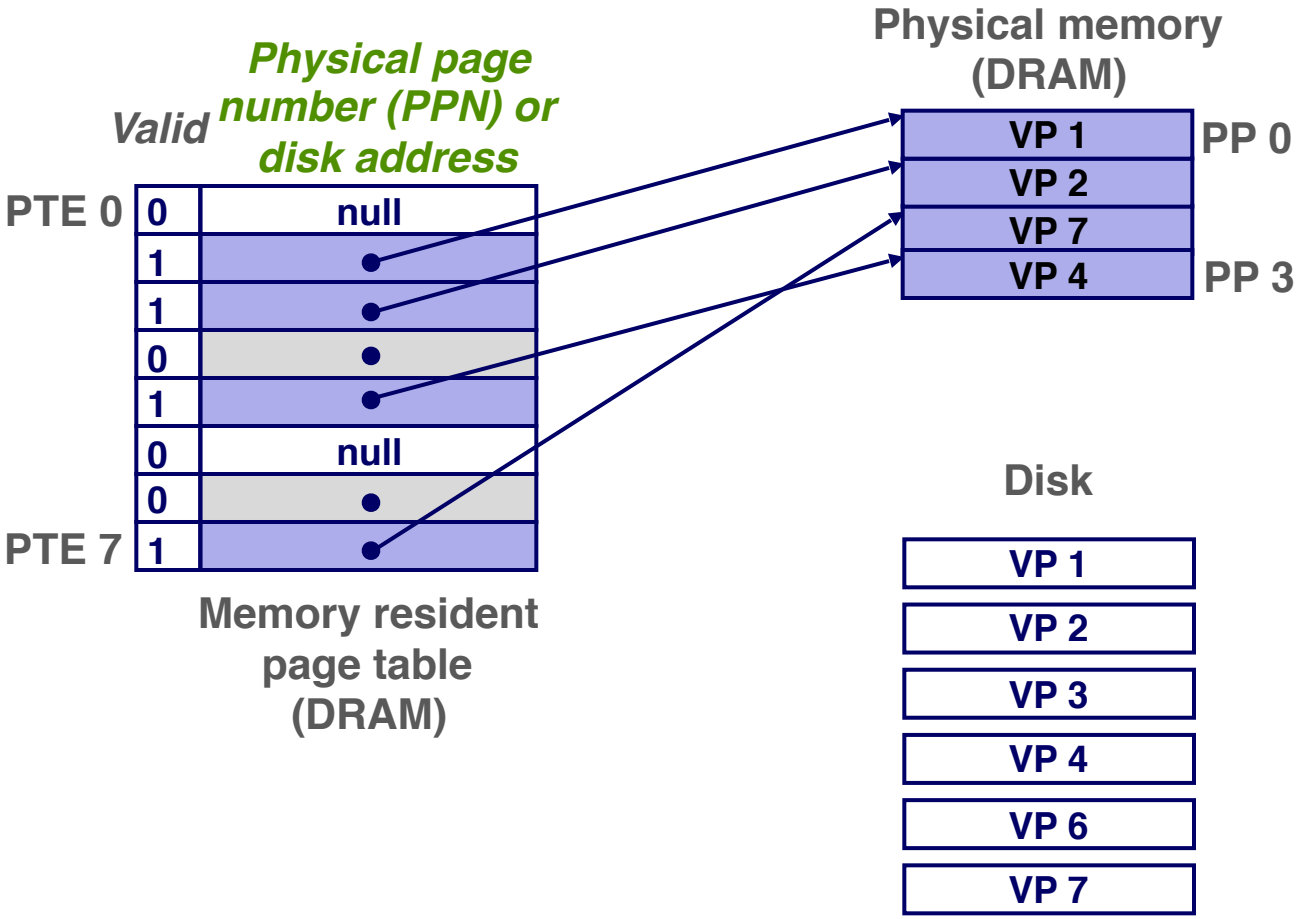

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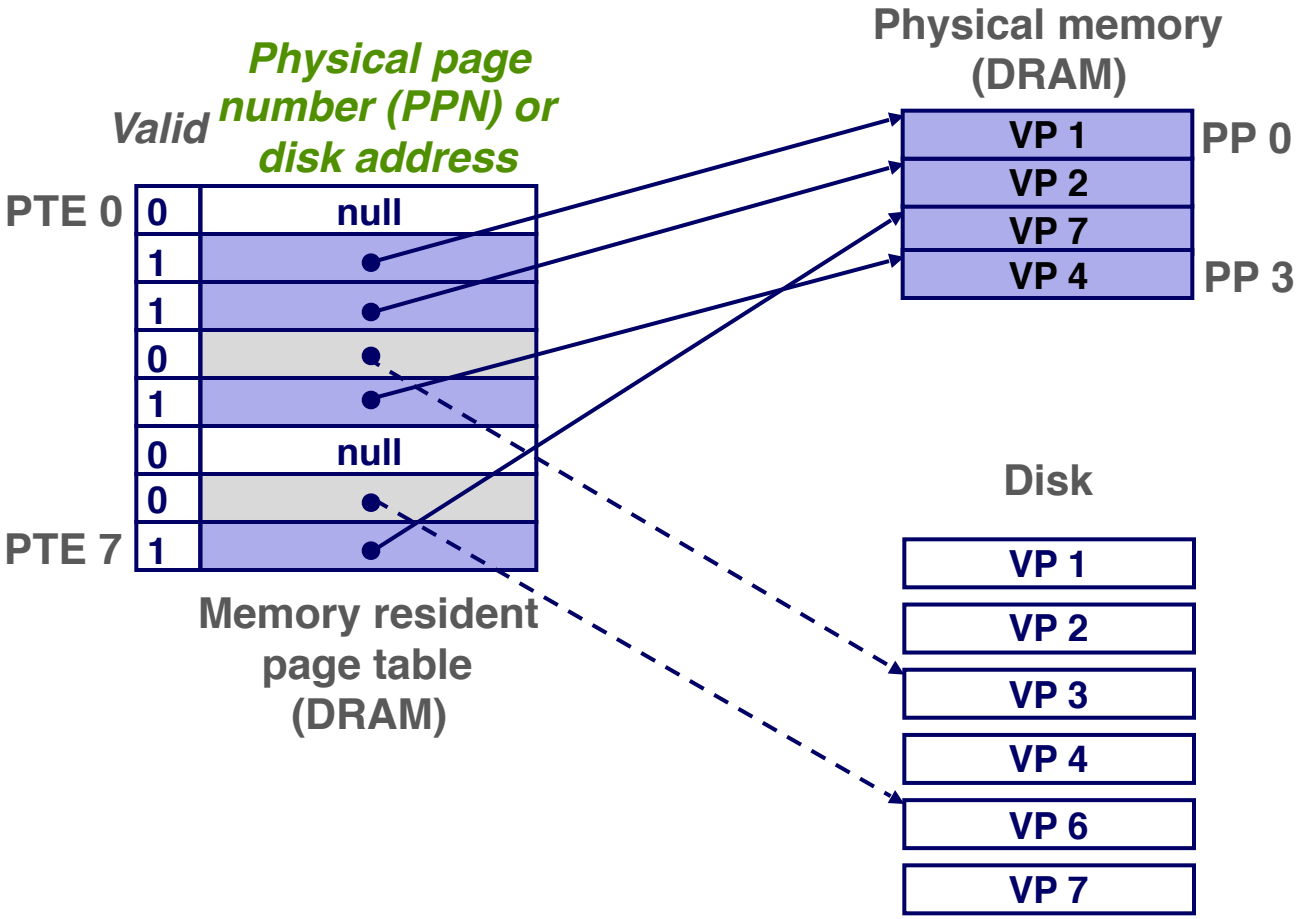

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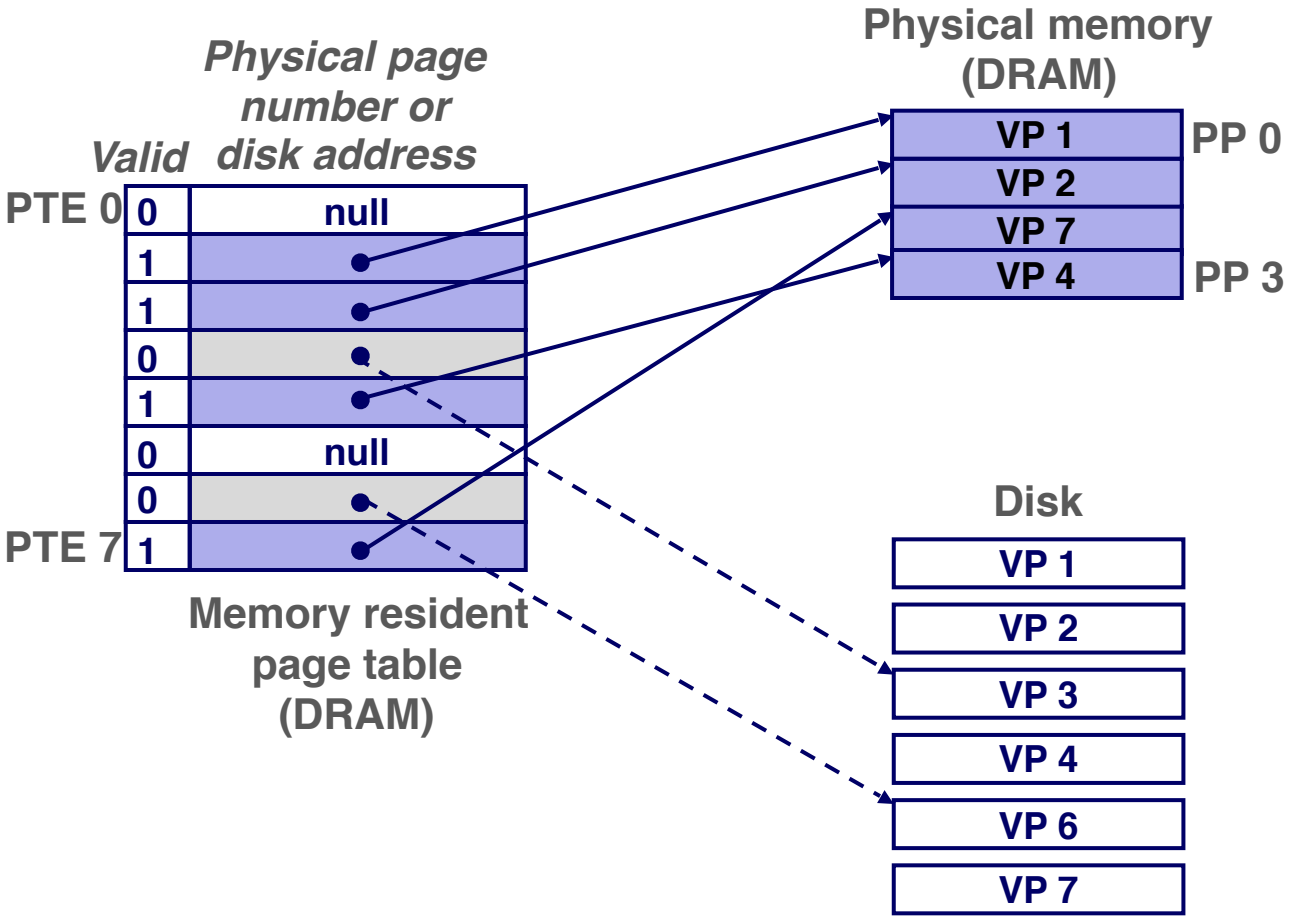

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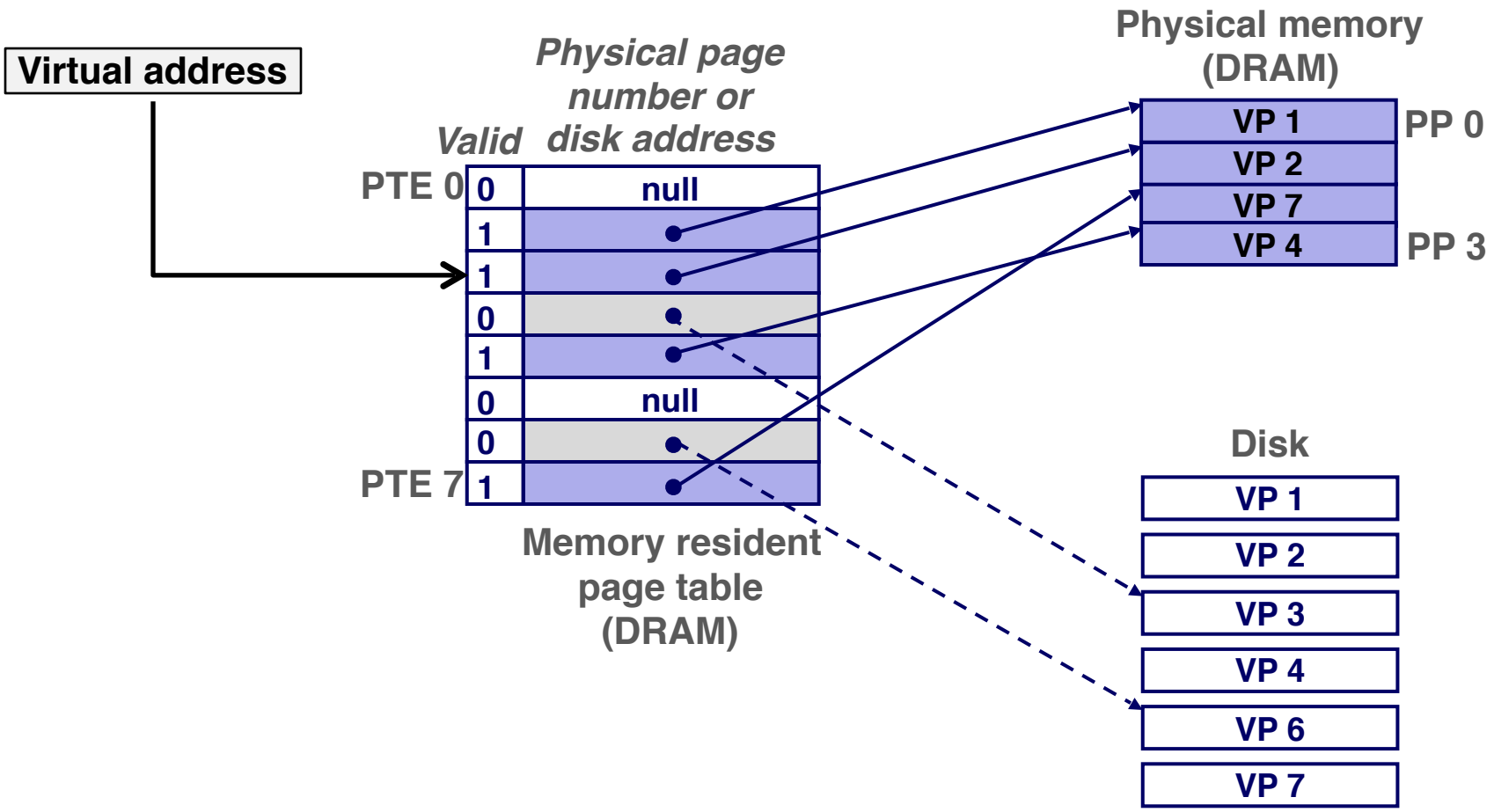

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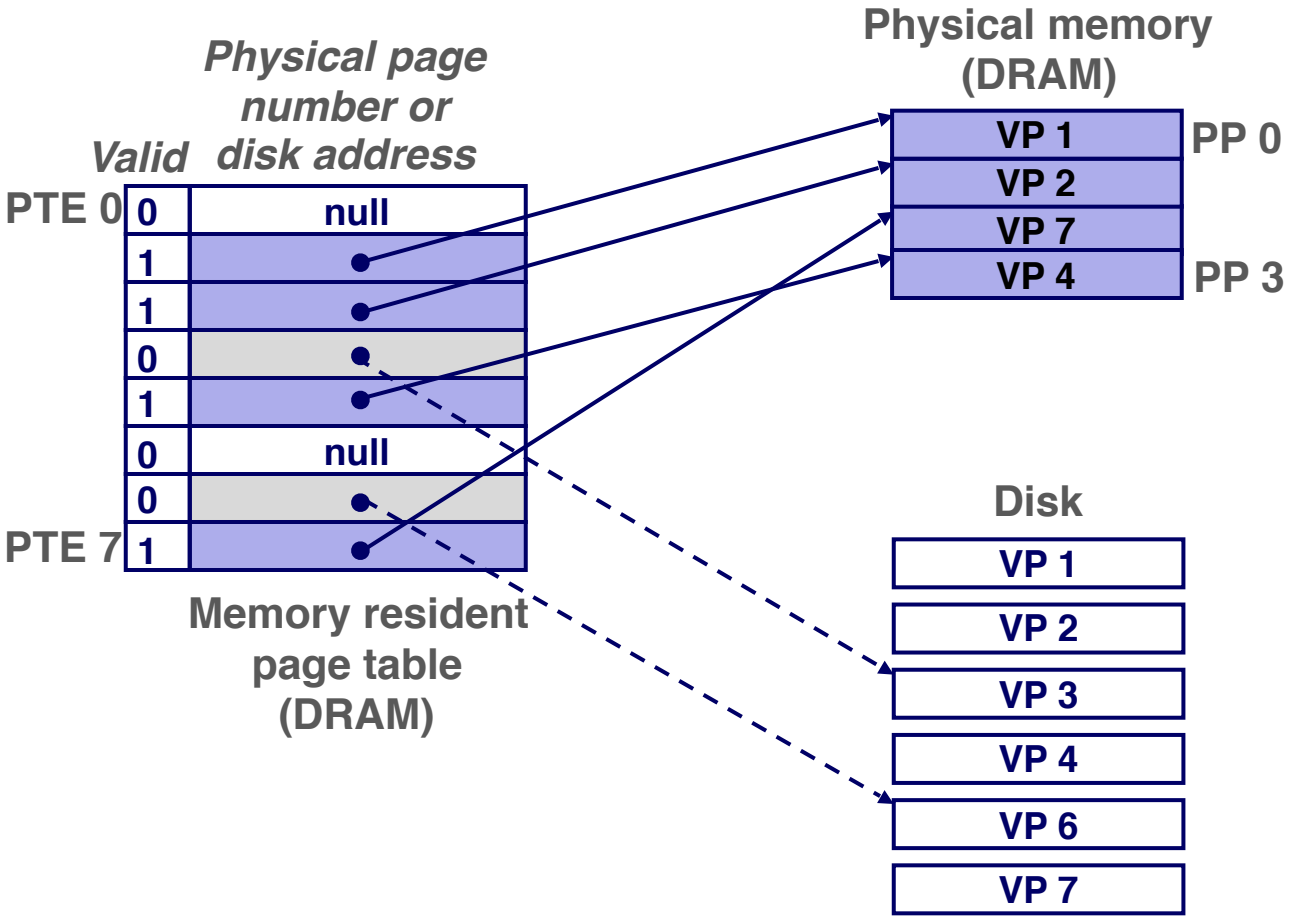

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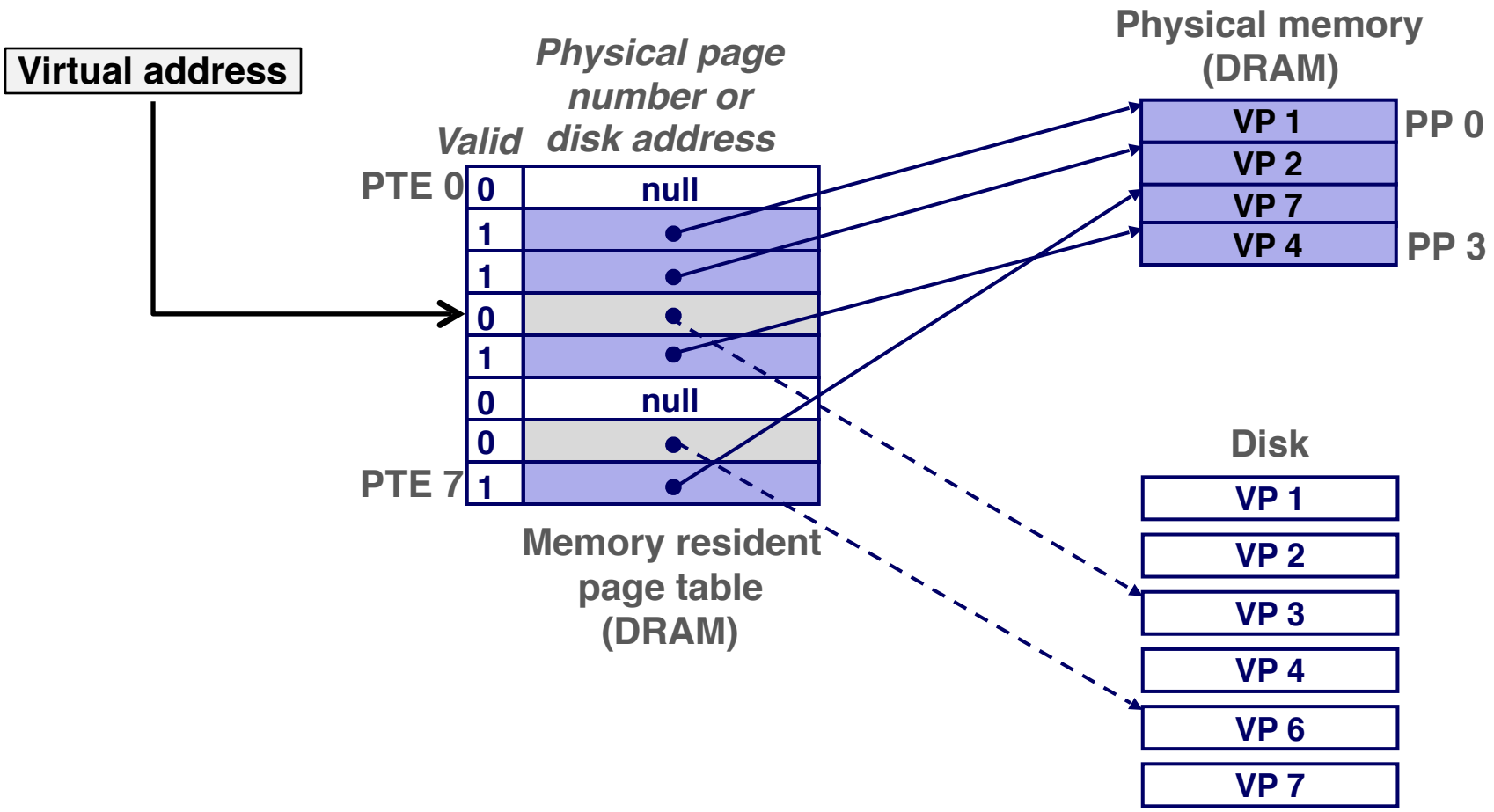

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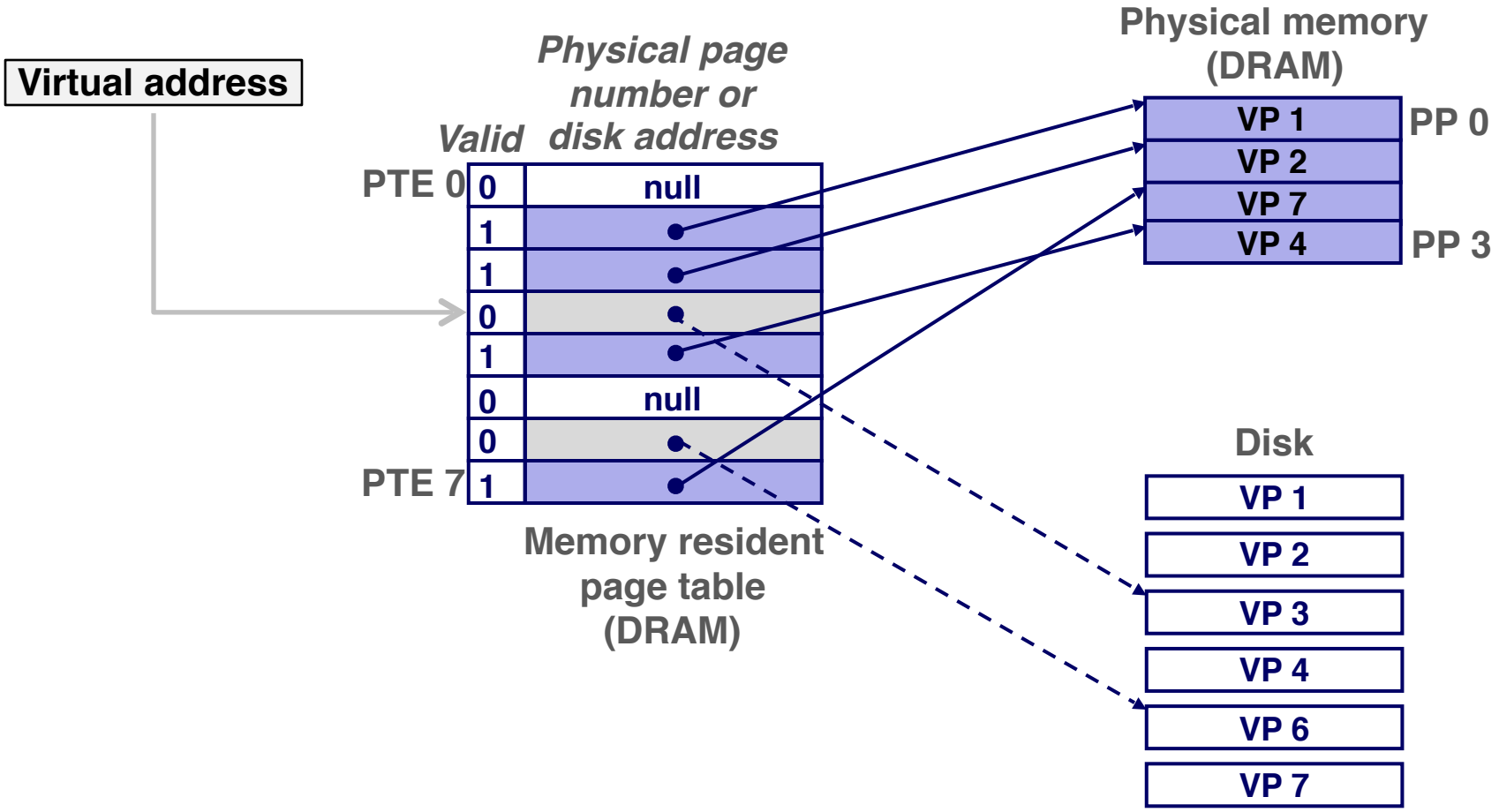

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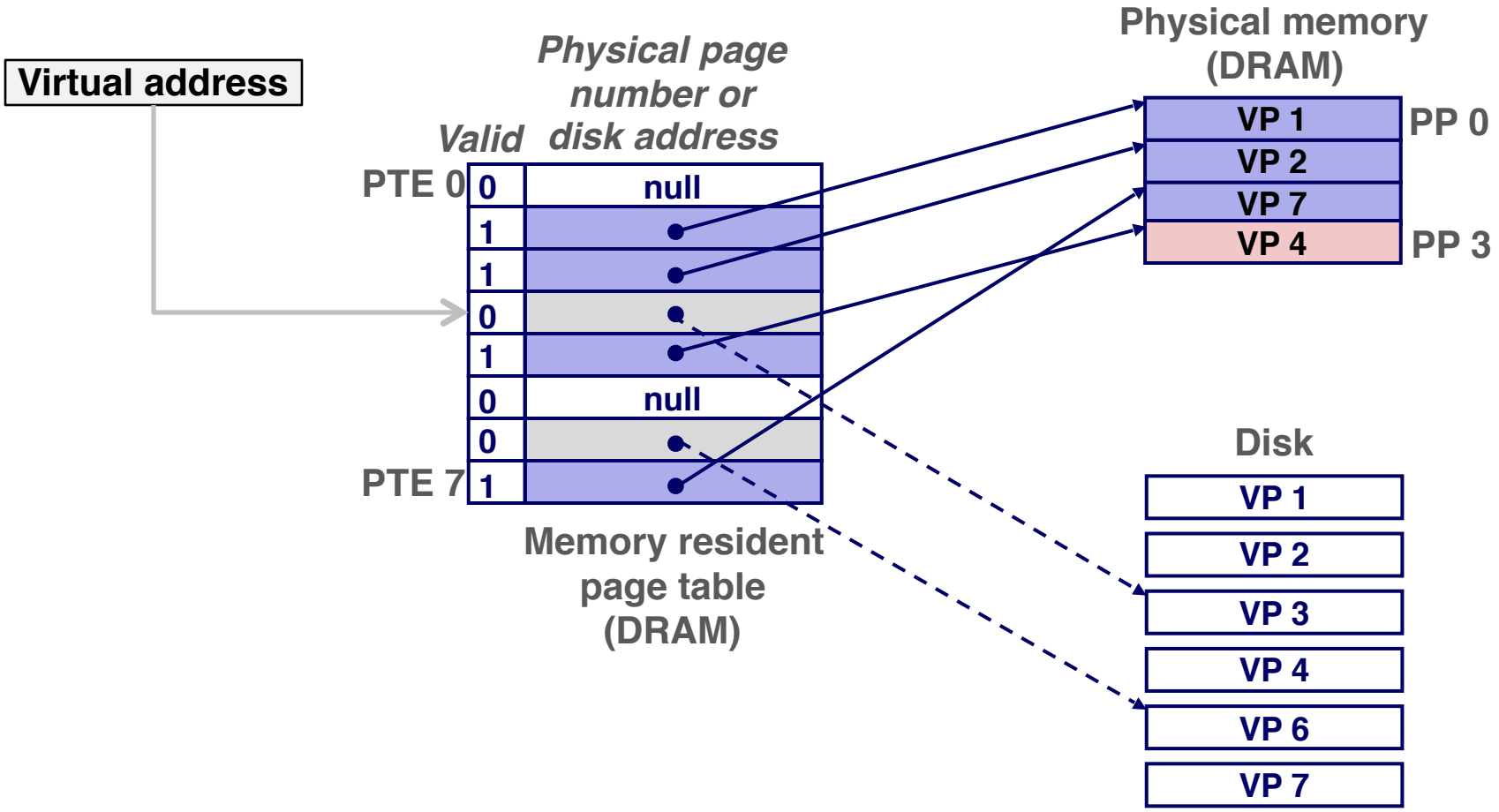

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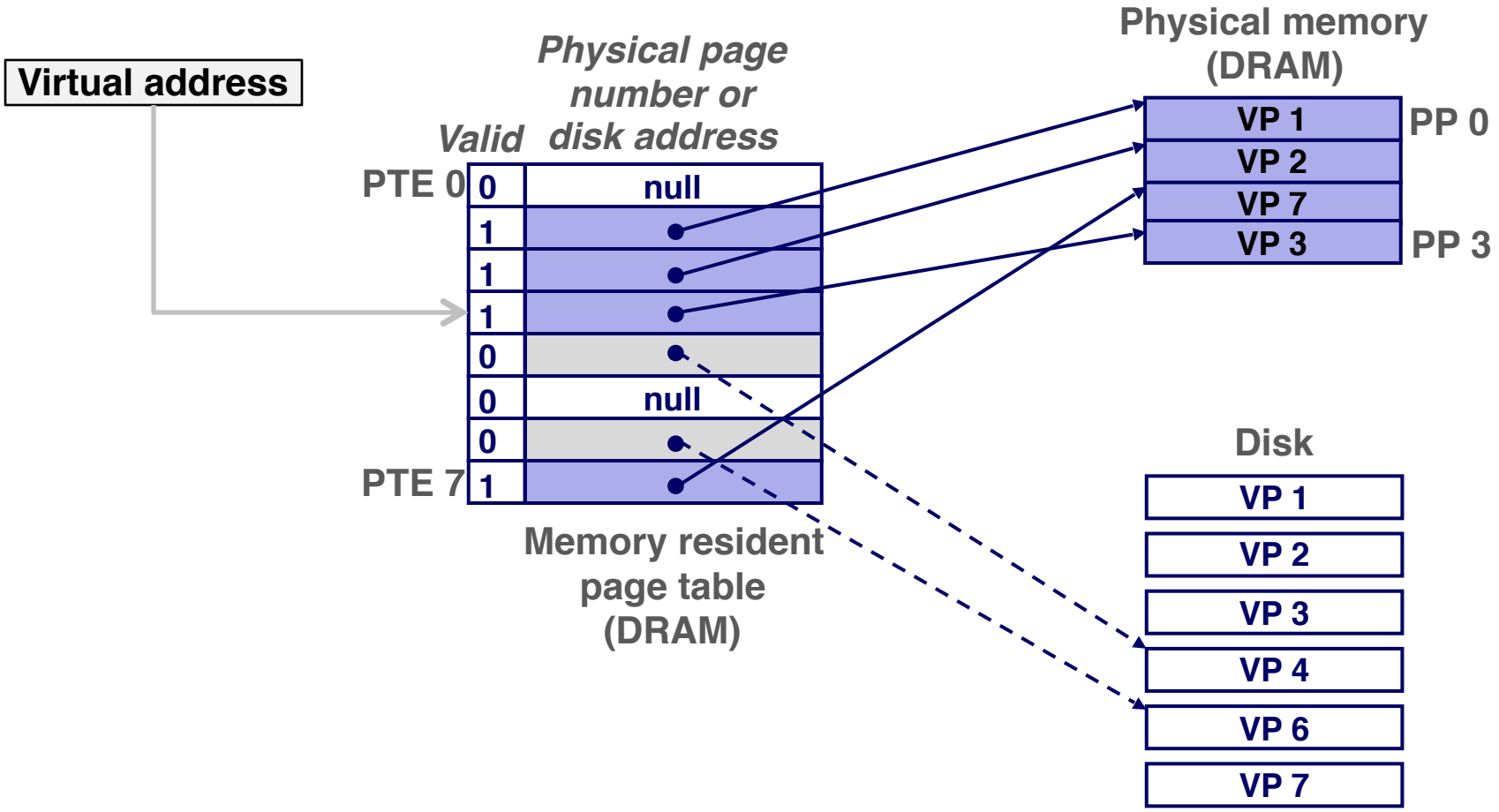

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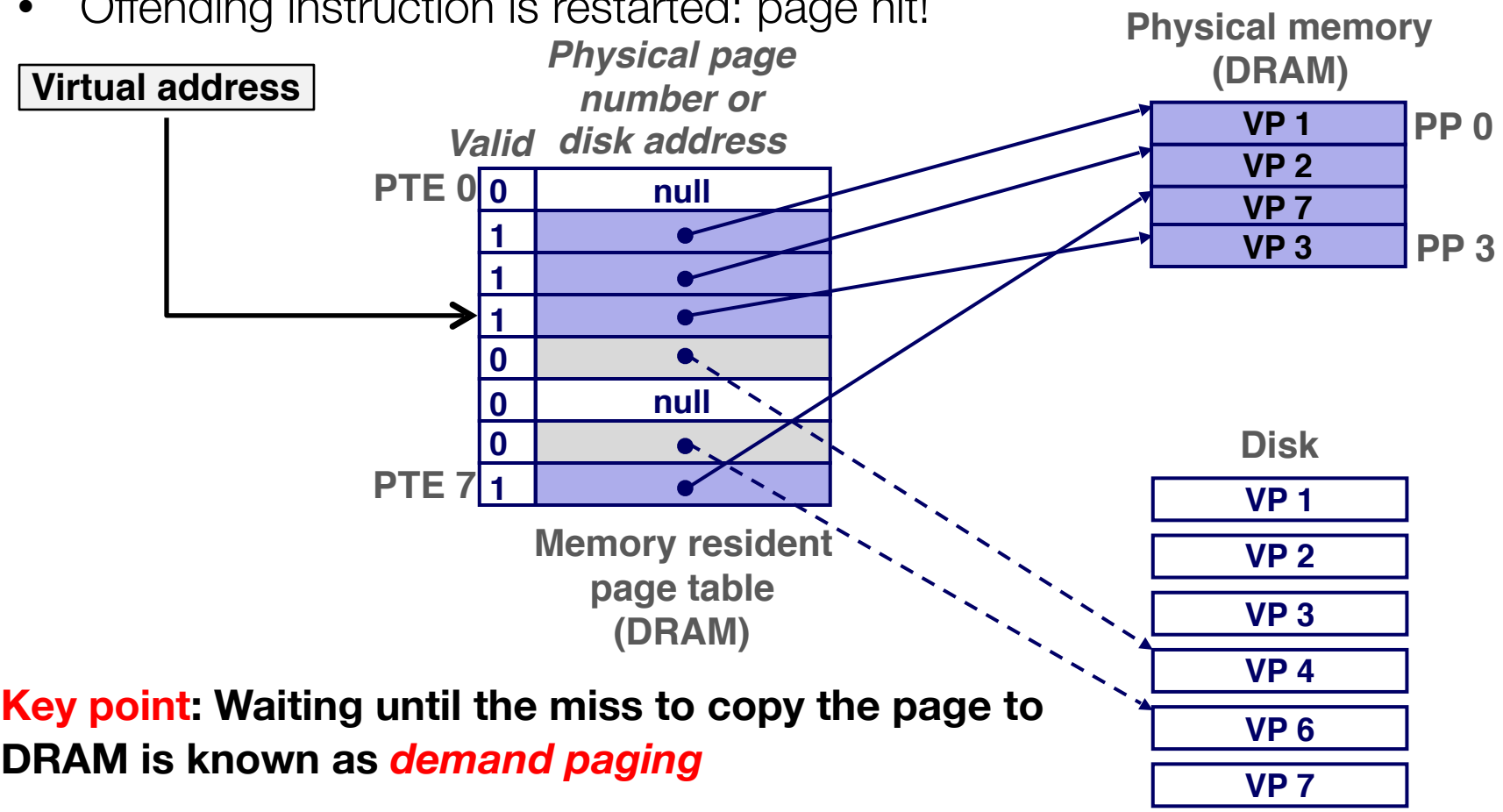

Key point: Waiting until the miss to copy the page to DRAM is known as *demand paging*

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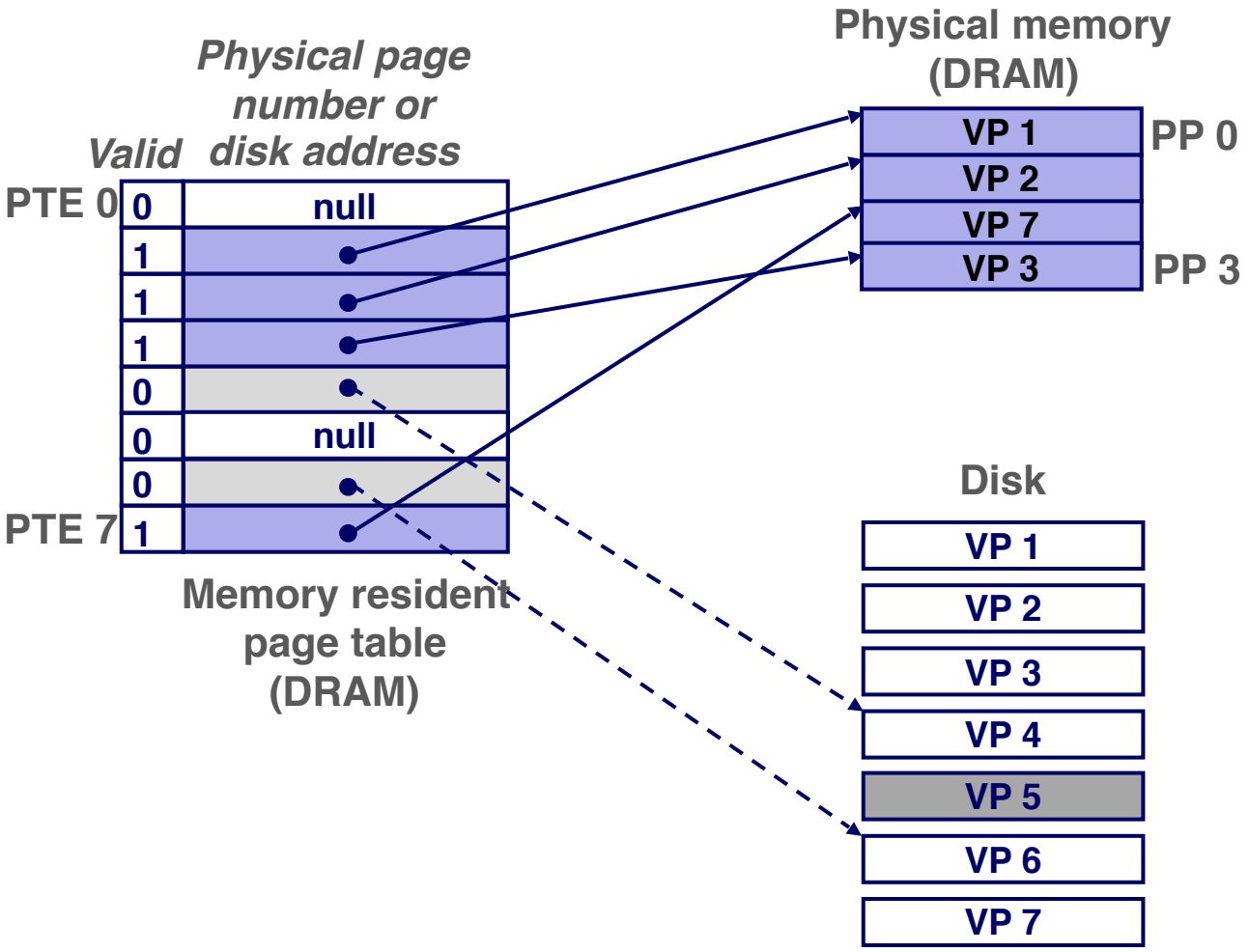

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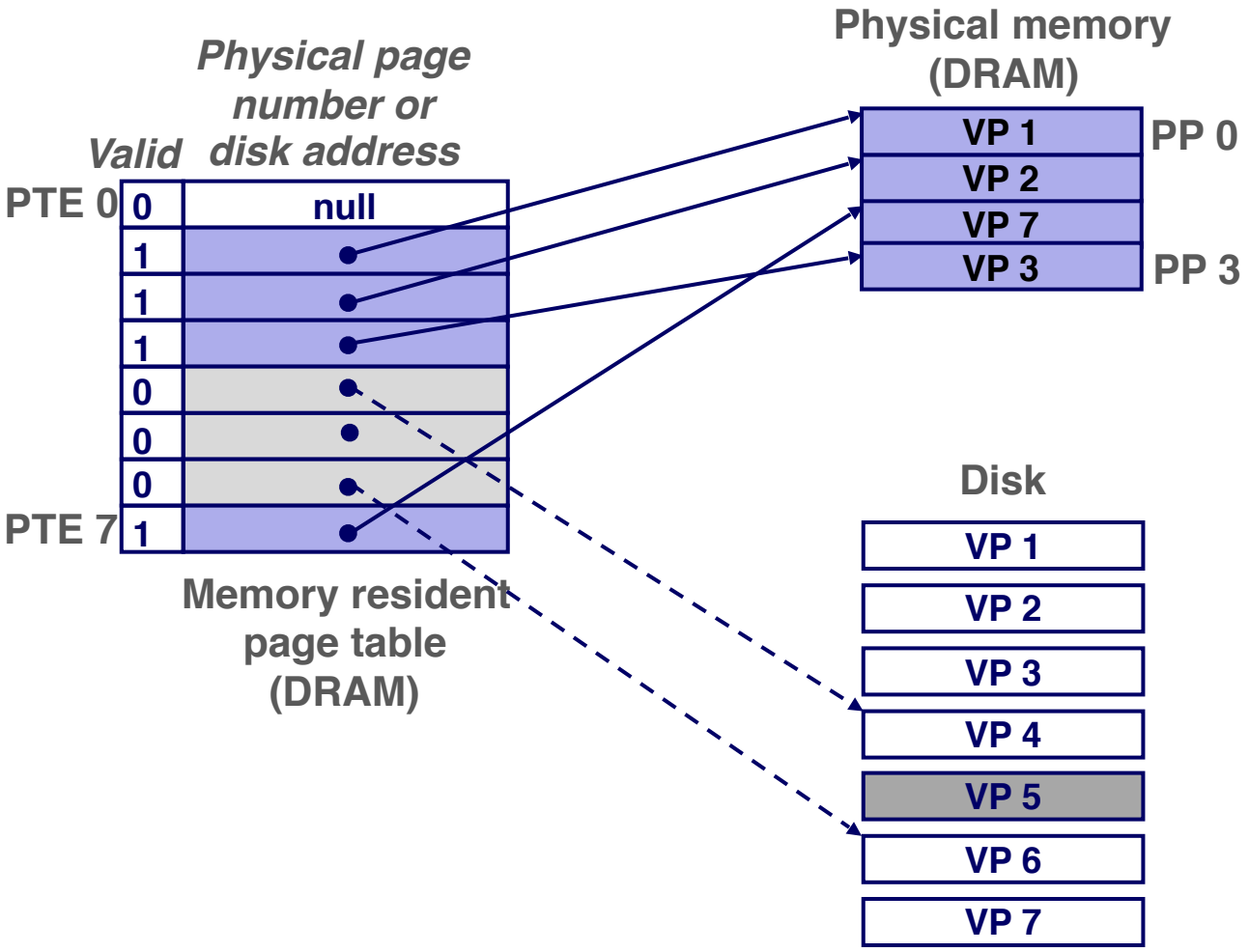

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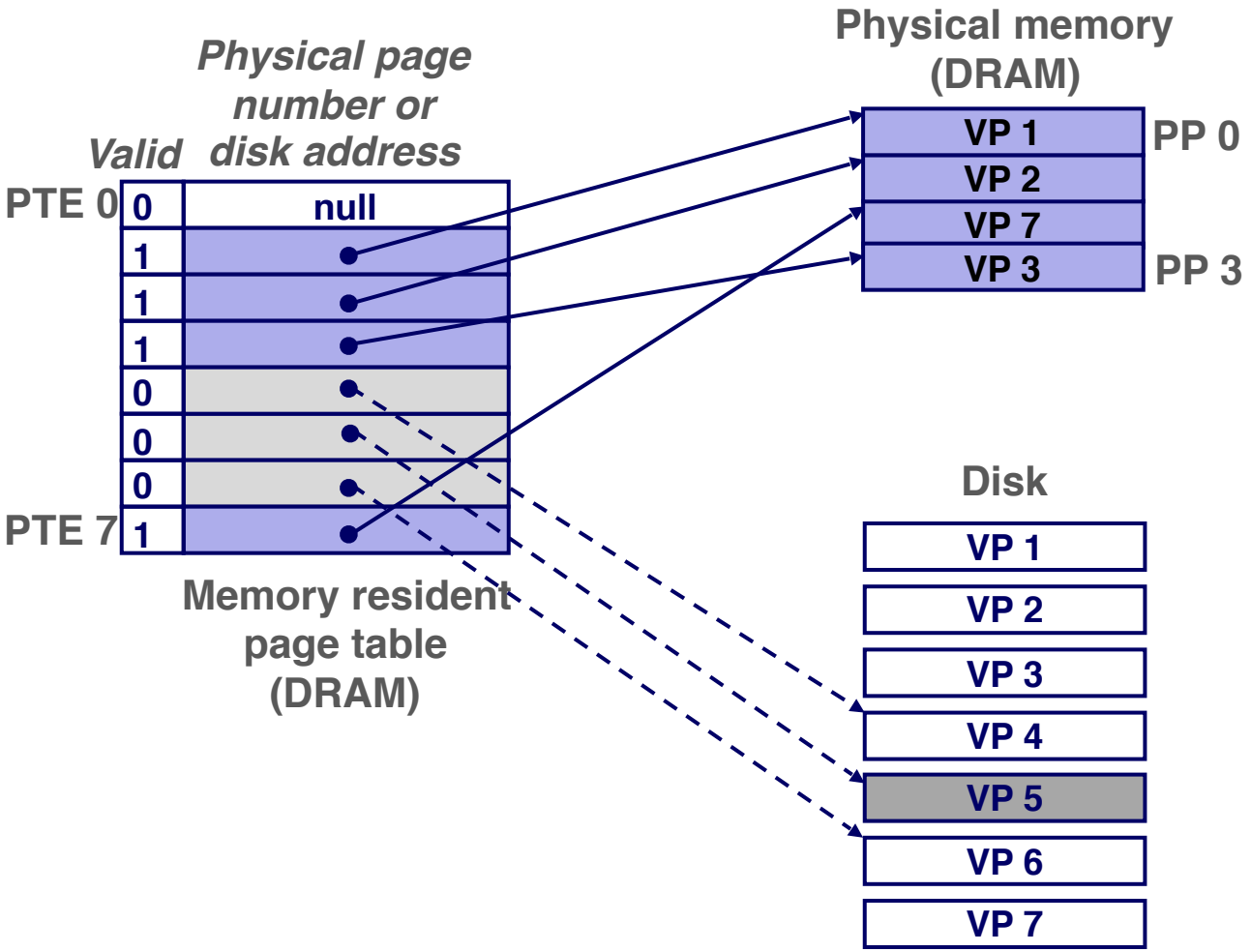

Virtual Memory Exploits Locality (Again!)

- Virtual memory seems terribly inefficient, but it works because of locality.

- At any point in time, programs tend to access a set of active virtual pages called the *working set*
  - Programs with better temporal locality will have smaller working sets

- If (working set size < main memory size)
  - Good performance for one process after initial misses

- If (SUM(working set sizes) > main memory size)
  - *Thrashing:* Performance meltdown where pages are swapped (copied) in and out continuously

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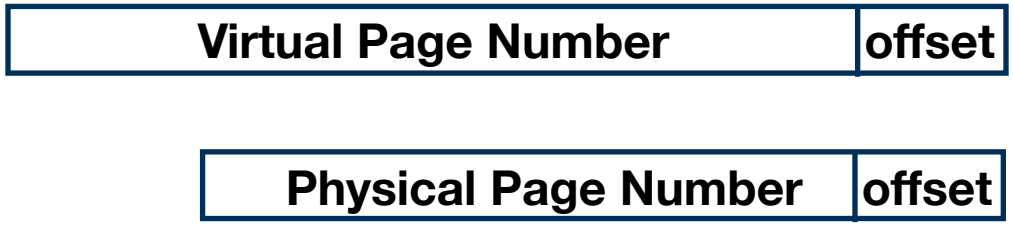

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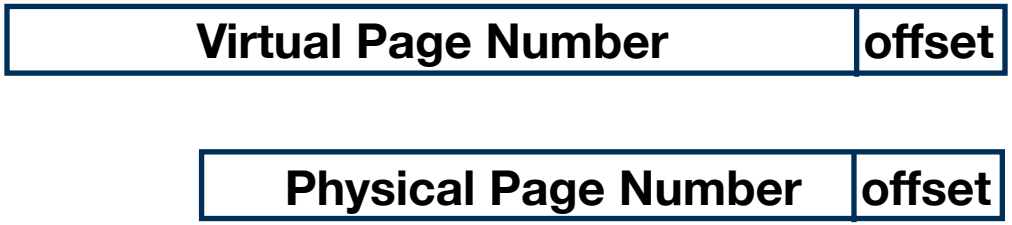

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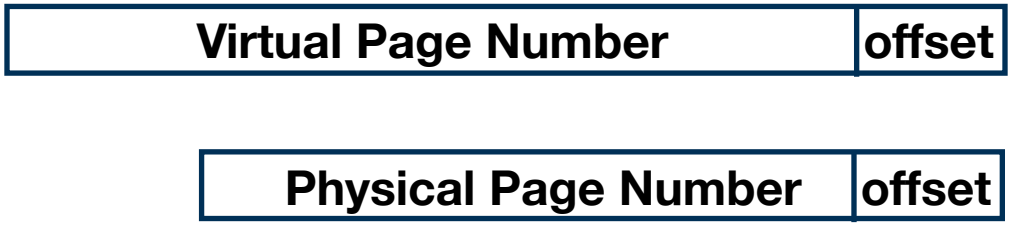

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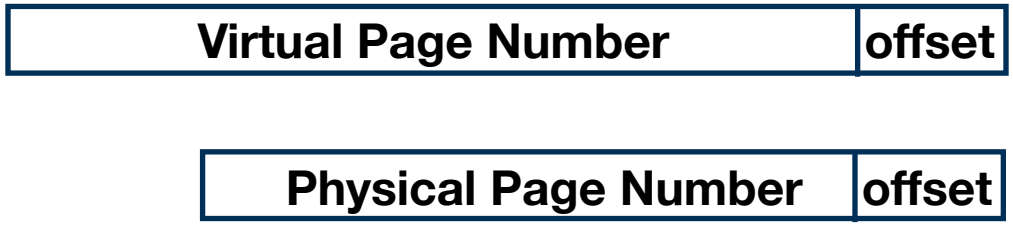

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- ~MBs of a page table *per process*
  - Too big for on-chip SRAM (c.f., a L1 cache is ~32 KB)
  - Too slow to access in disk
  - Put the page table in DRAM, with its start address stored in a special register (Page Table Base Register). More on this later.

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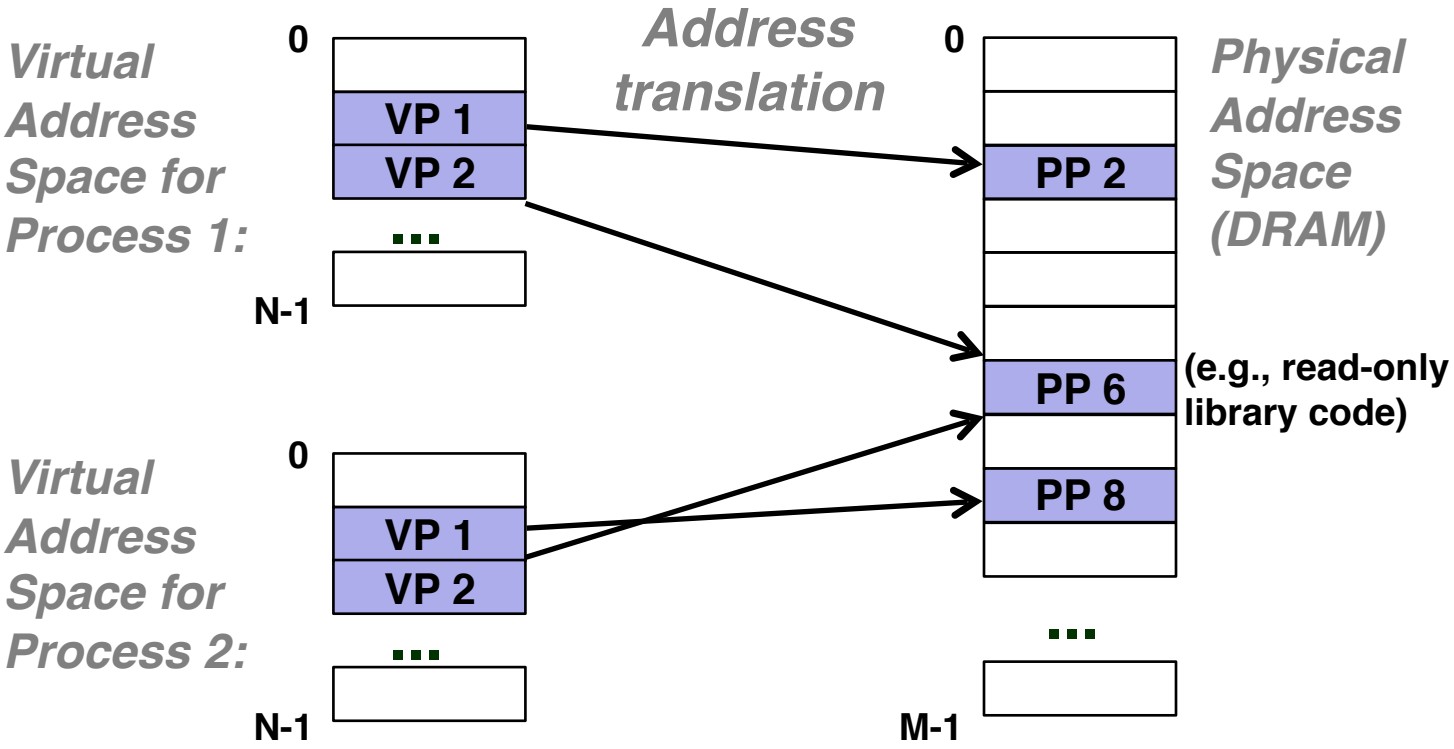
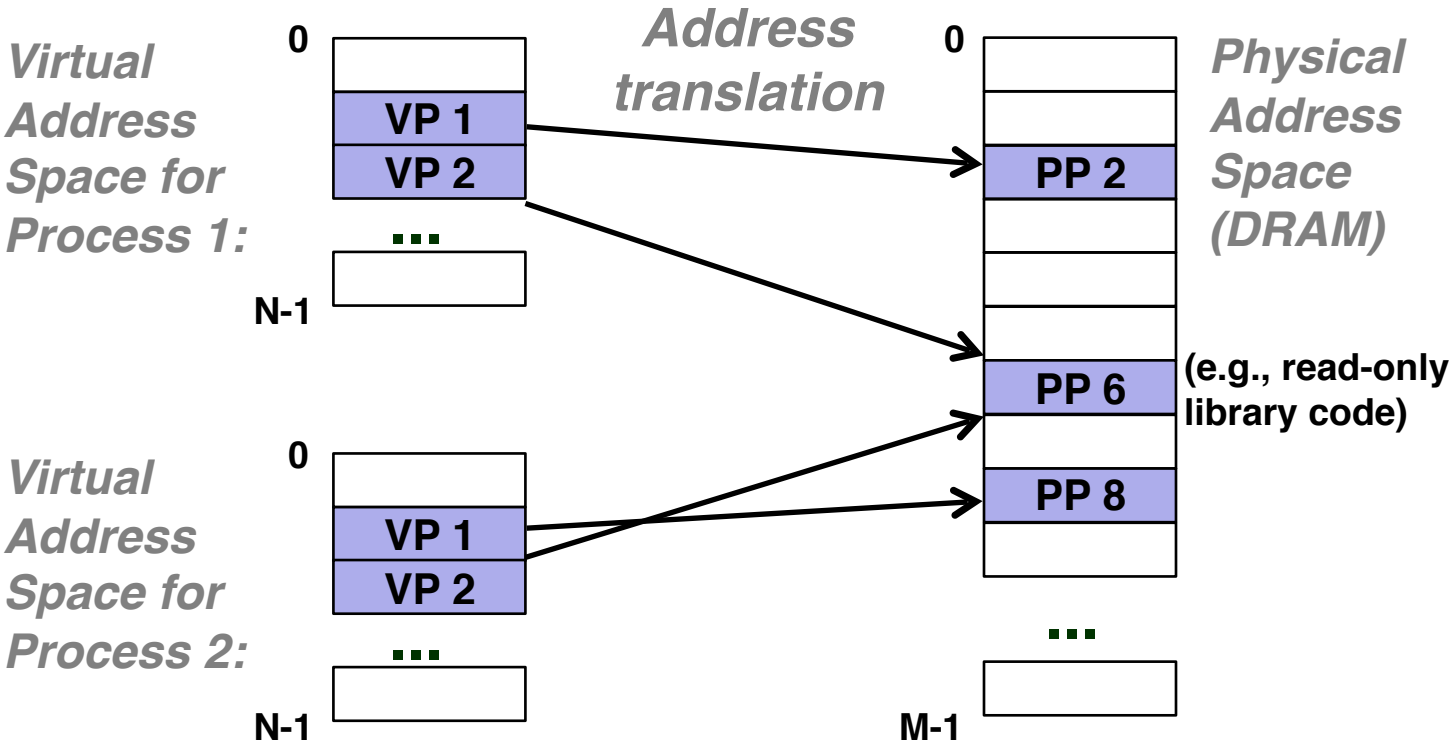
VM as a Tool for Memory Management

- Each process has its own virtual address space
  - It can view memory as a simple linear array
  - Mapping scatters addresses through physical memory
    - Well-chosen mappings can improve locality



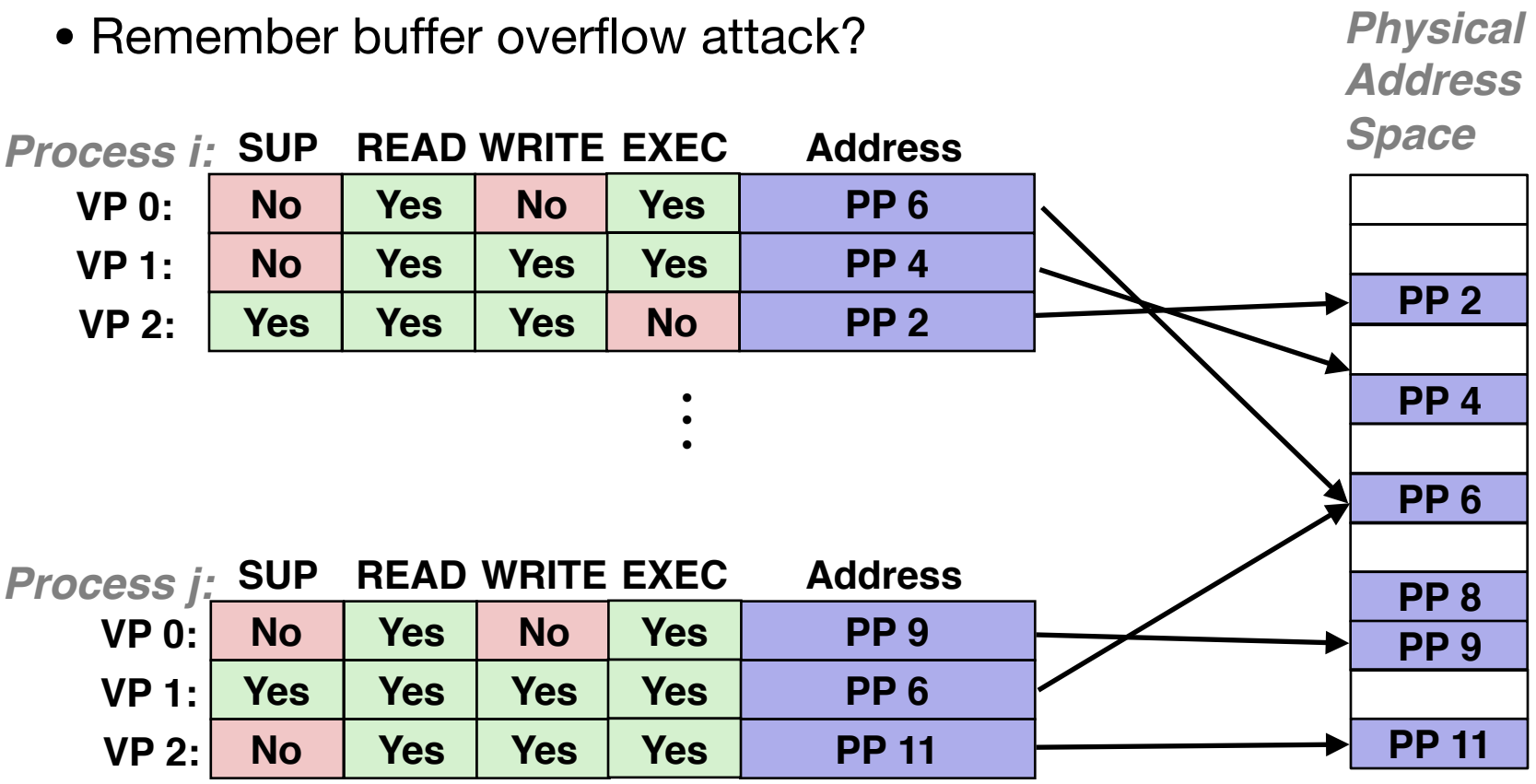
Virtual Memory Enables Sharing

- Simplifying memory allocation
  - Each virtual page can be mapped to any physical page
  - A virtual page can be stored in different physical pages at different times
- Sharing code and data among processes
  - Map virtual pages to the same physical page (here: PP 6)



VM Provides Further Protection Opportunities

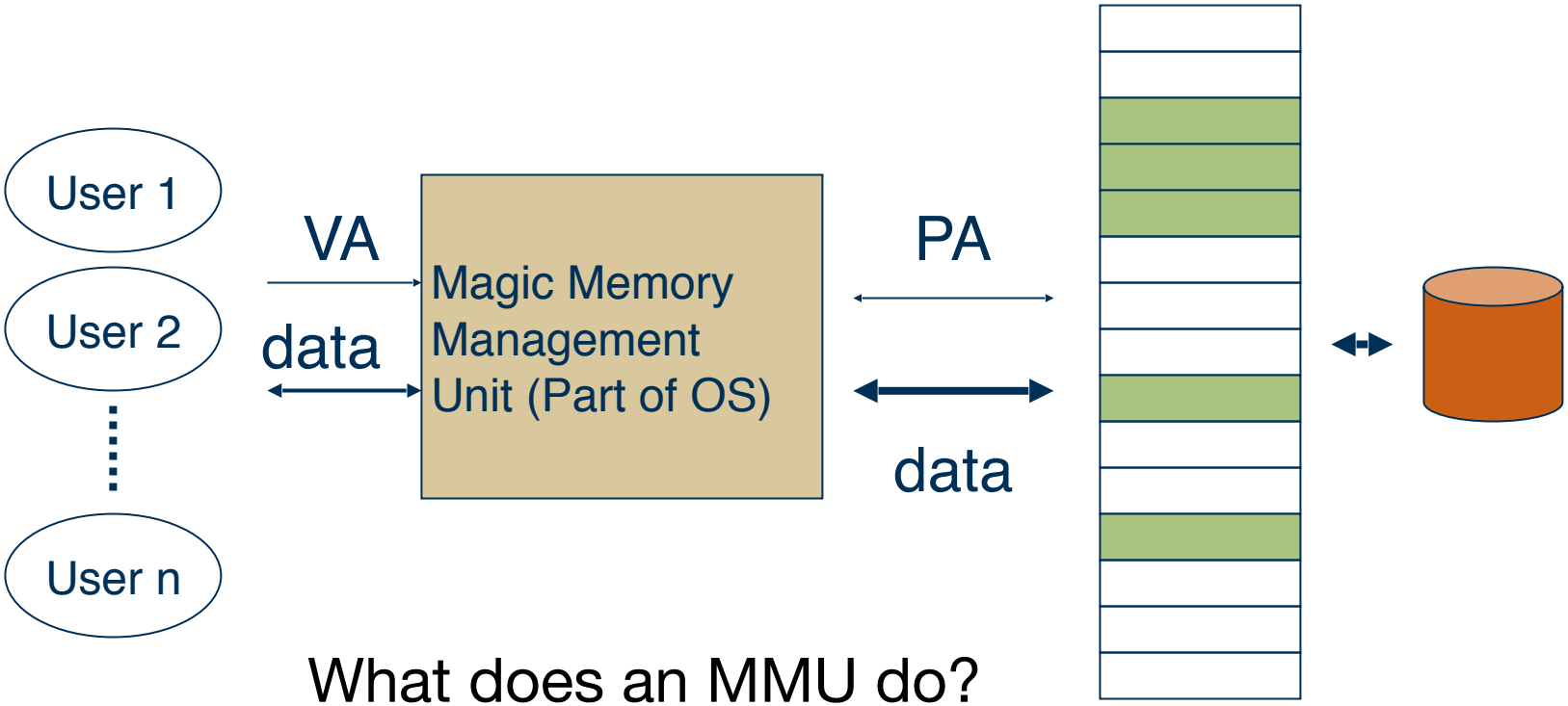
- Extend PTEs with permission bits
- MMU checks these bits on each access (read/write/executable/ accessible only in supervisor mode?)
- Remember buffer overflow attack?



Today

- VM basic concepts and operation
- Other critical benefits of VM
- Address translation

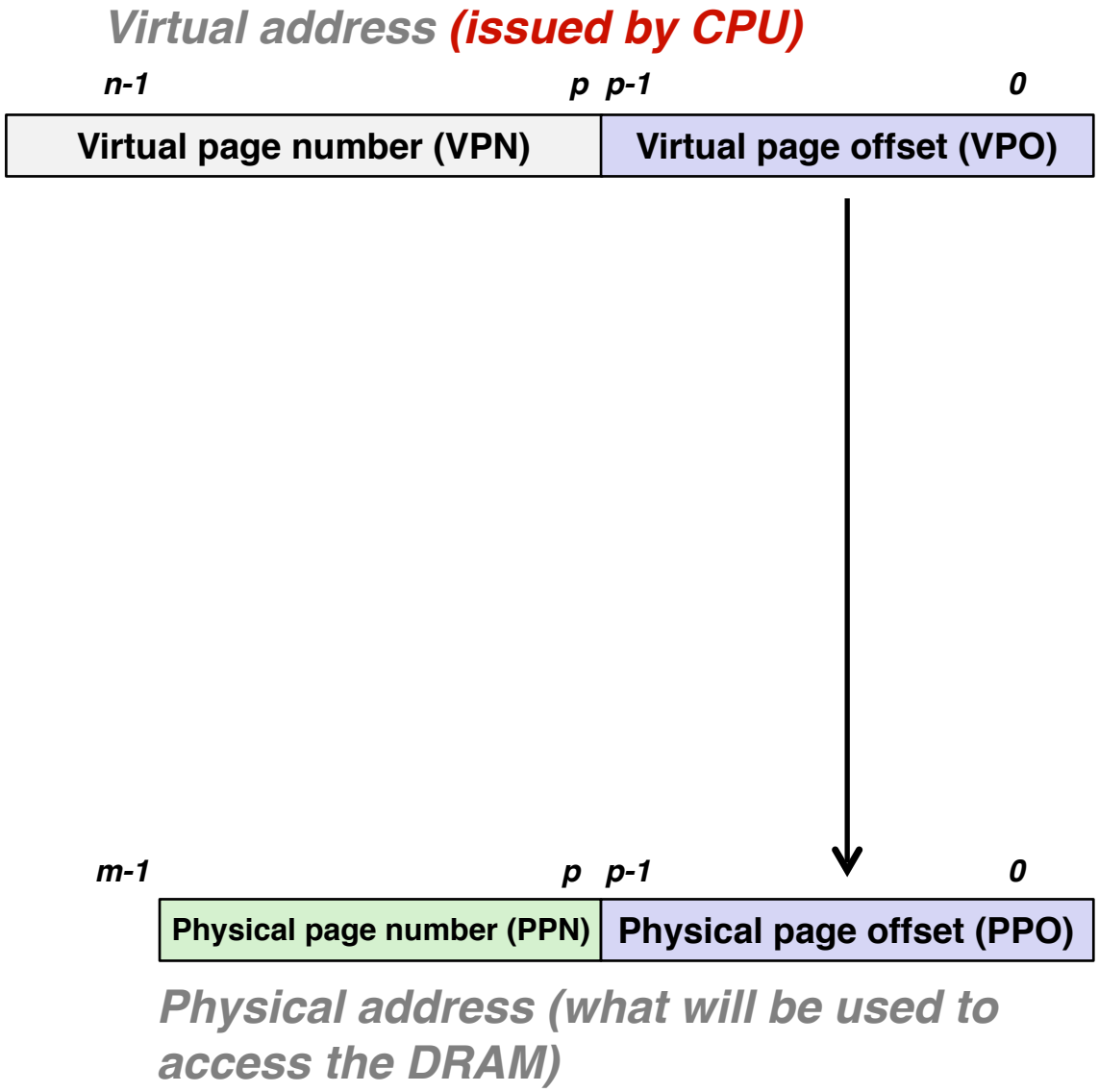
So Far…



What does an MMU do?

- Translate address from a VA to PA
  - Enforce permissions
  - Fetch from disk

Address Translation With a Page Table



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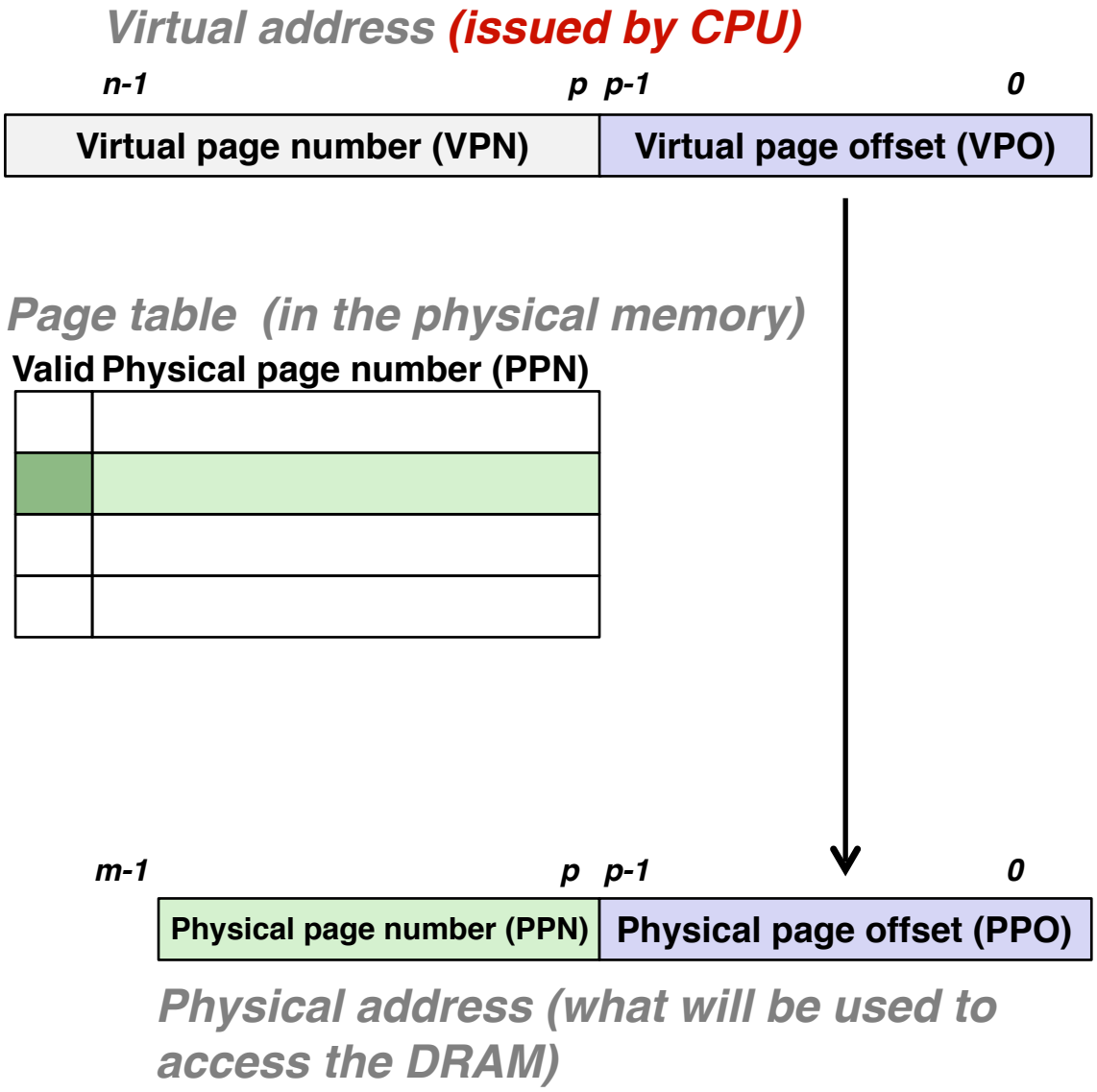

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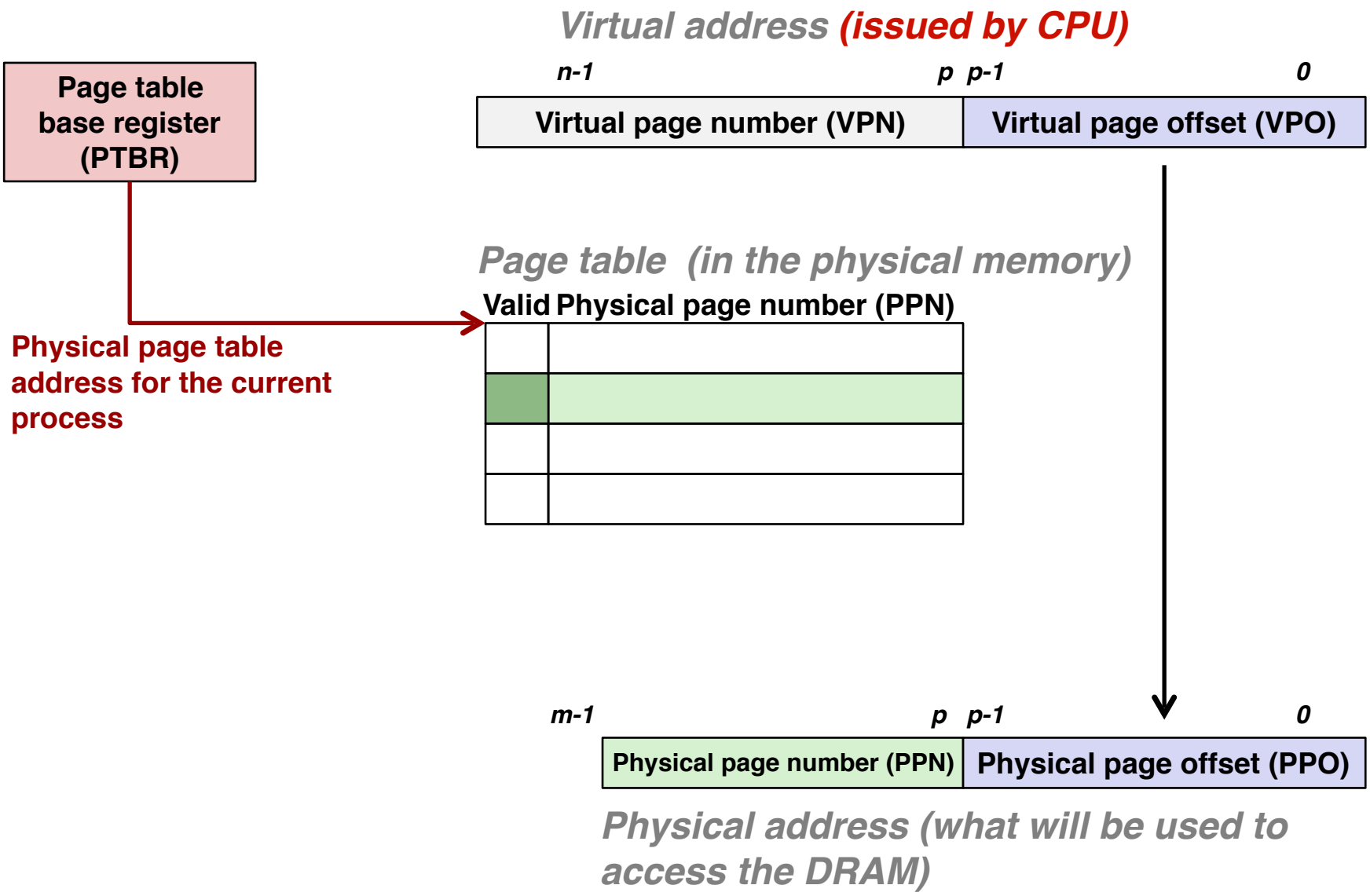

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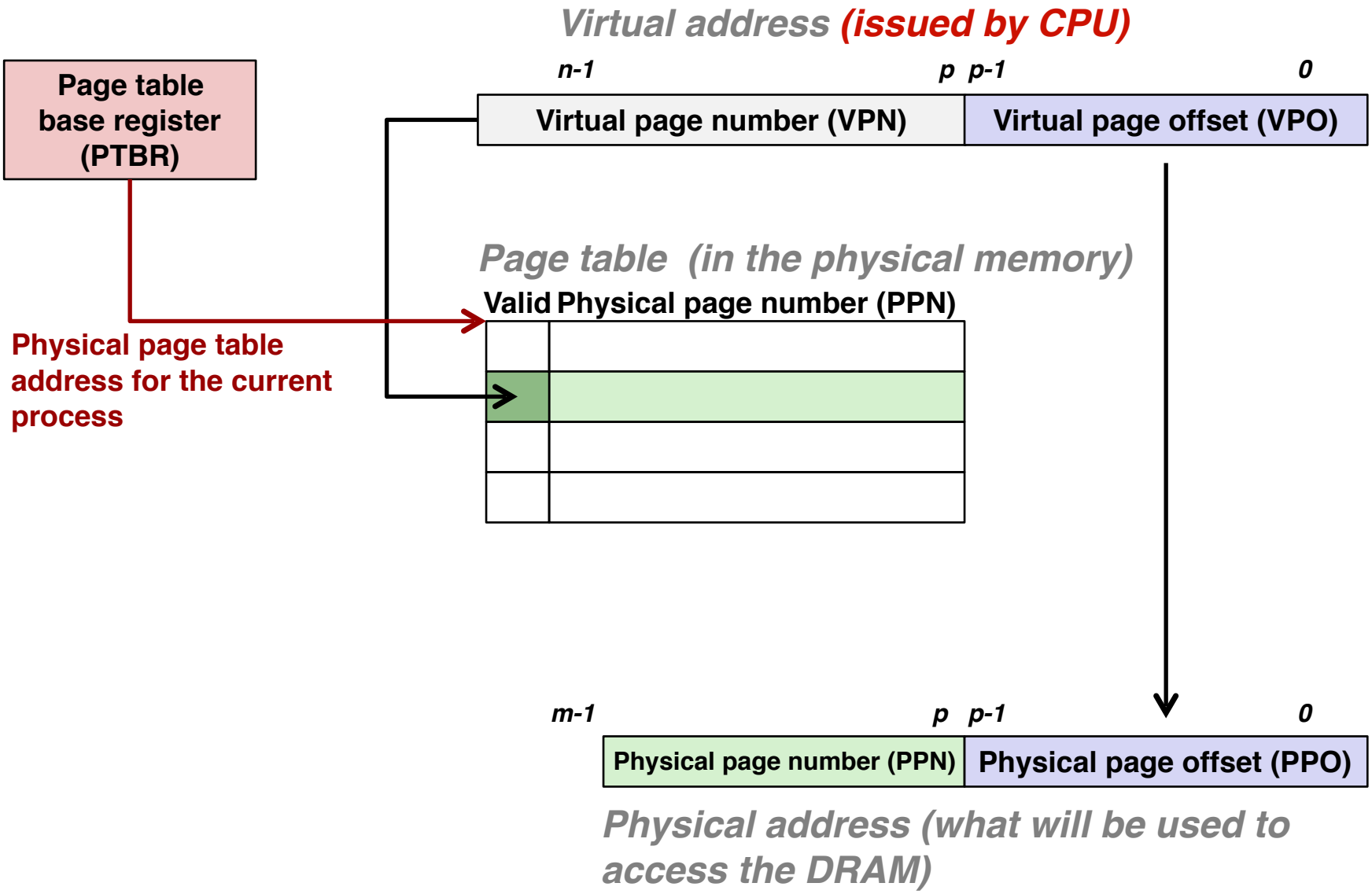

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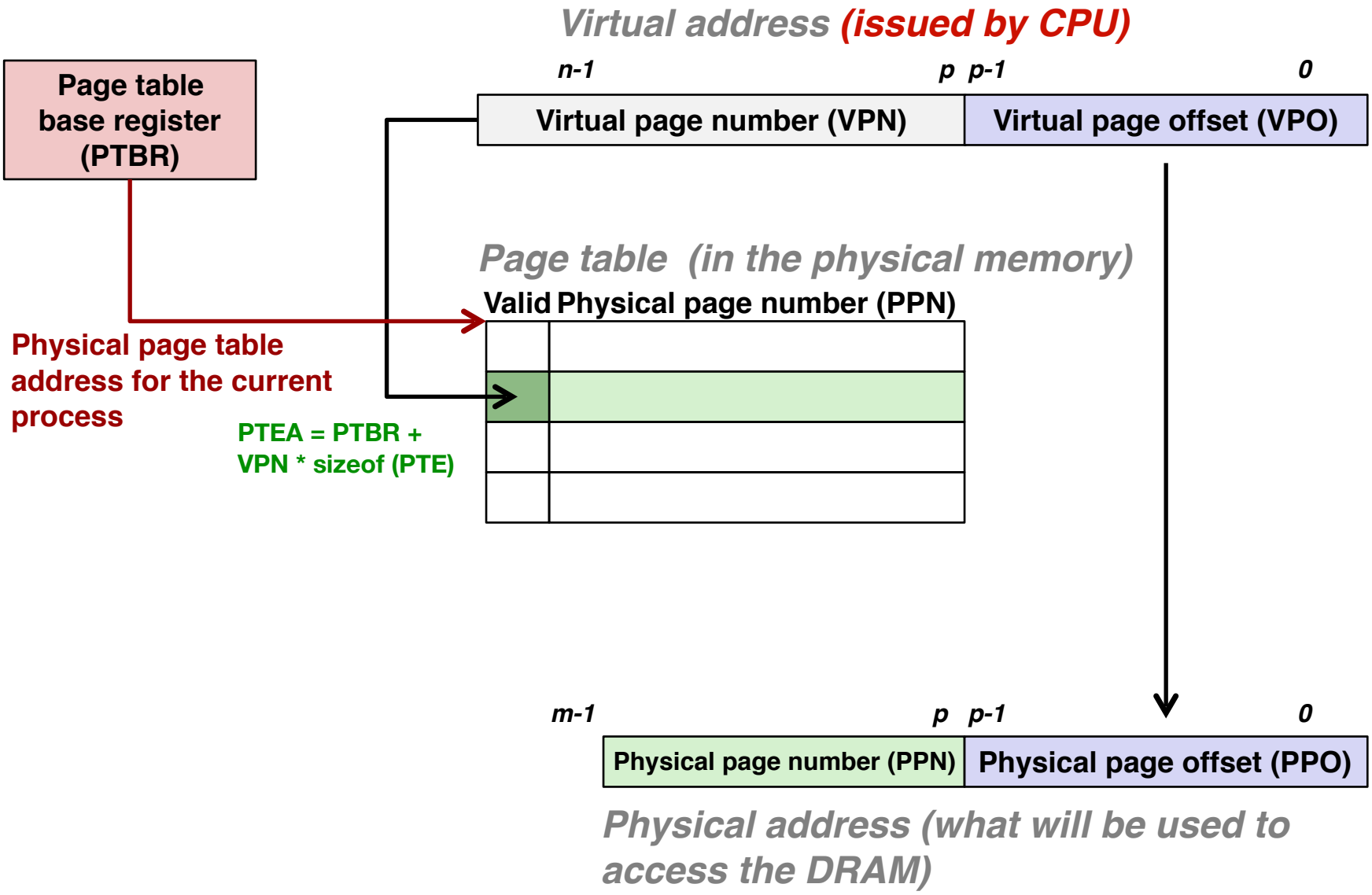

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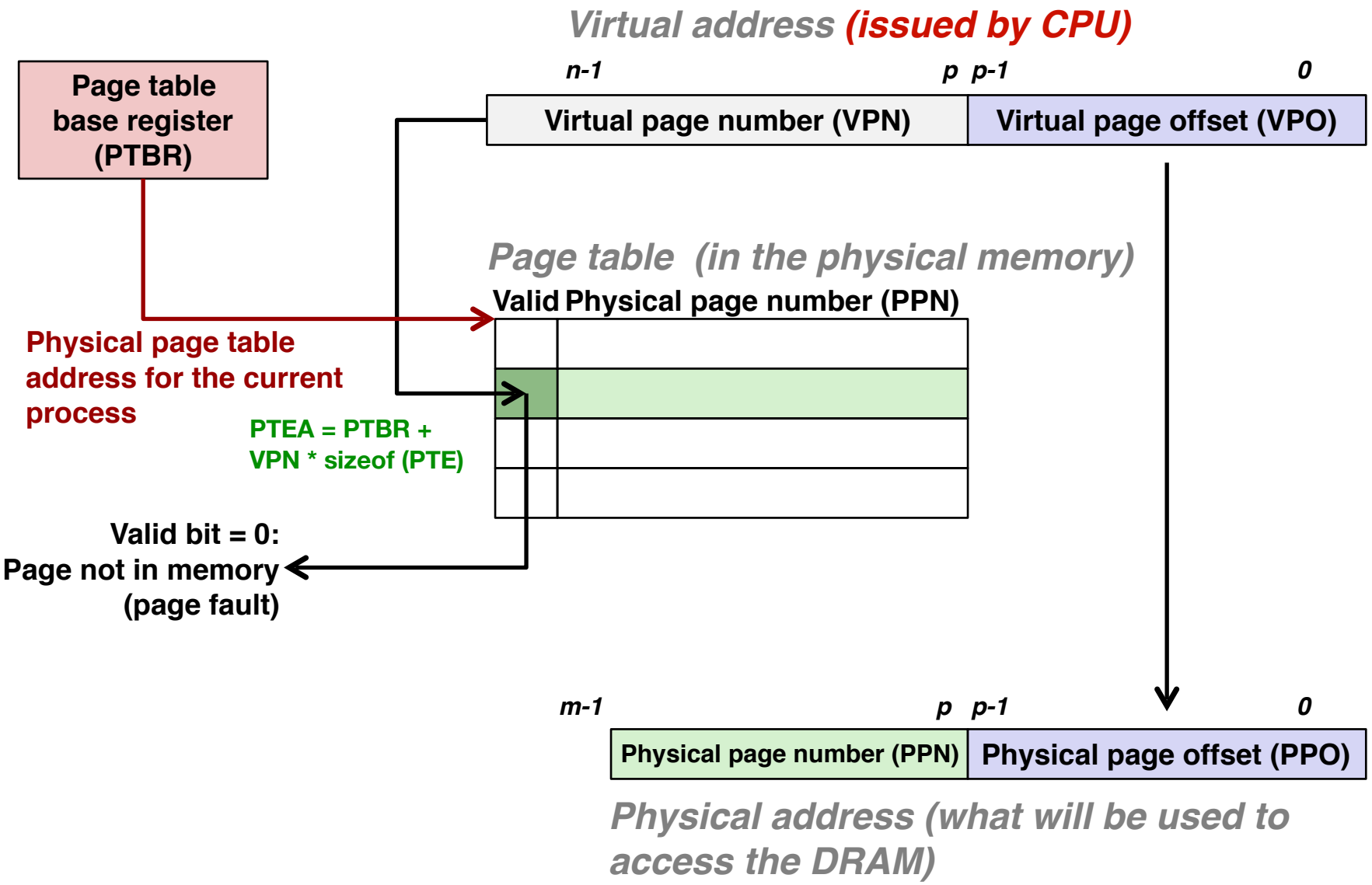

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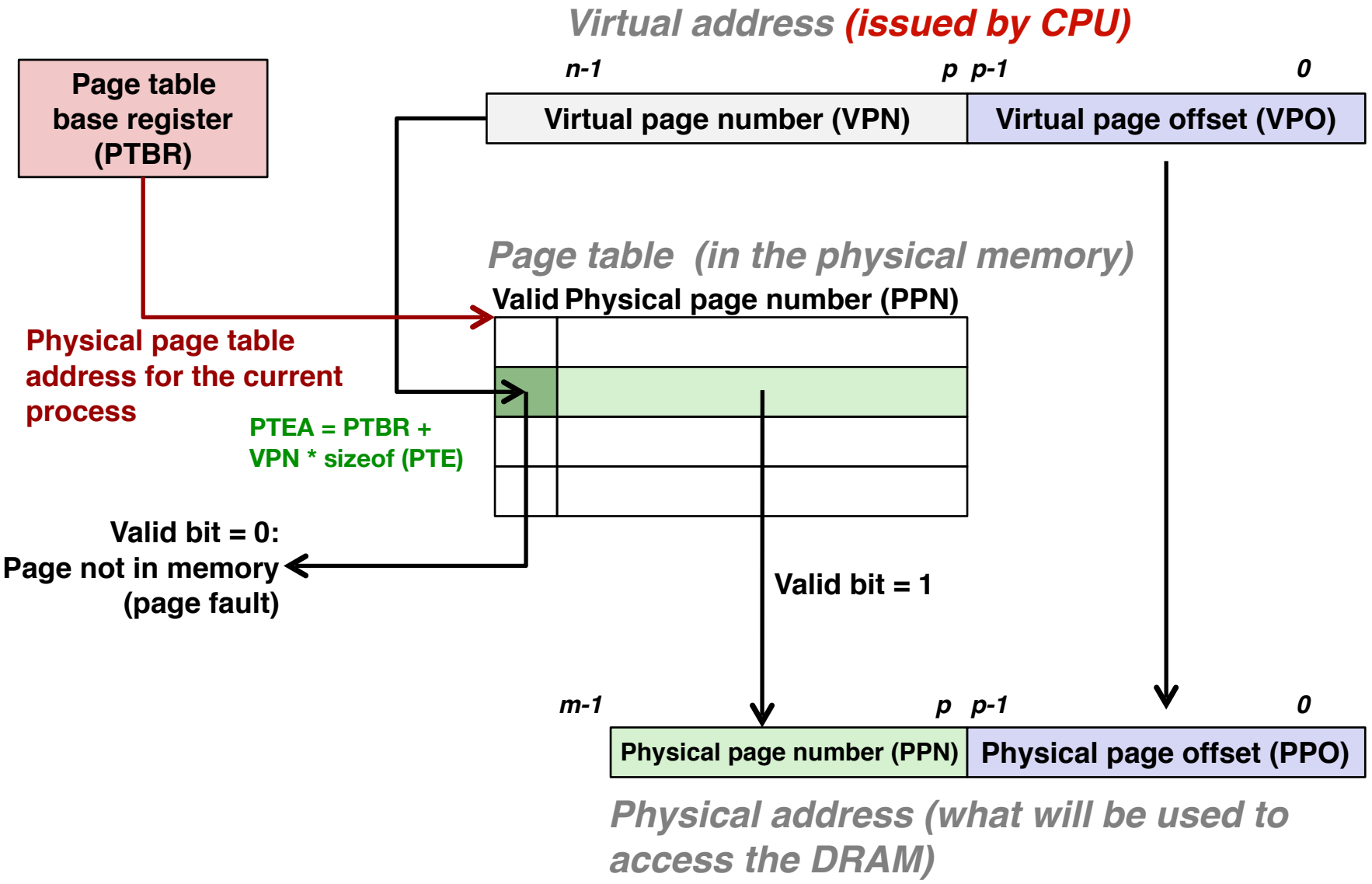
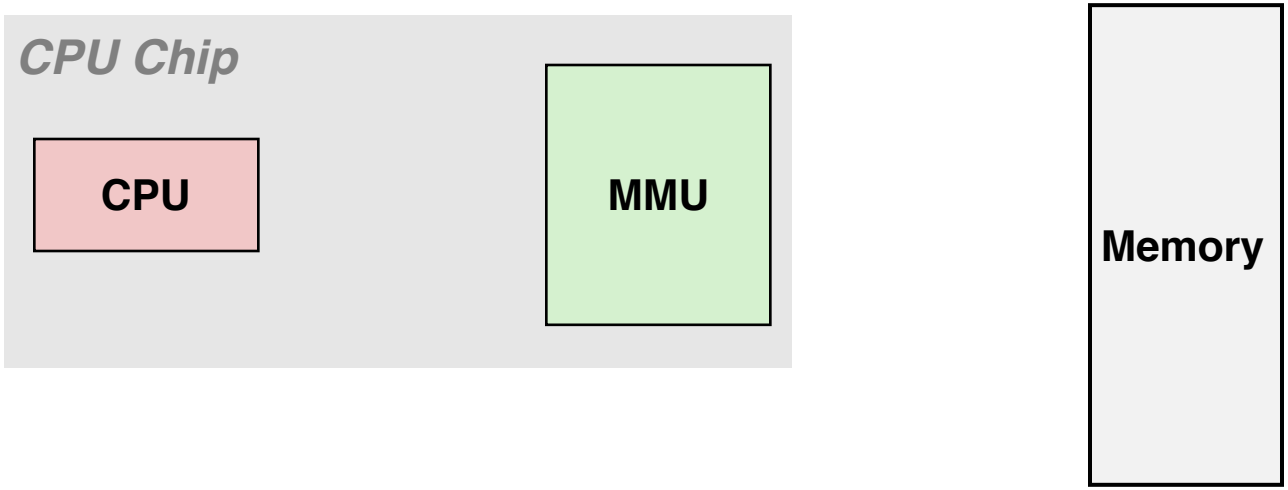


Address Translation: Page Hit



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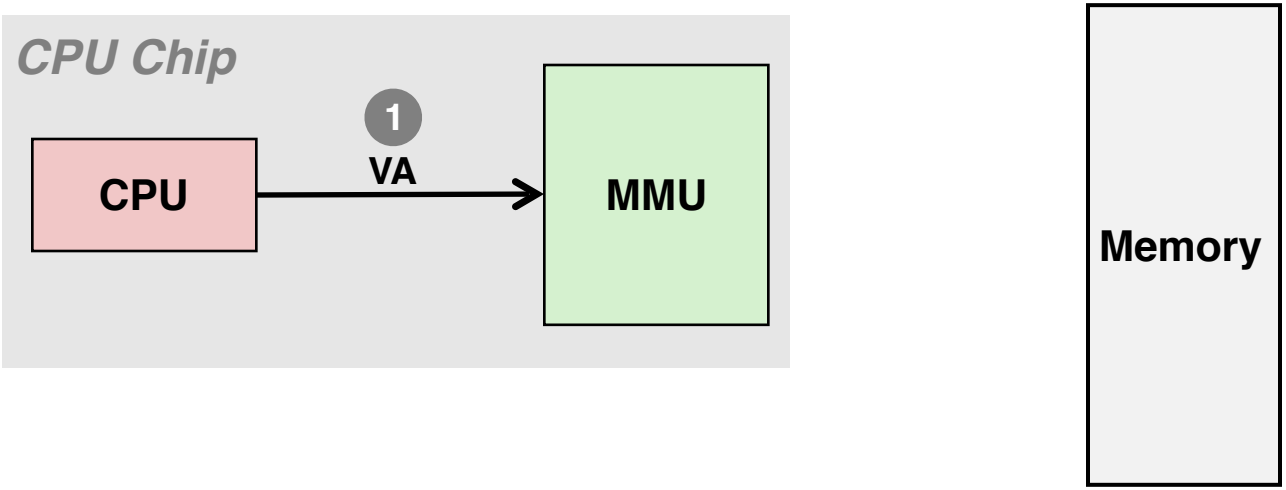

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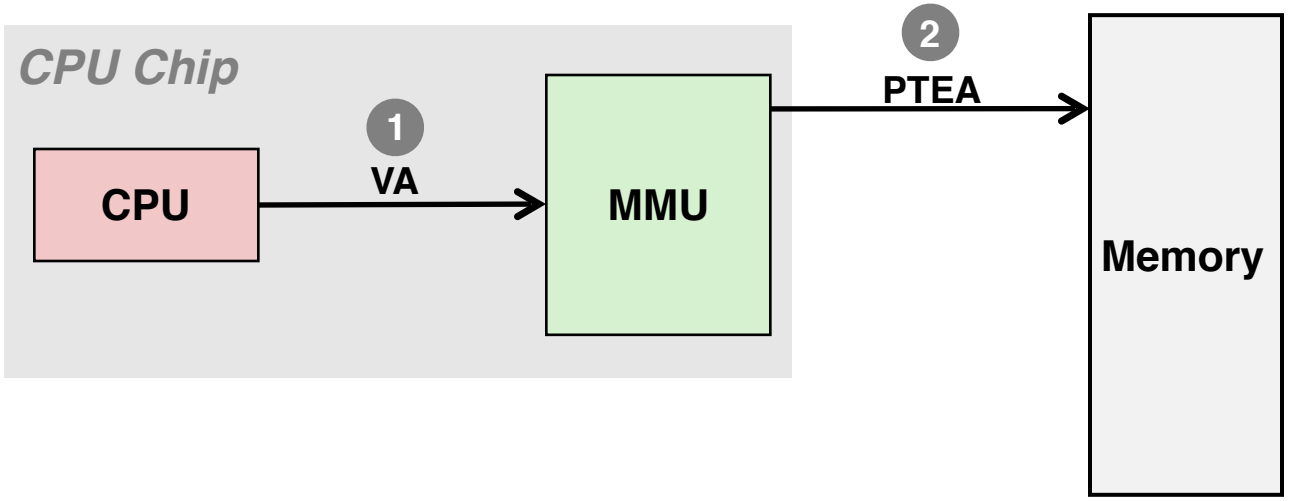

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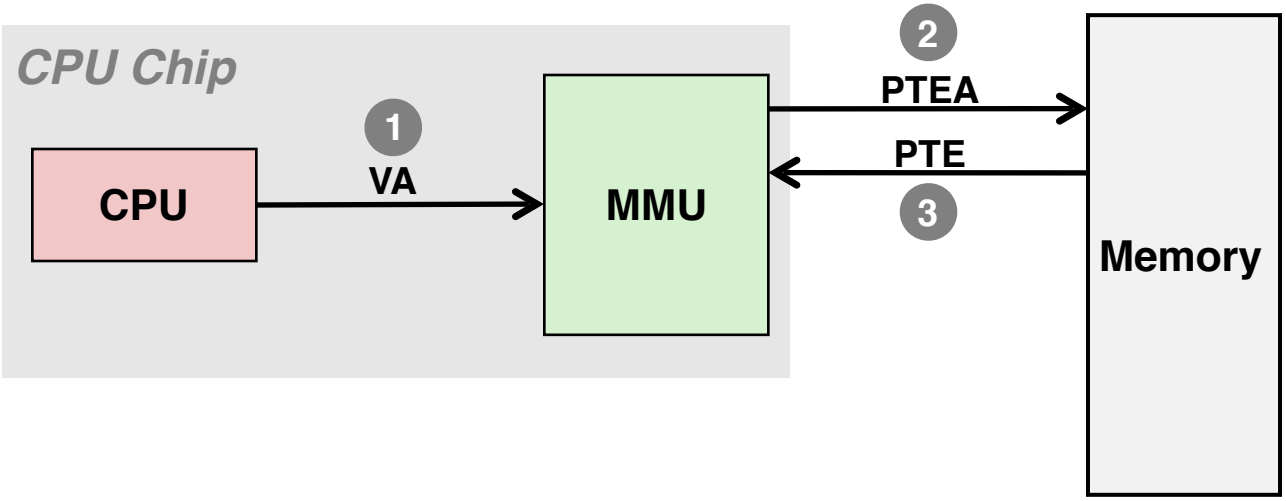

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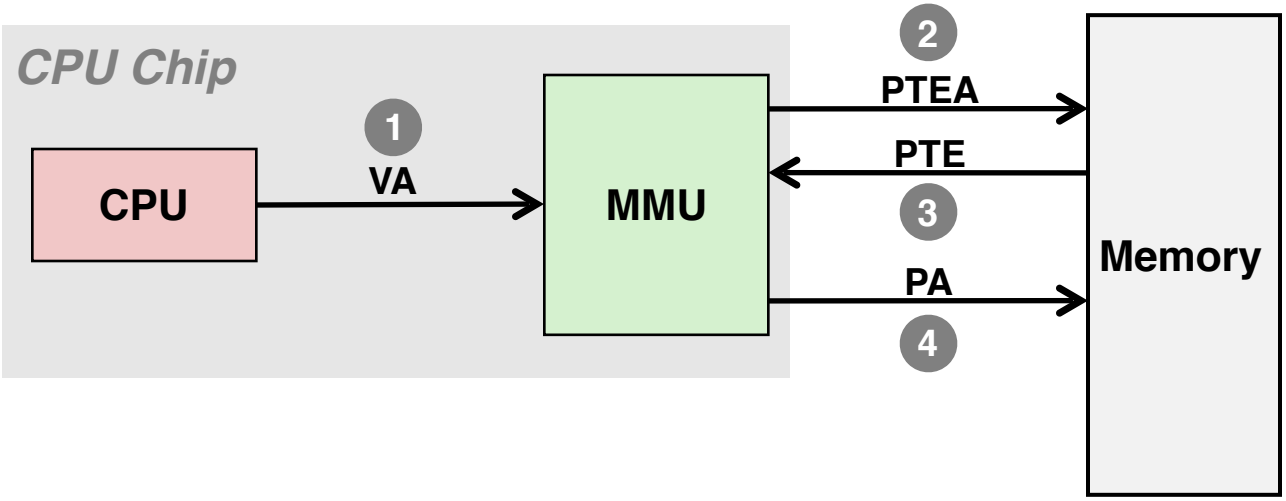

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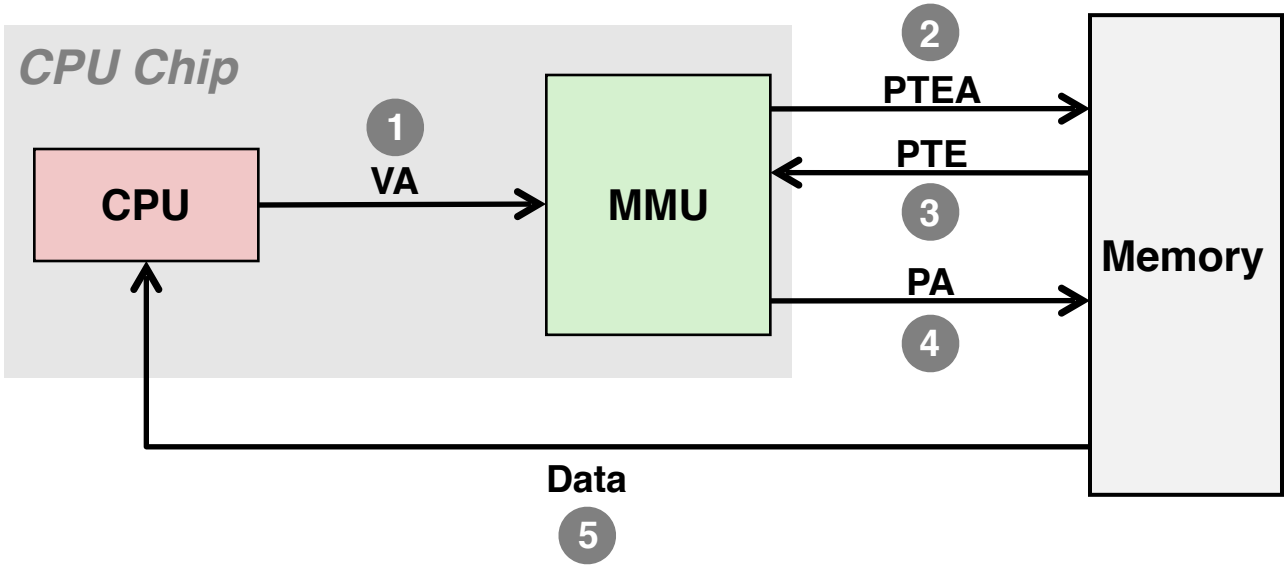

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2-3) MMU fetches PTE from page table in memory

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5) Cache/memory sends data word to processor

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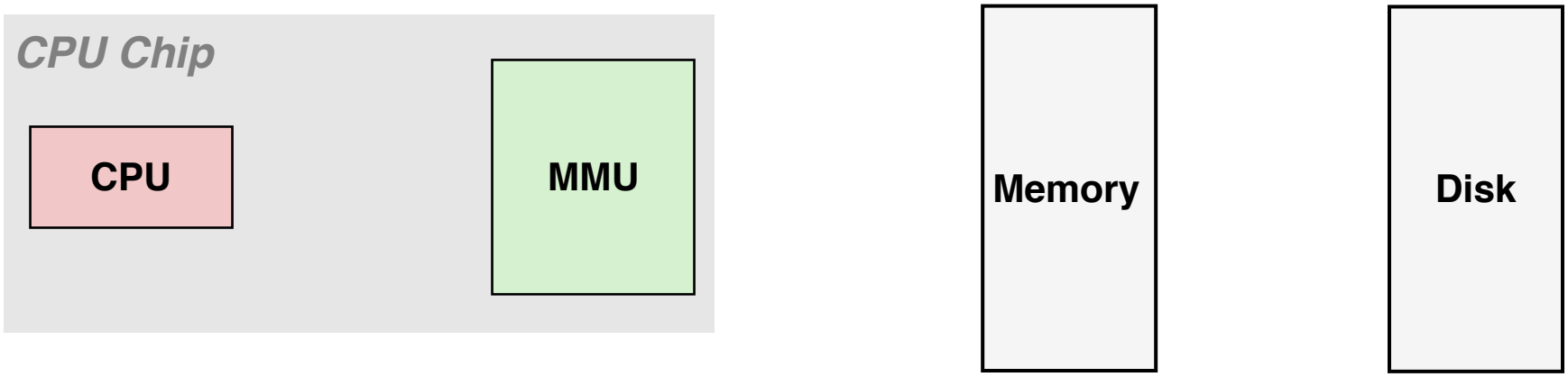

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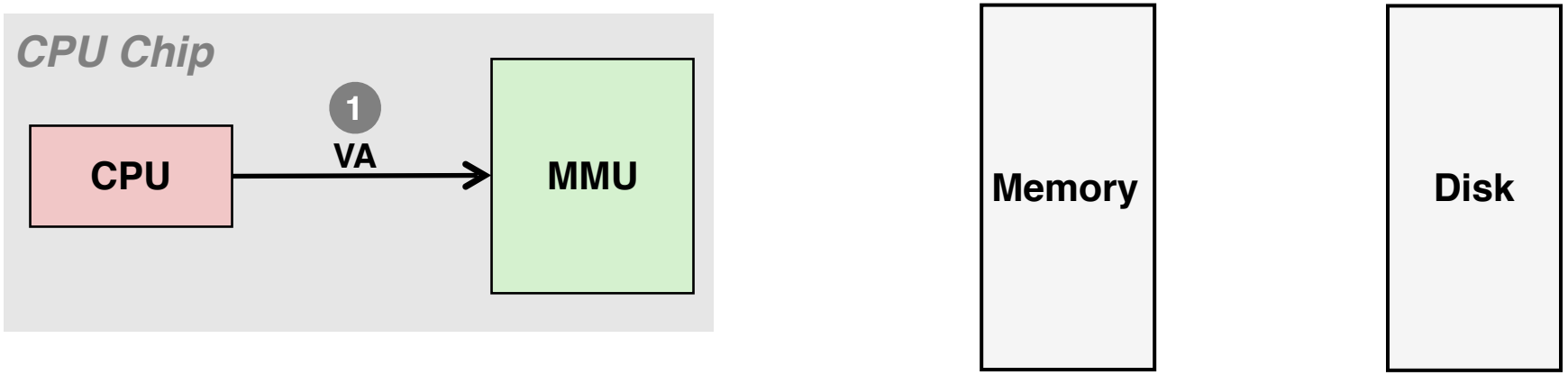

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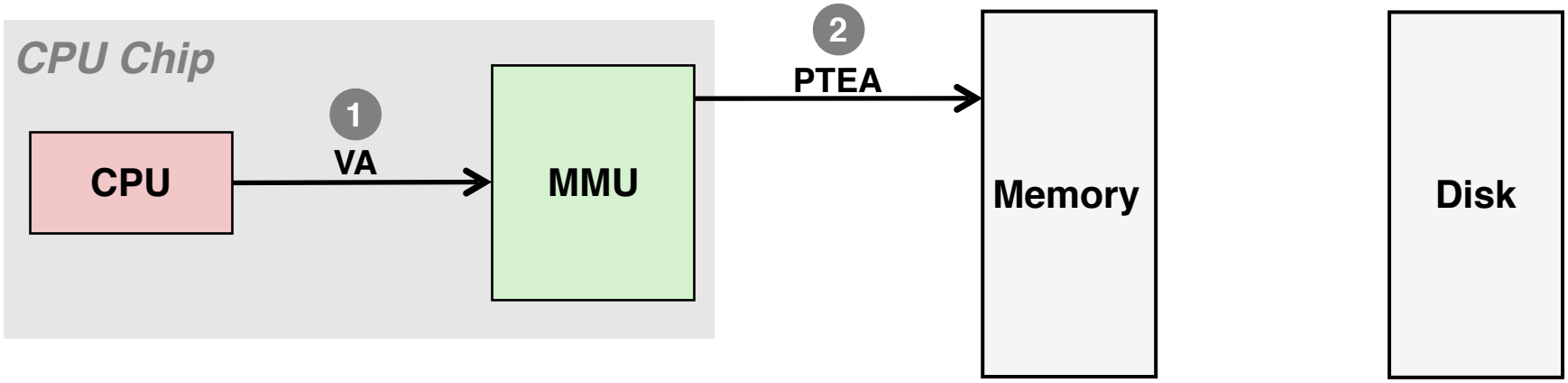

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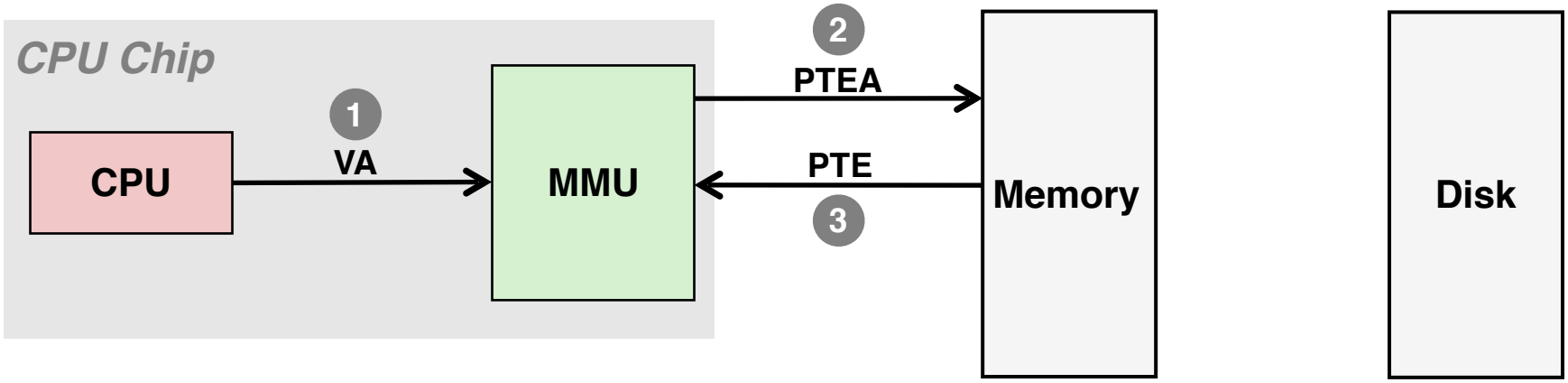

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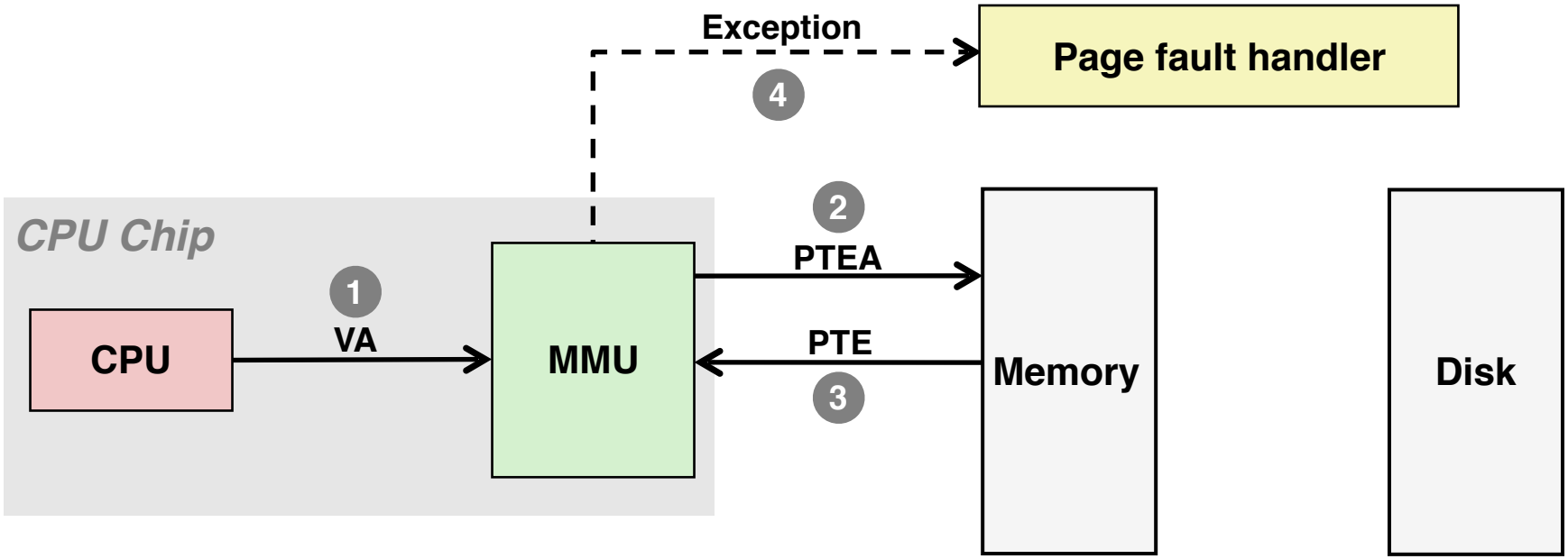

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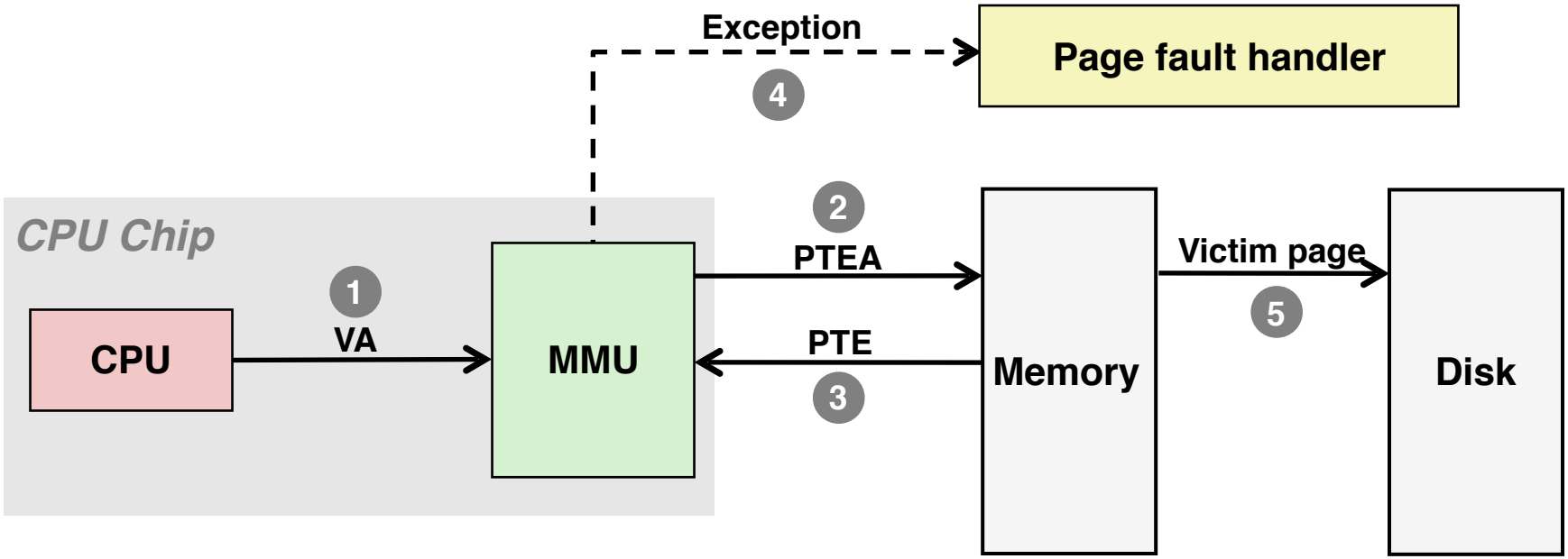

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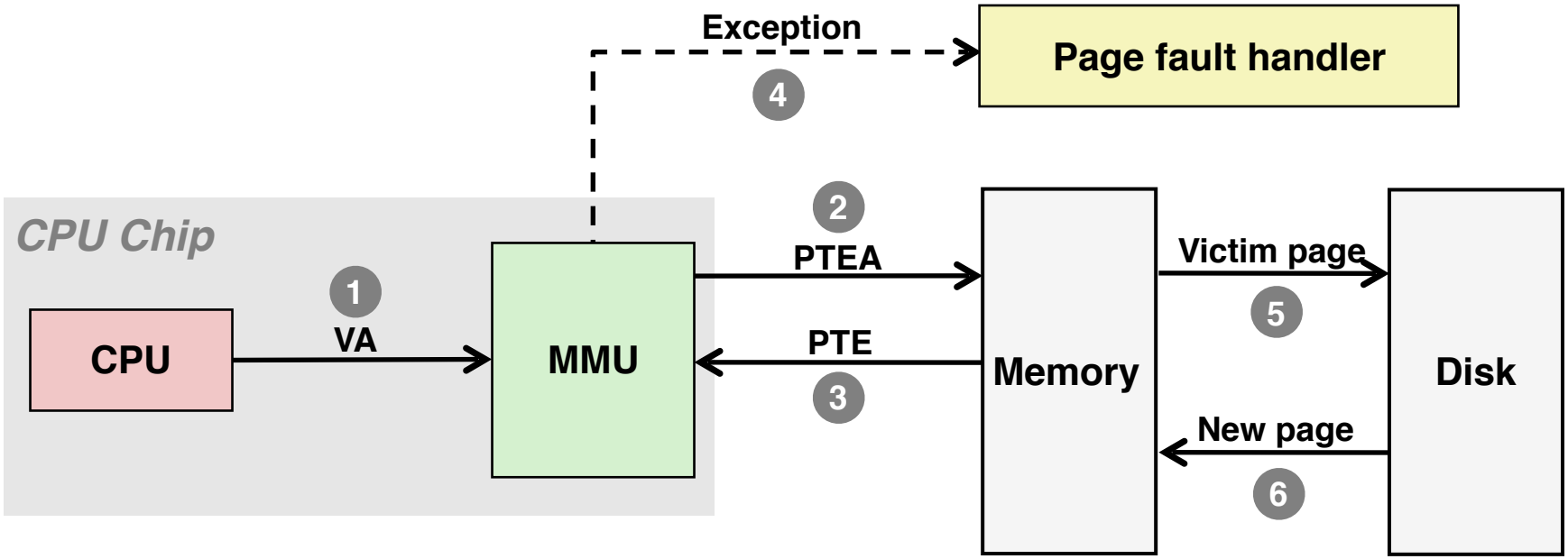

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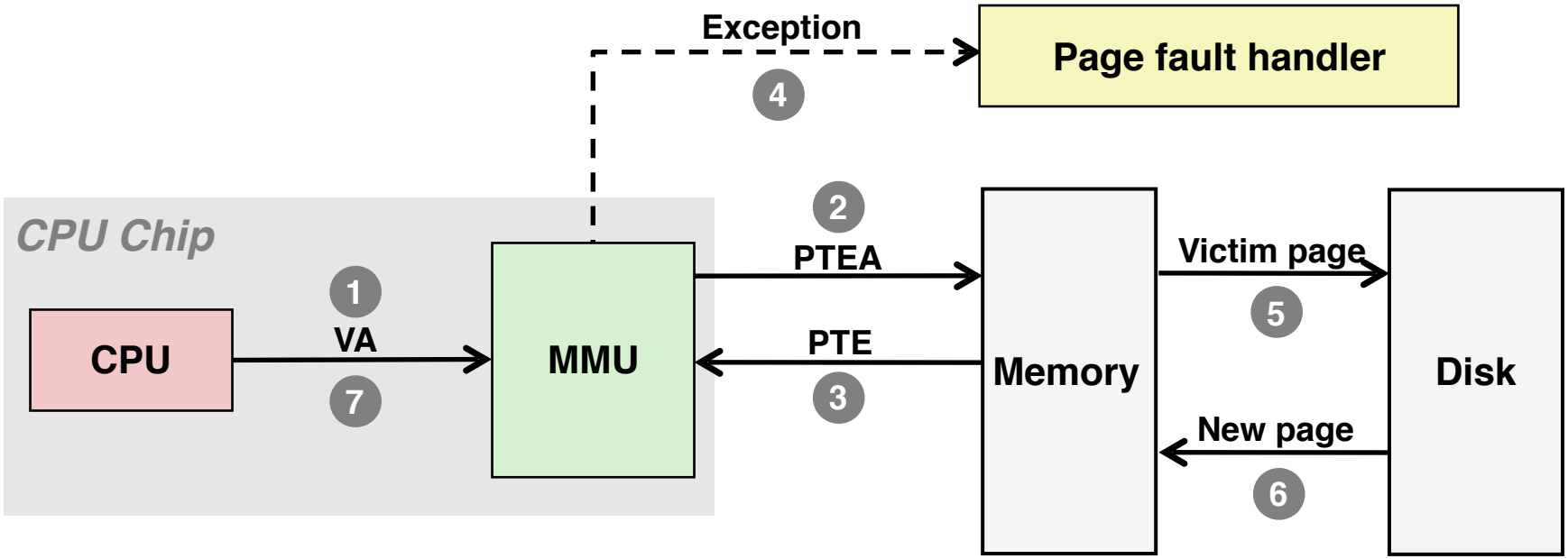

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7) Handler returns to original process, restarting faulting instruction

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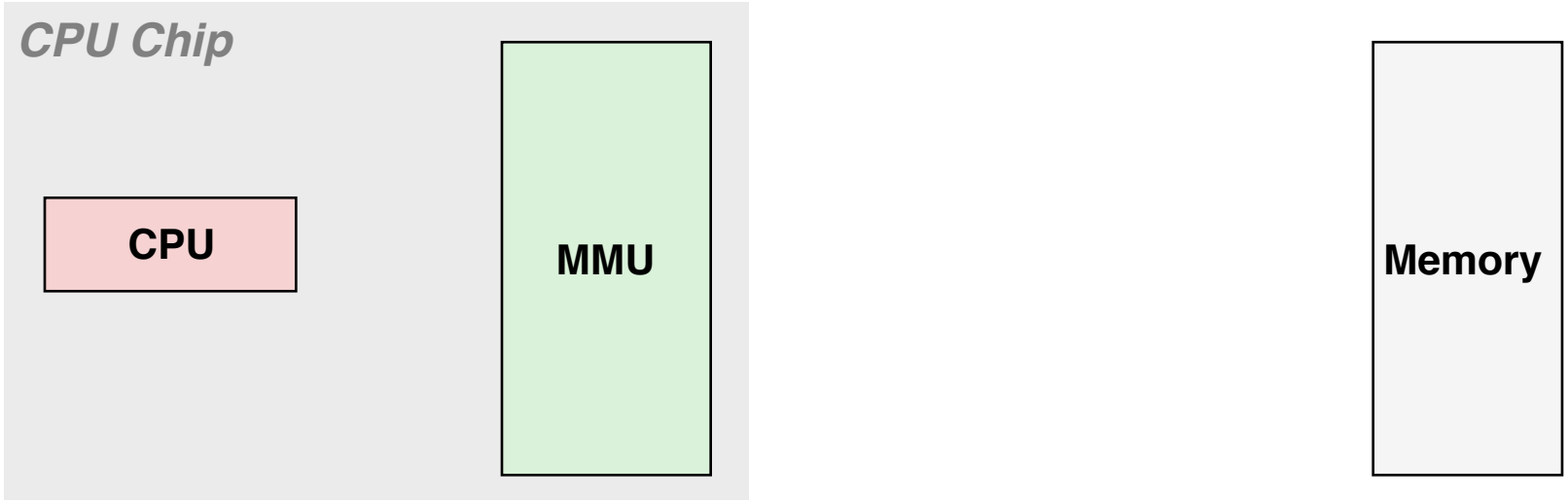
Integrating VM and Cache



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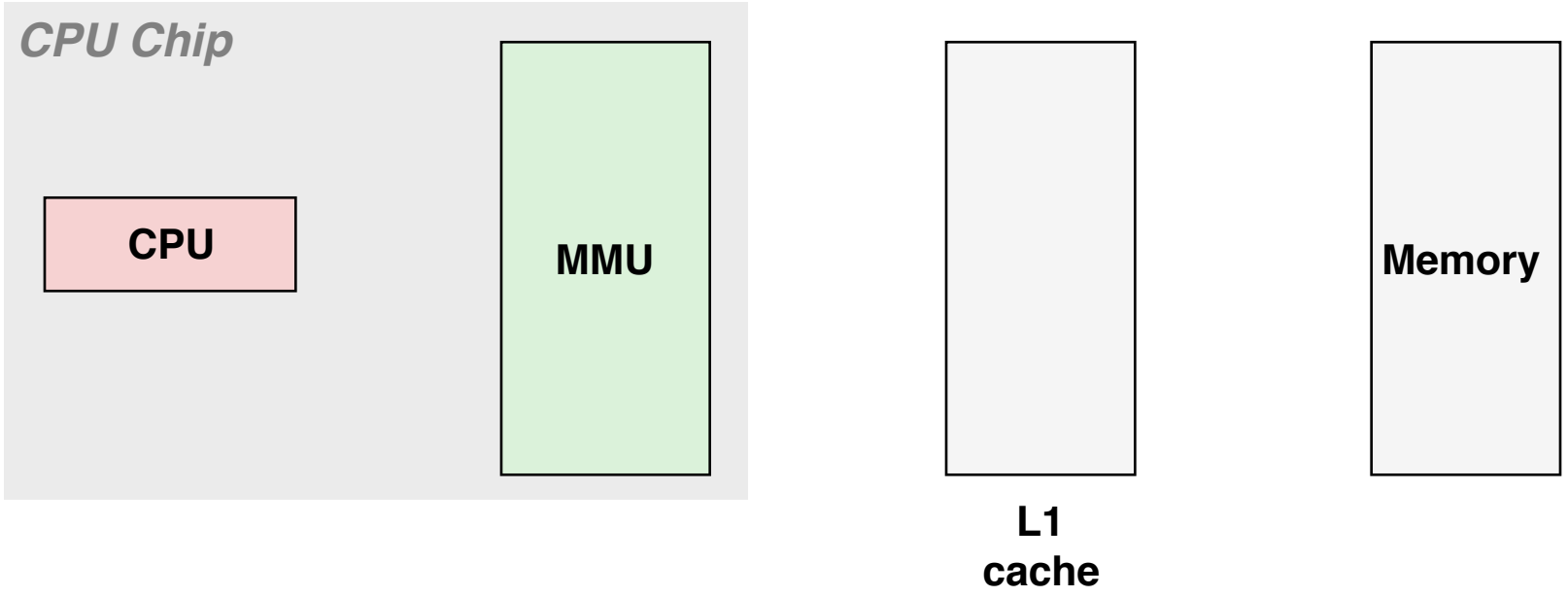

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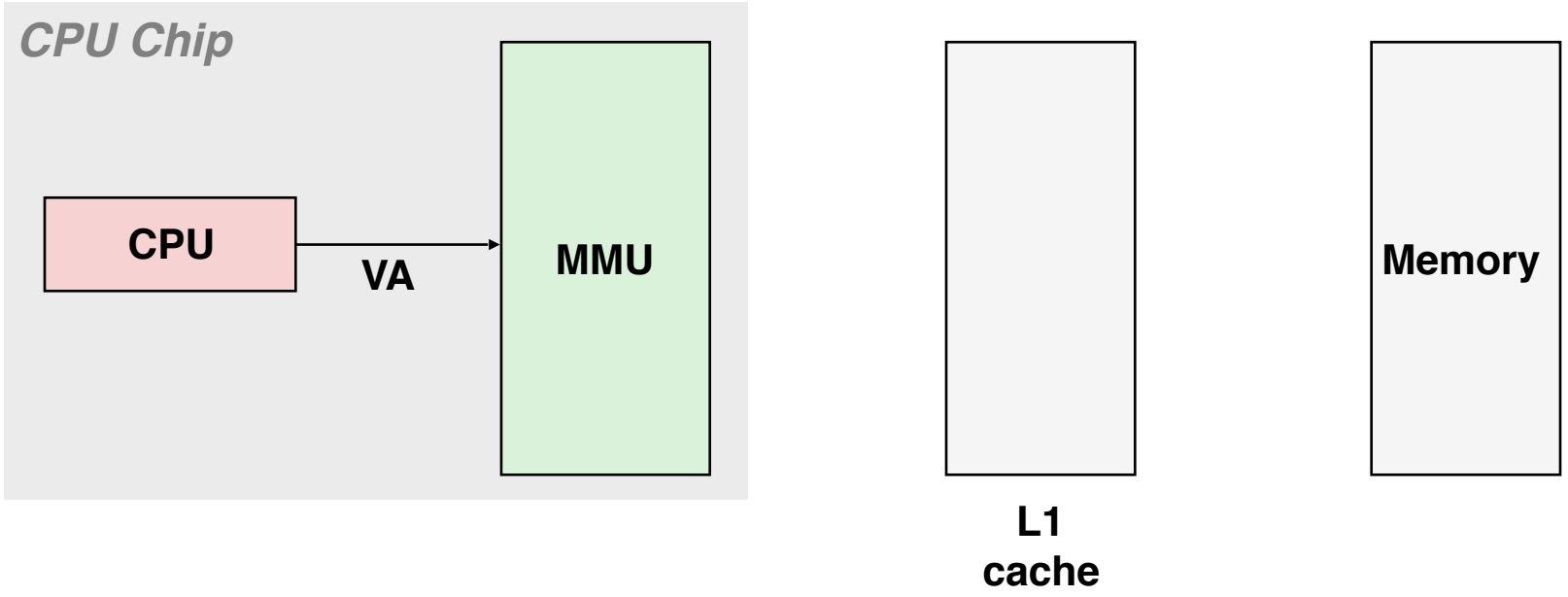

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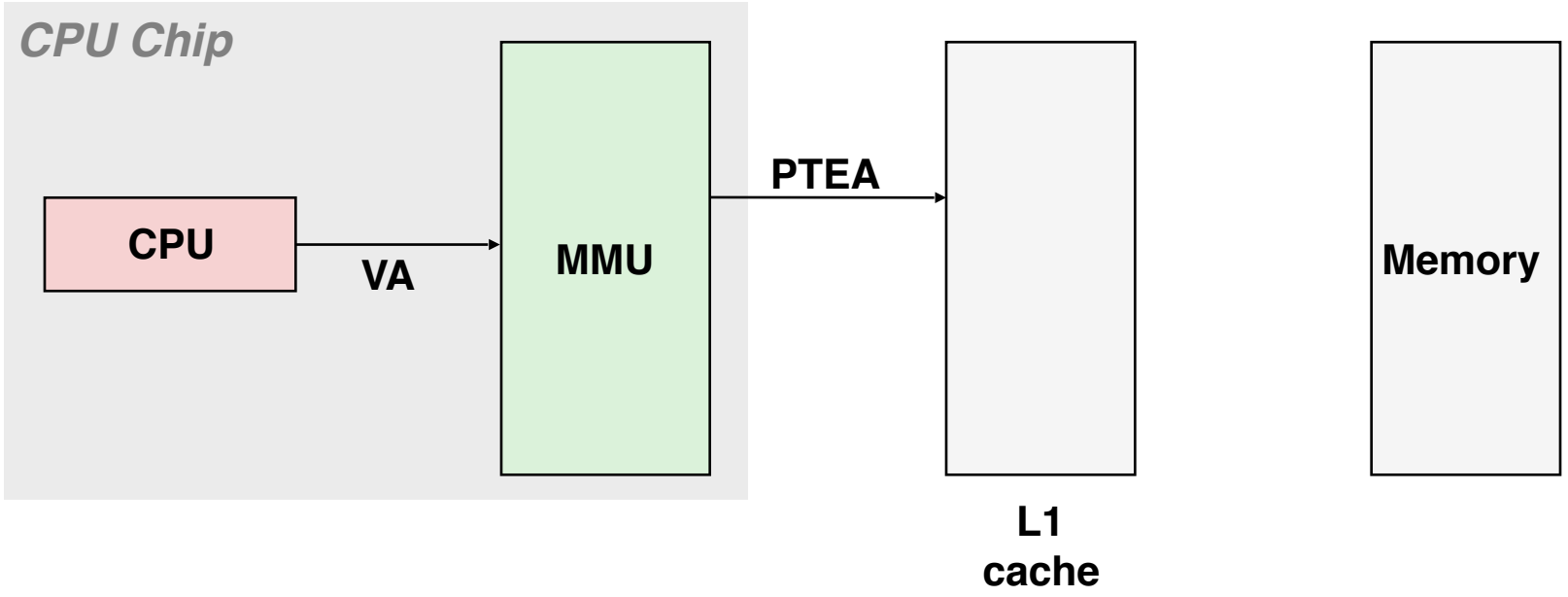

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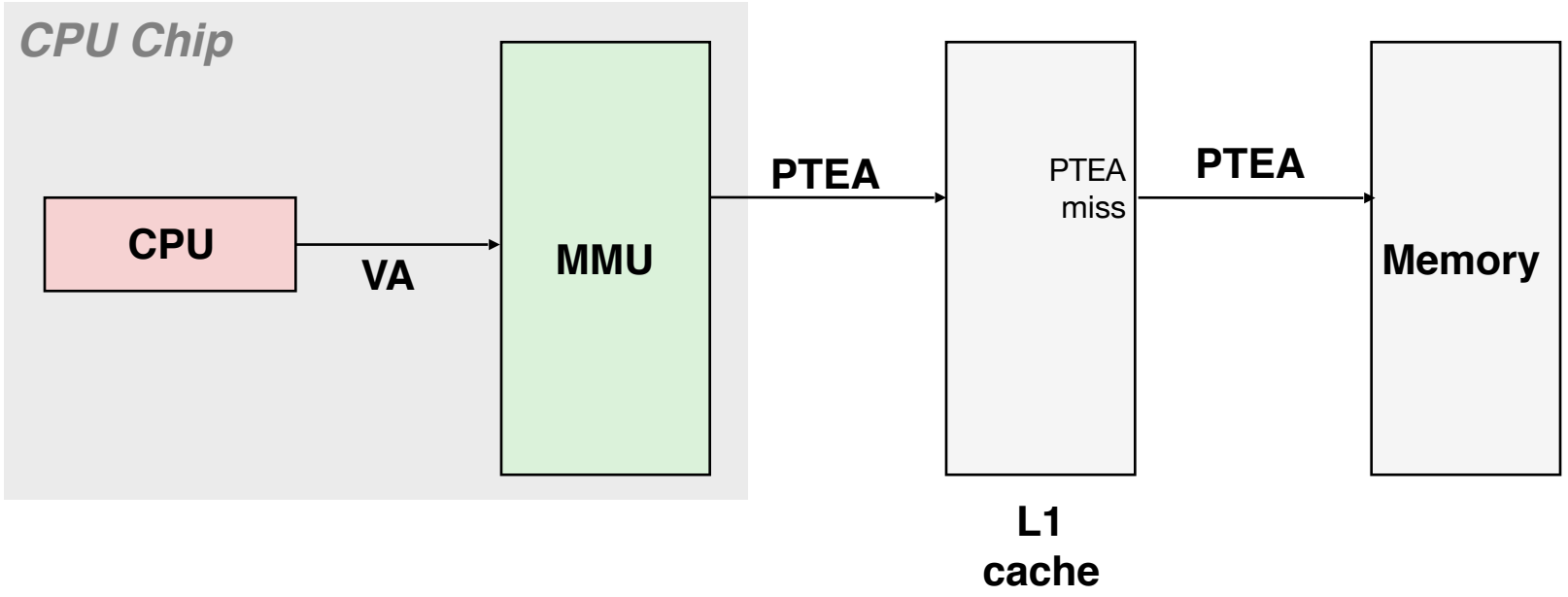

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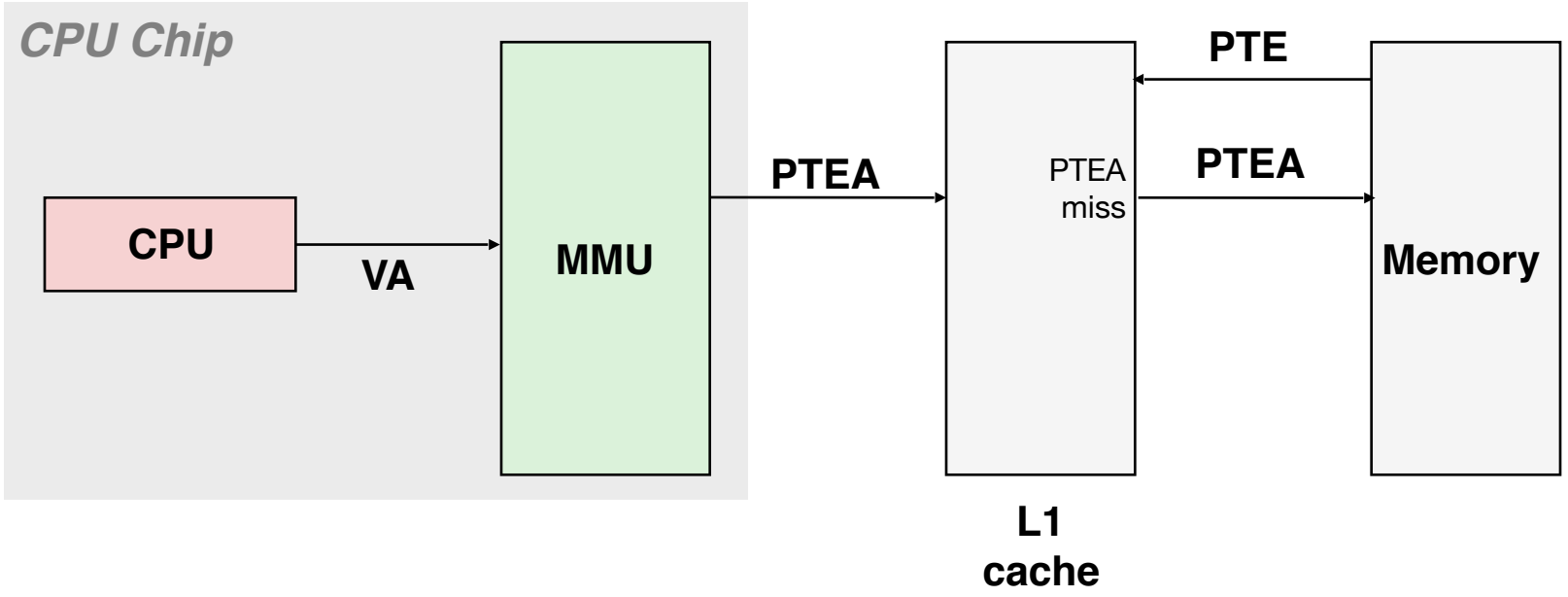

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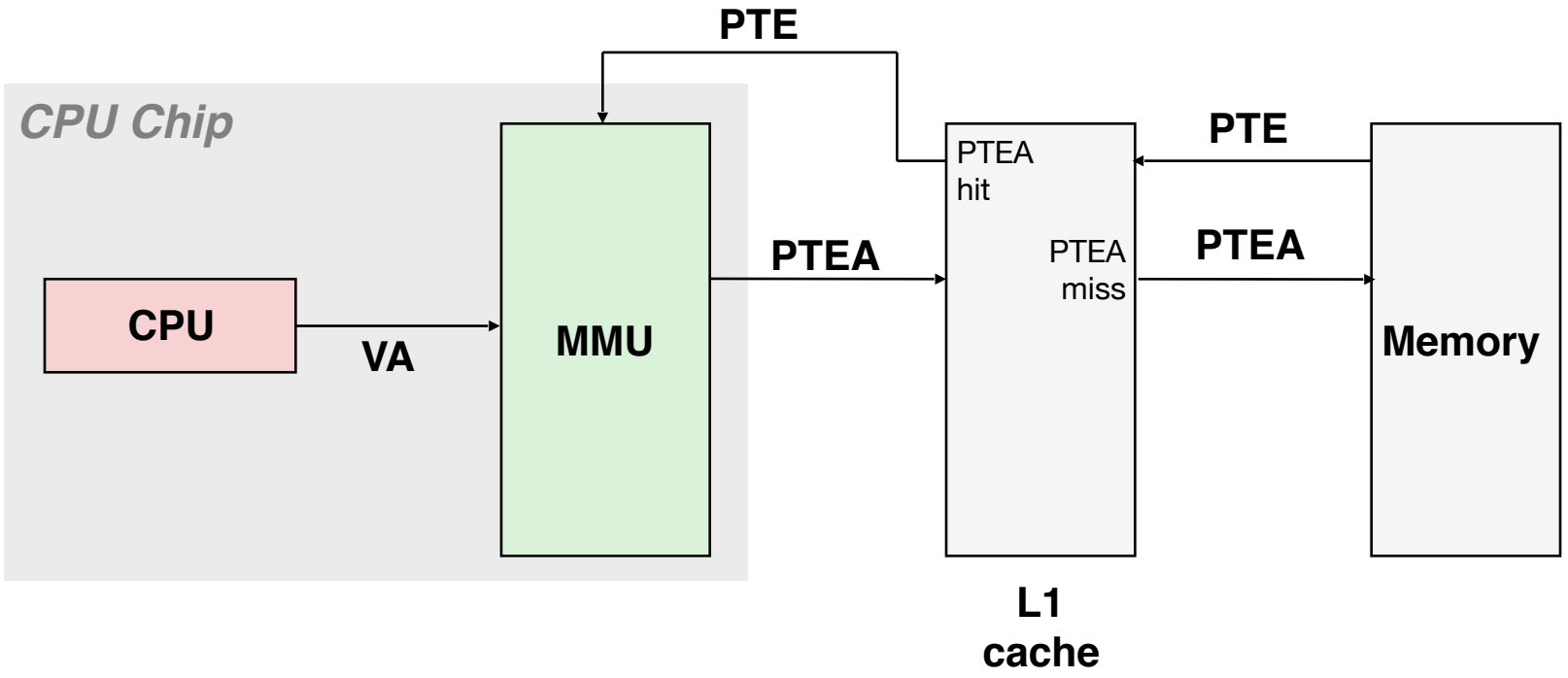

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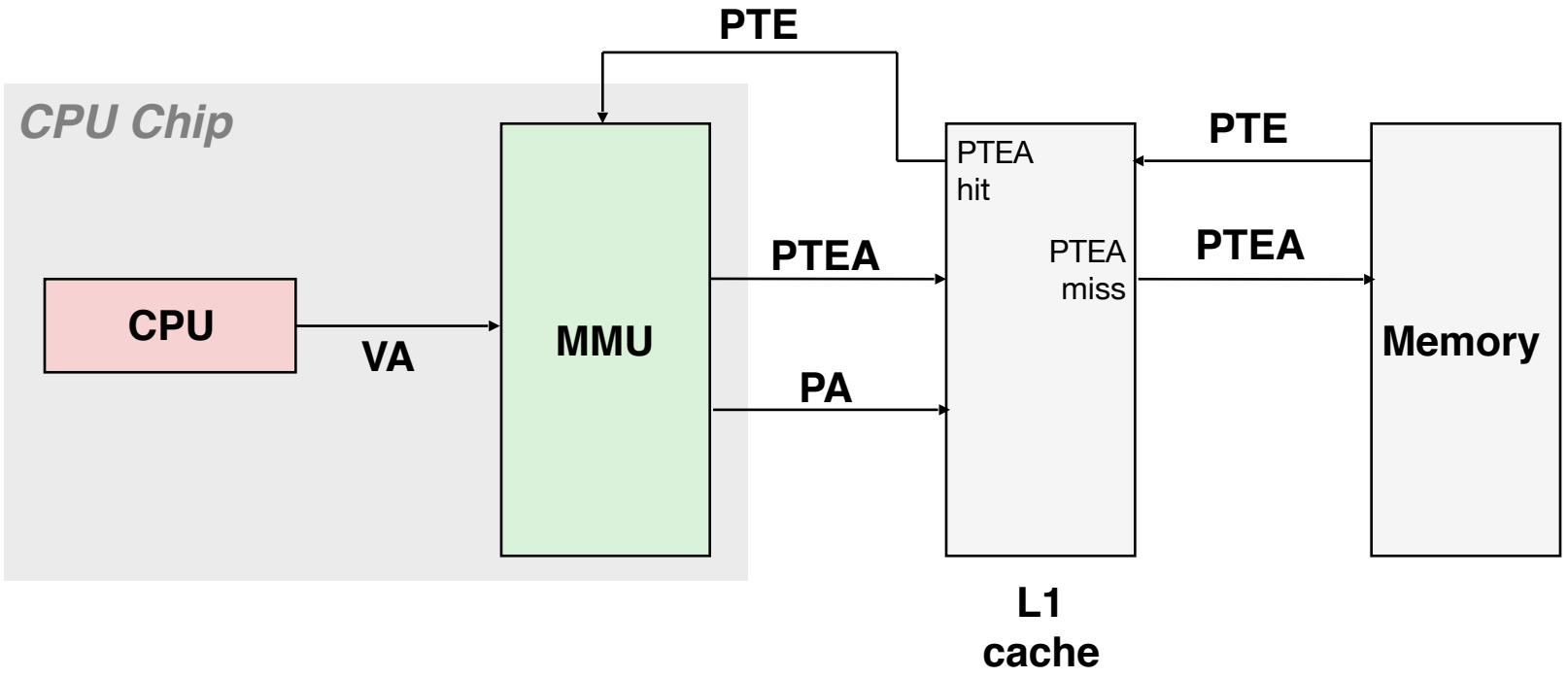

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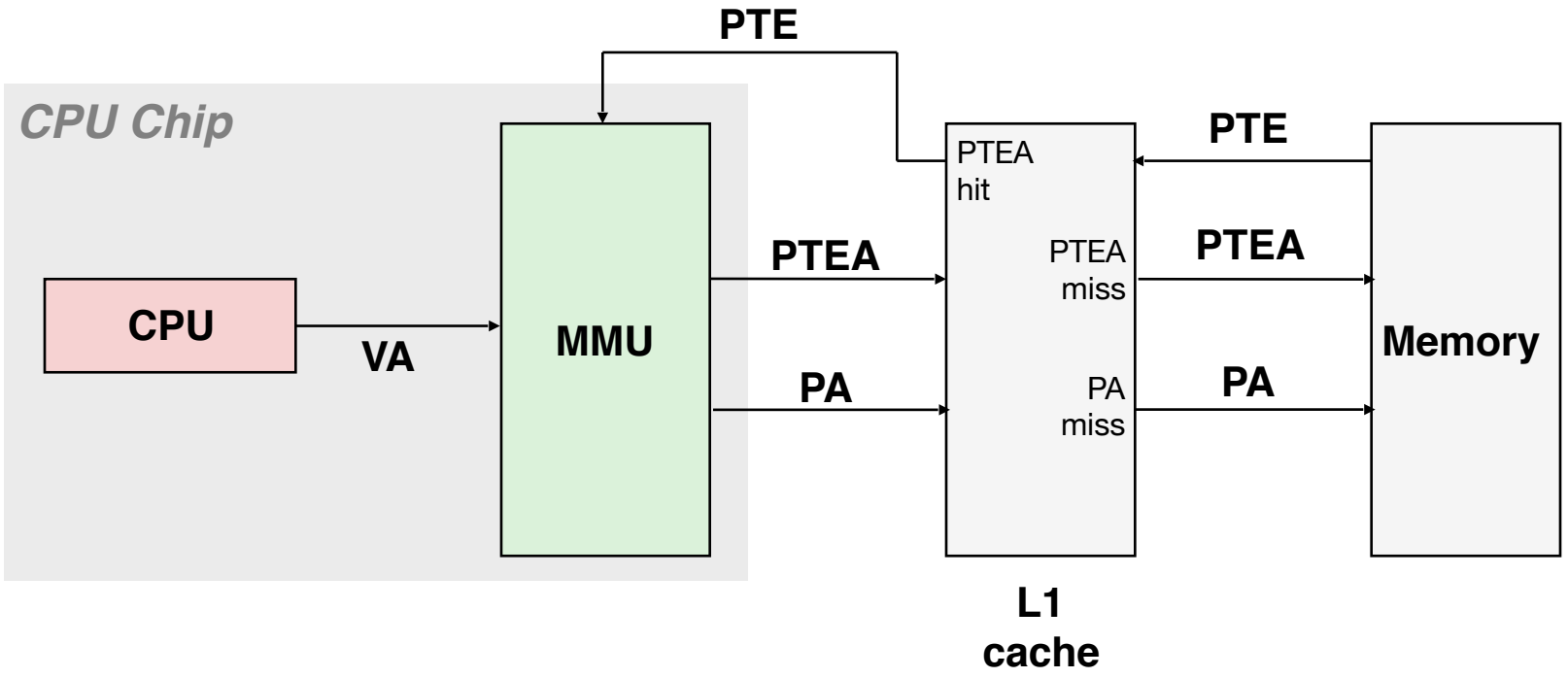

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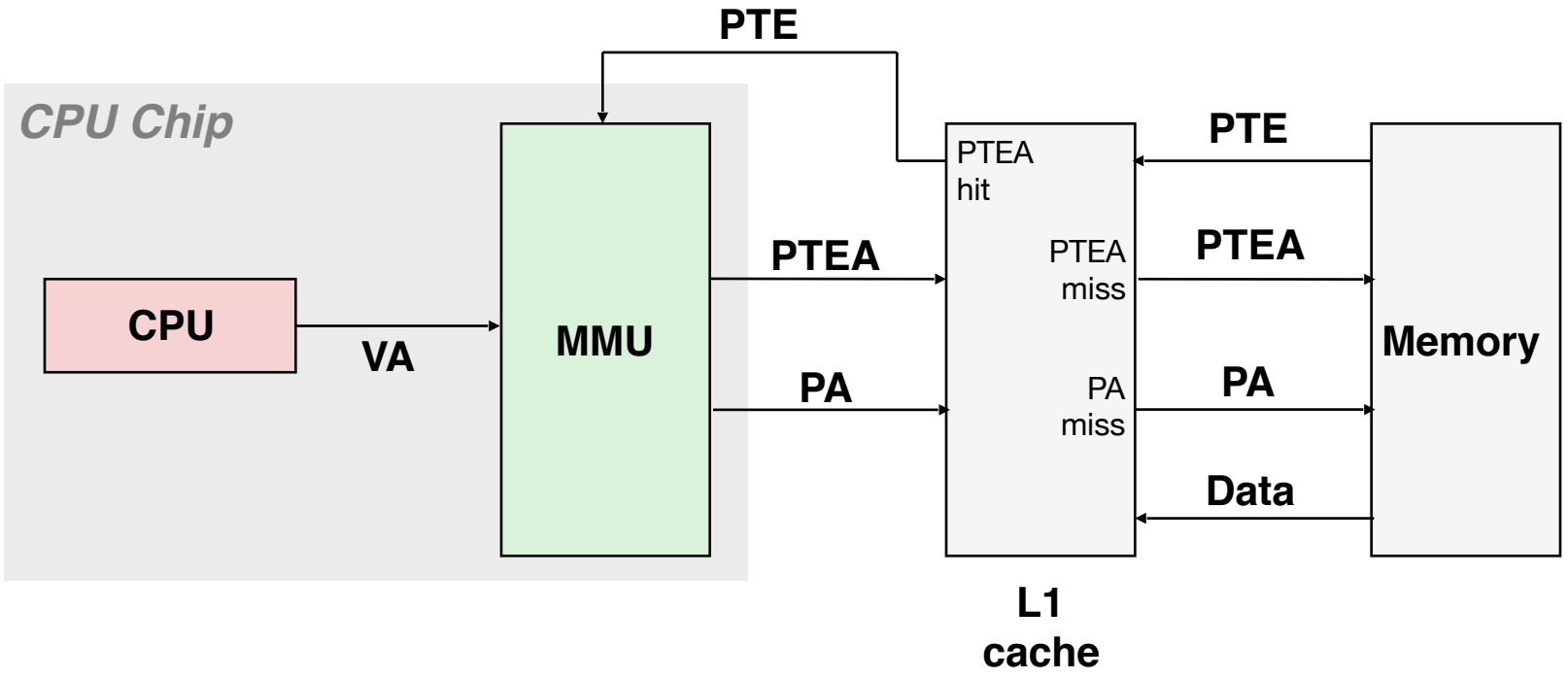

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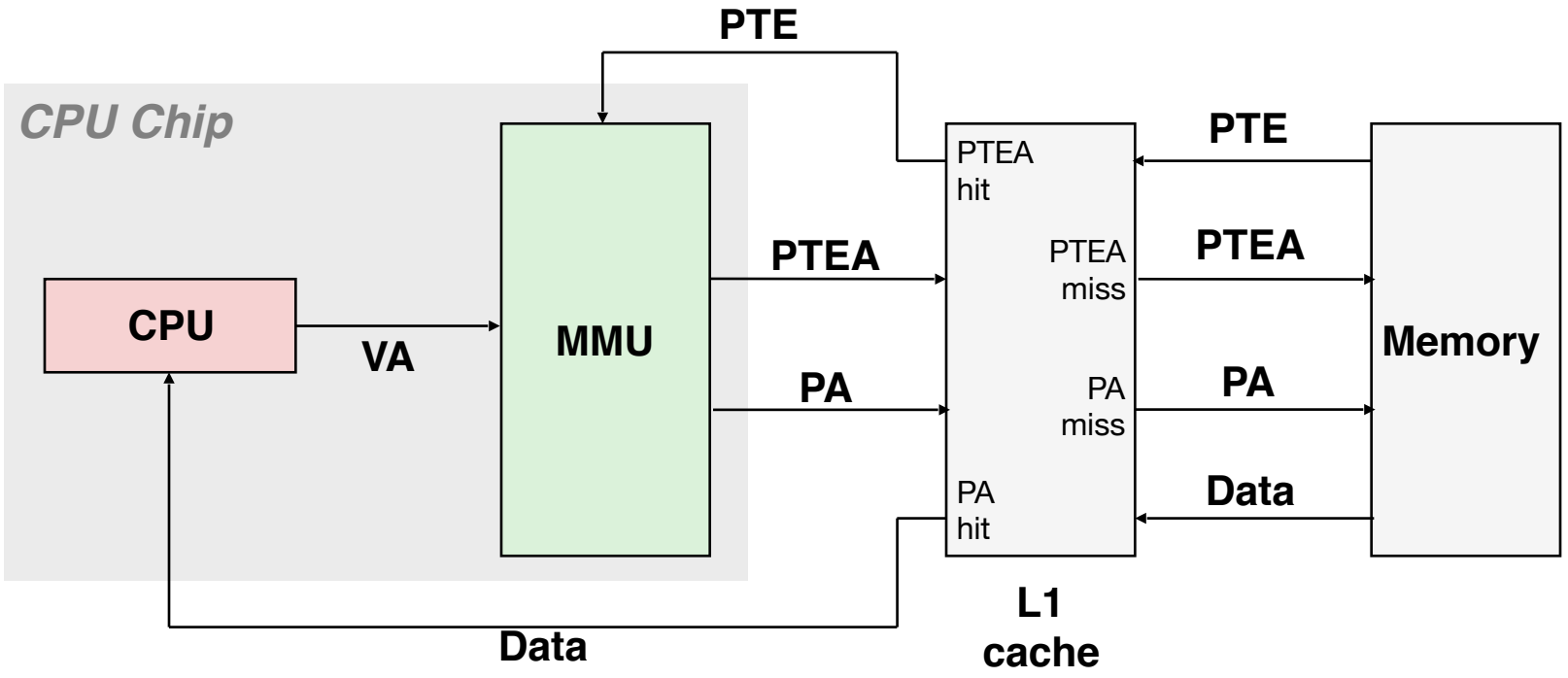

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Today

- Three Virtual Memory Optimizations
  - TLB
  - Virtually-indexed, physically-tagged cache
  - Page the page table (a.k.a., multi-level page table)
- Case-study: Intel Core i7/Linux example

Speeding up Address Translation

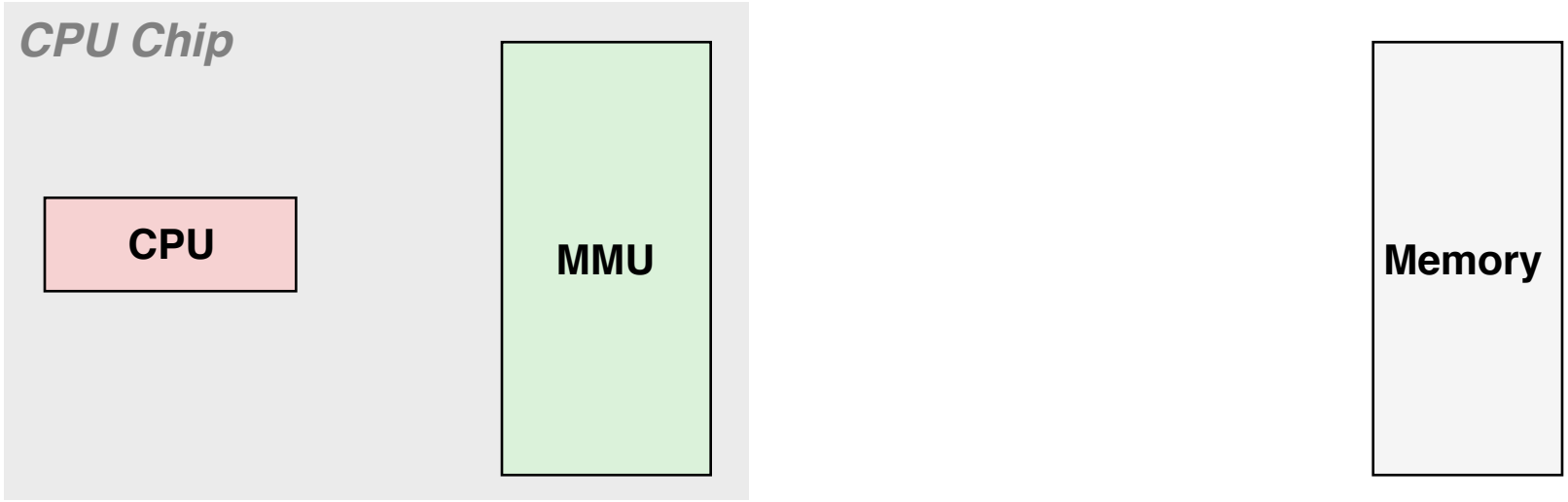
Speeding up Address Translation

- Problem: Every memory load/store requires two memory accesses: one for PTE, another for real
  - The PTE access is kind of an overhead
  - Can we speed it up?

Speeding up Address Translation

- Problem: Every memory load/store requires two memory accesses: one for PTE, another for real
  - The PTE access is kind of an overhead
  - Can we speed it up?
- Page table entries (PTEs) are already cached in L1 data cache like any other memory data. But:
  - PTEs may be evicted by other data references
  - PTE hit still requires a small L1 delay

Recall: Page Table is Cached



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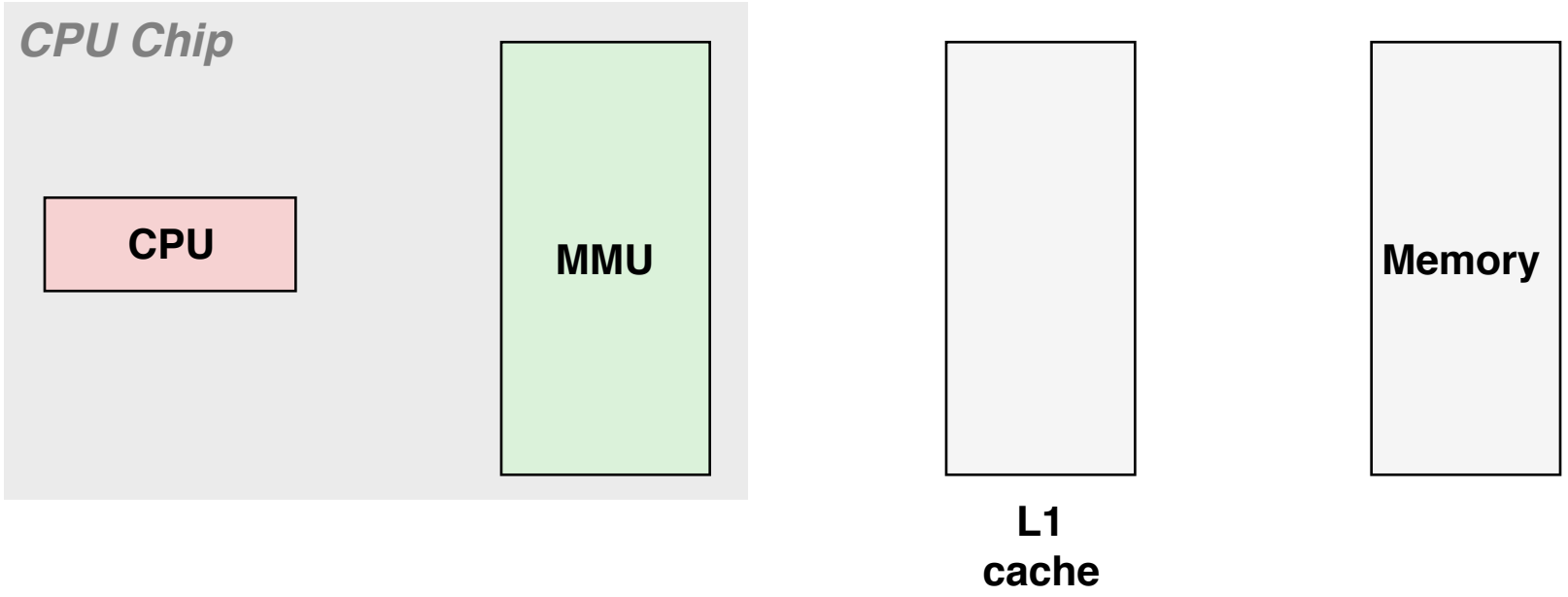

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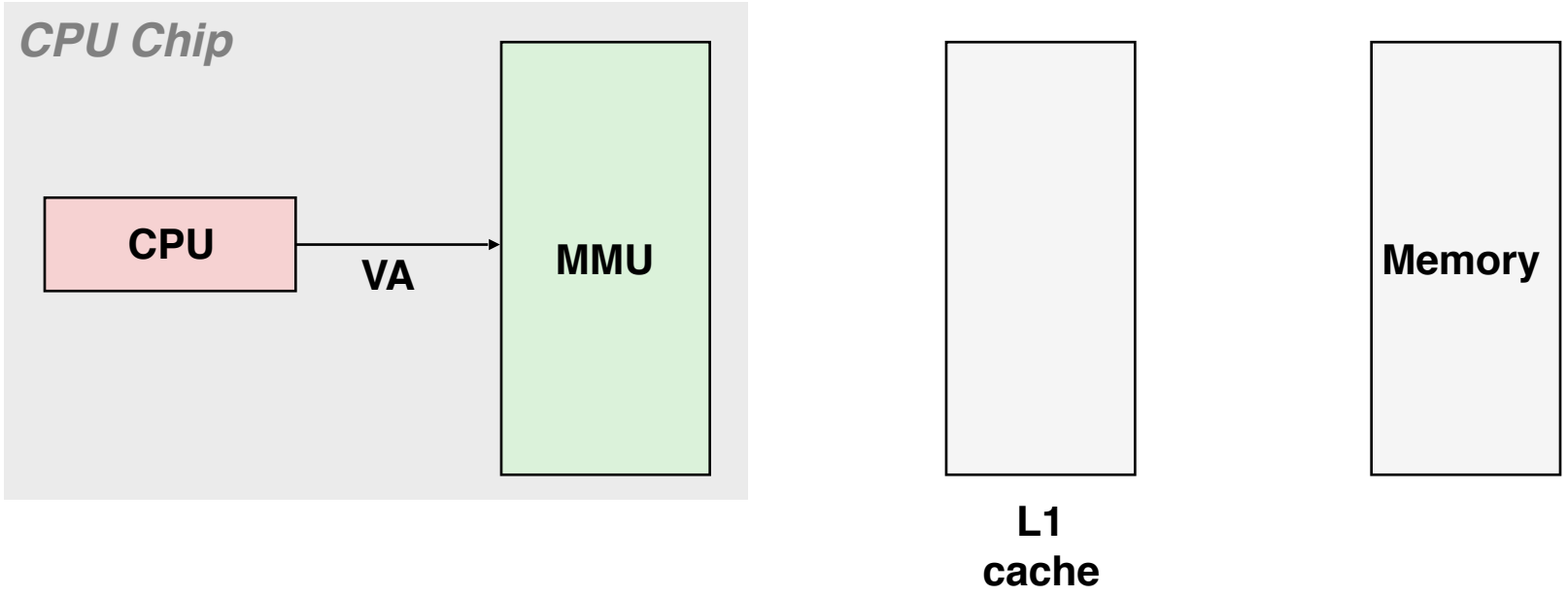

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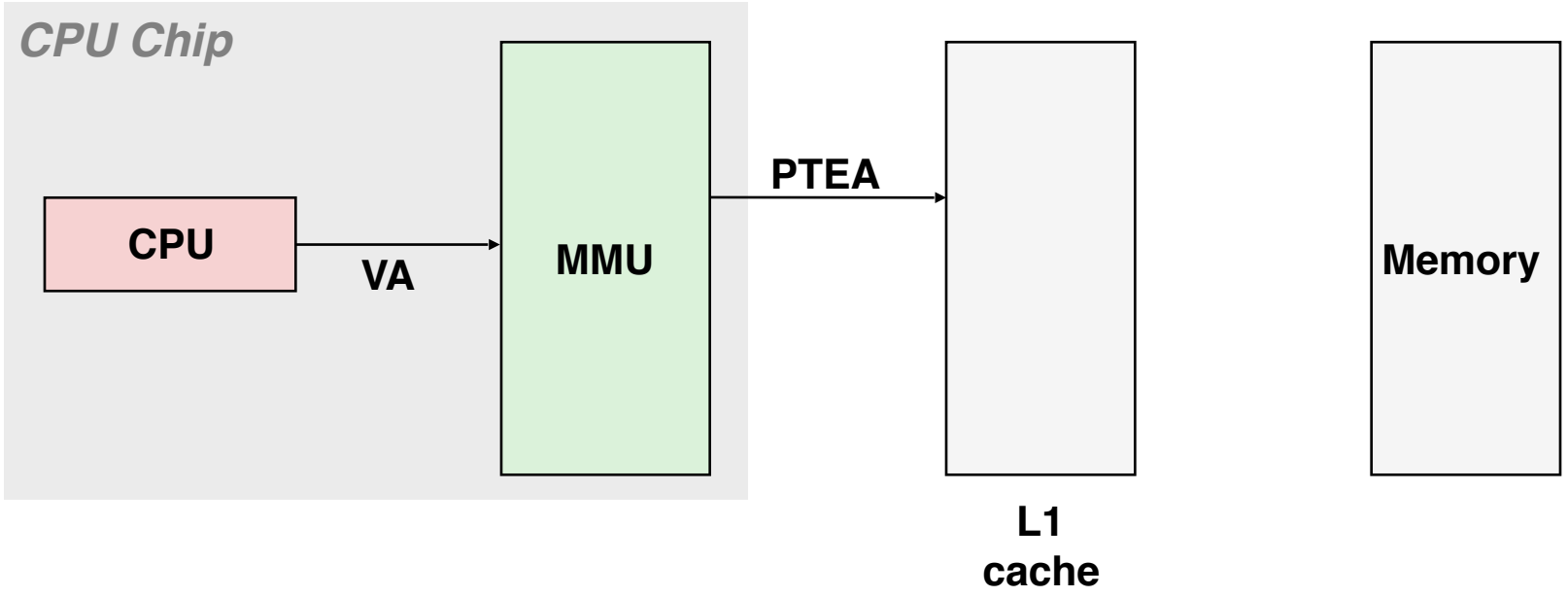

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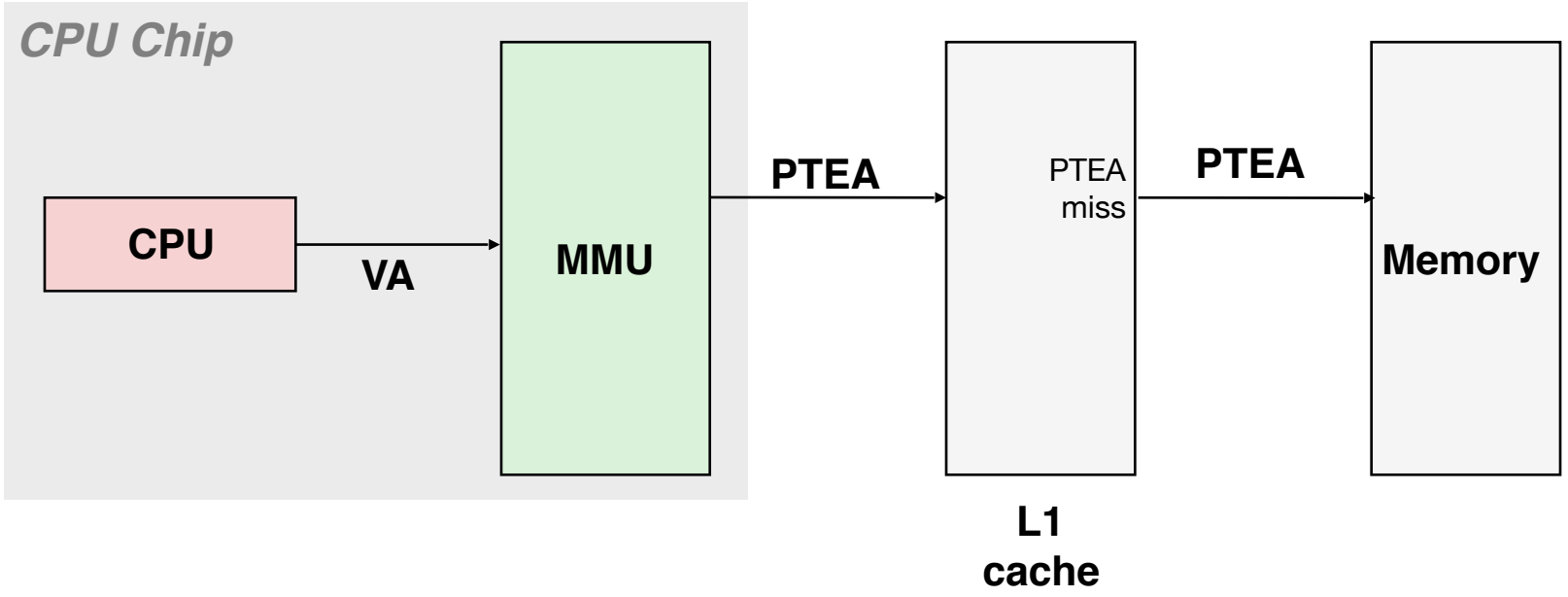

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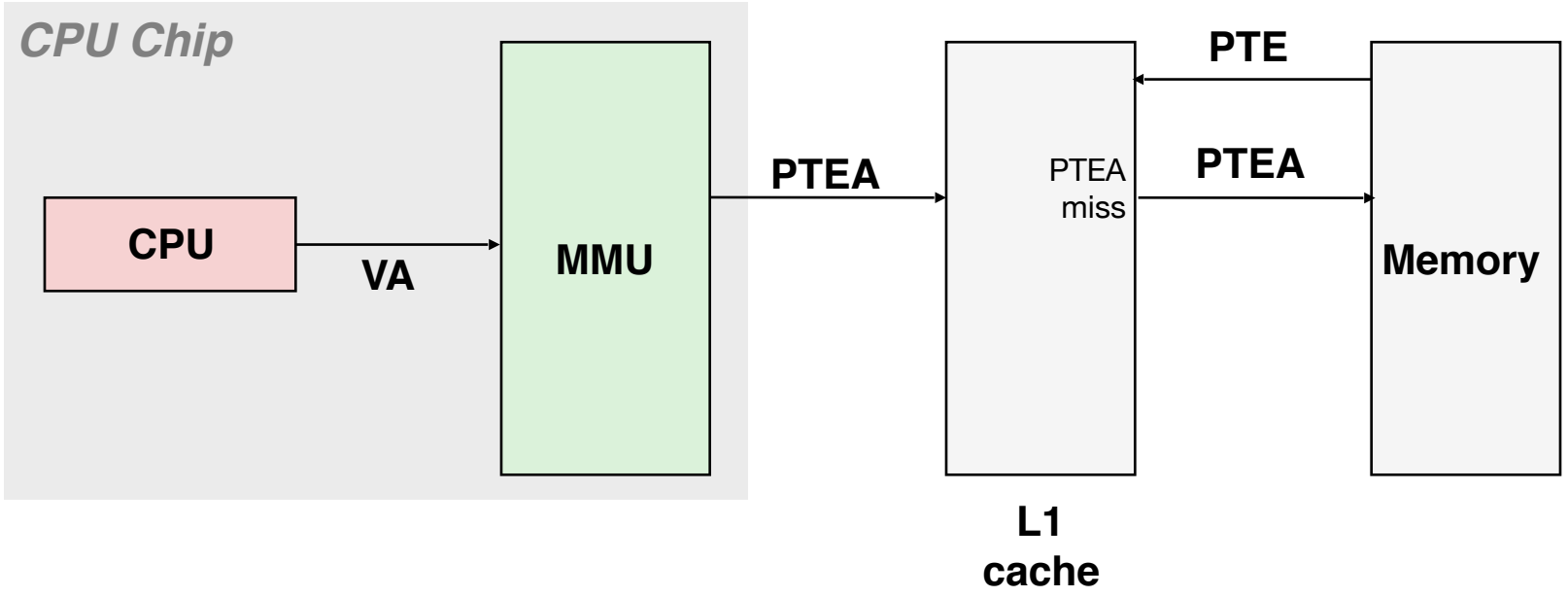

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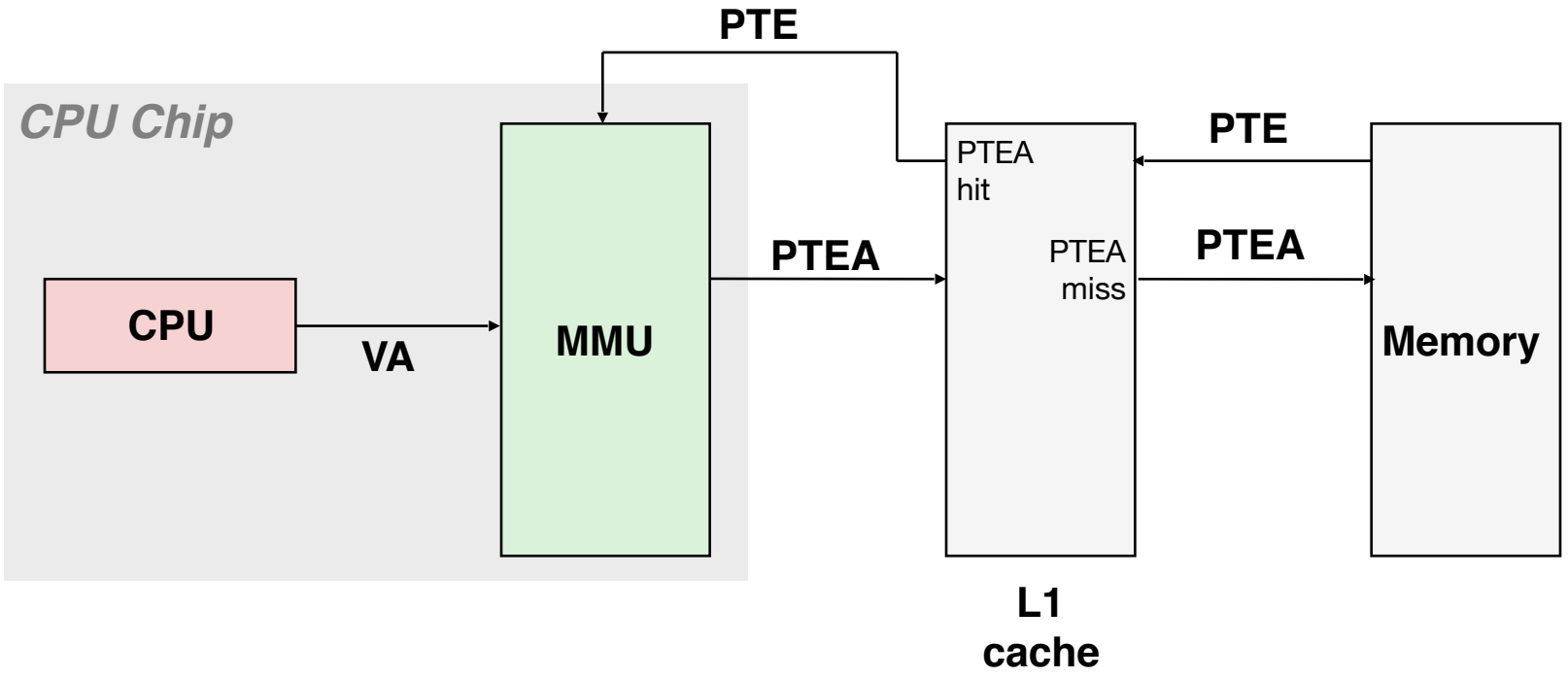

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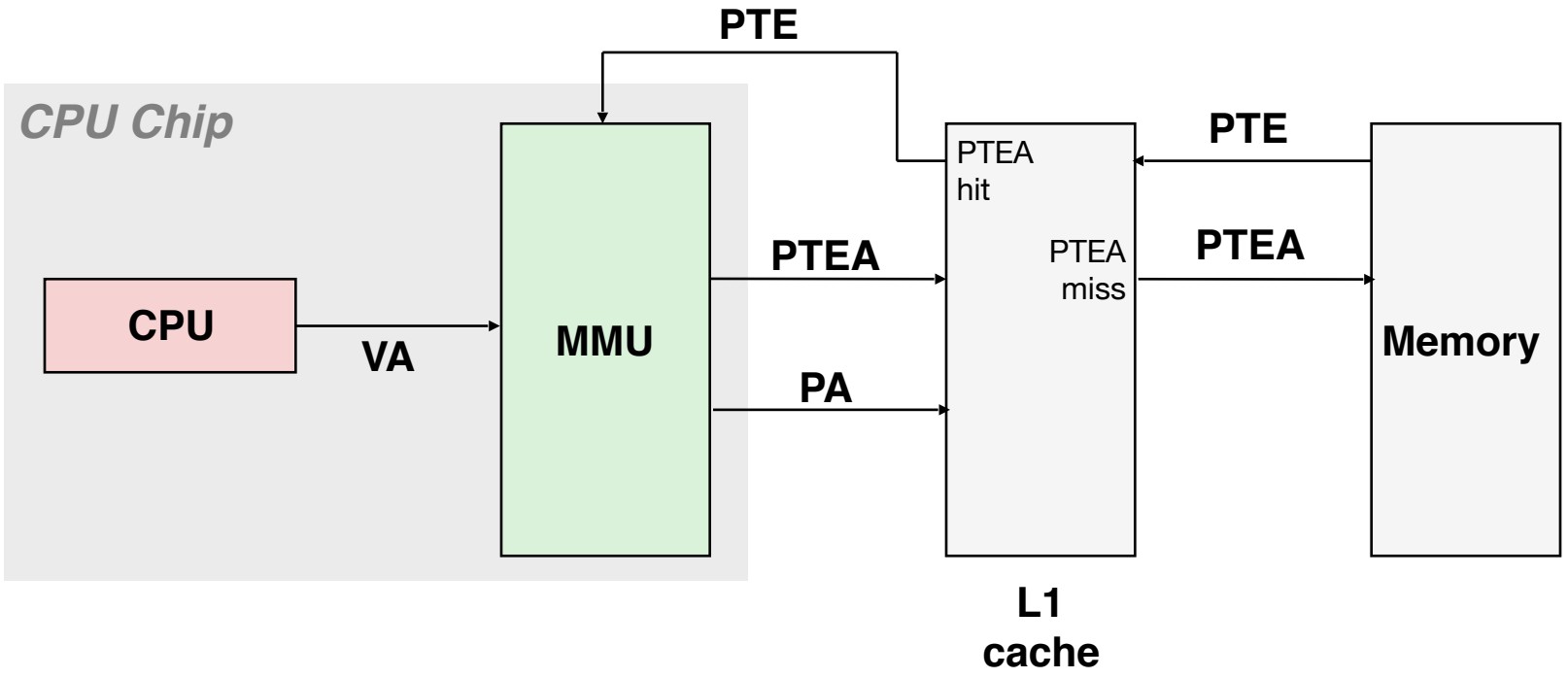

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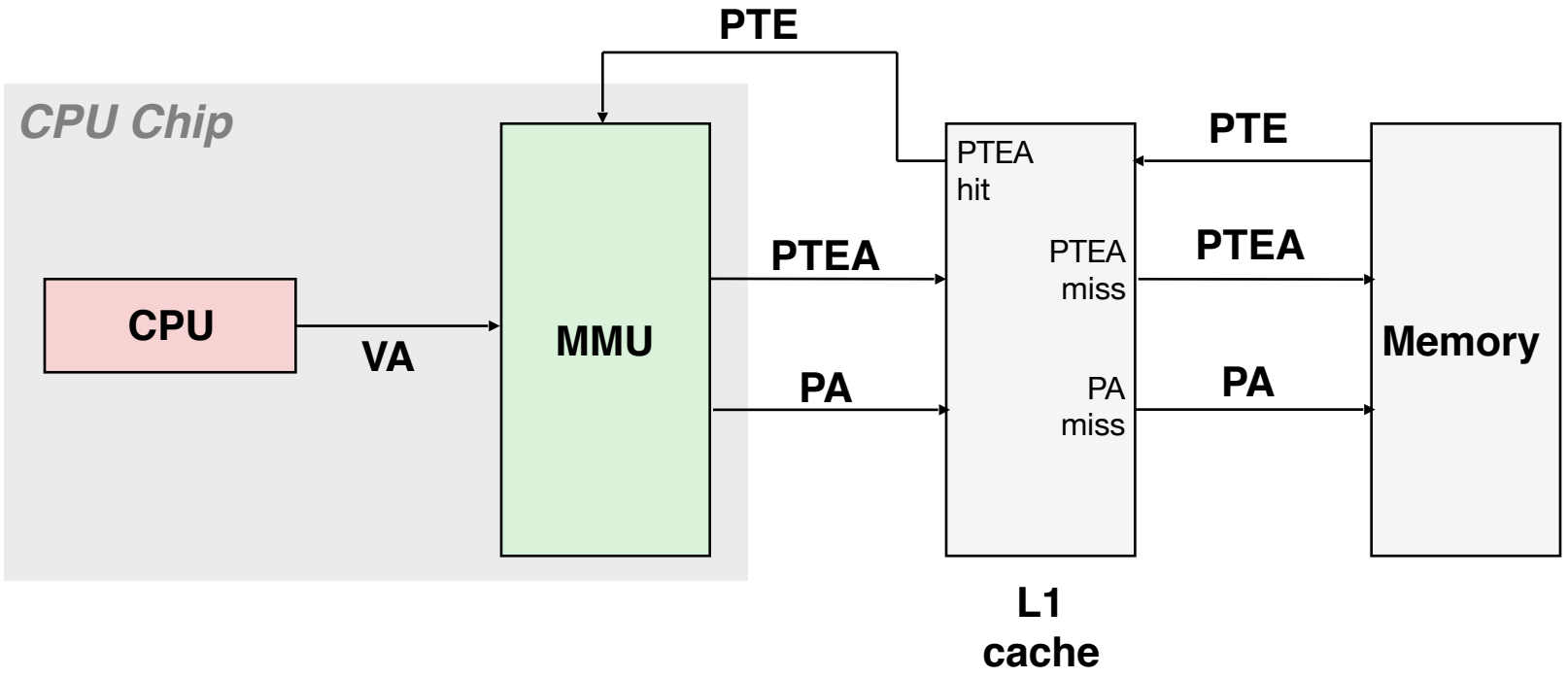

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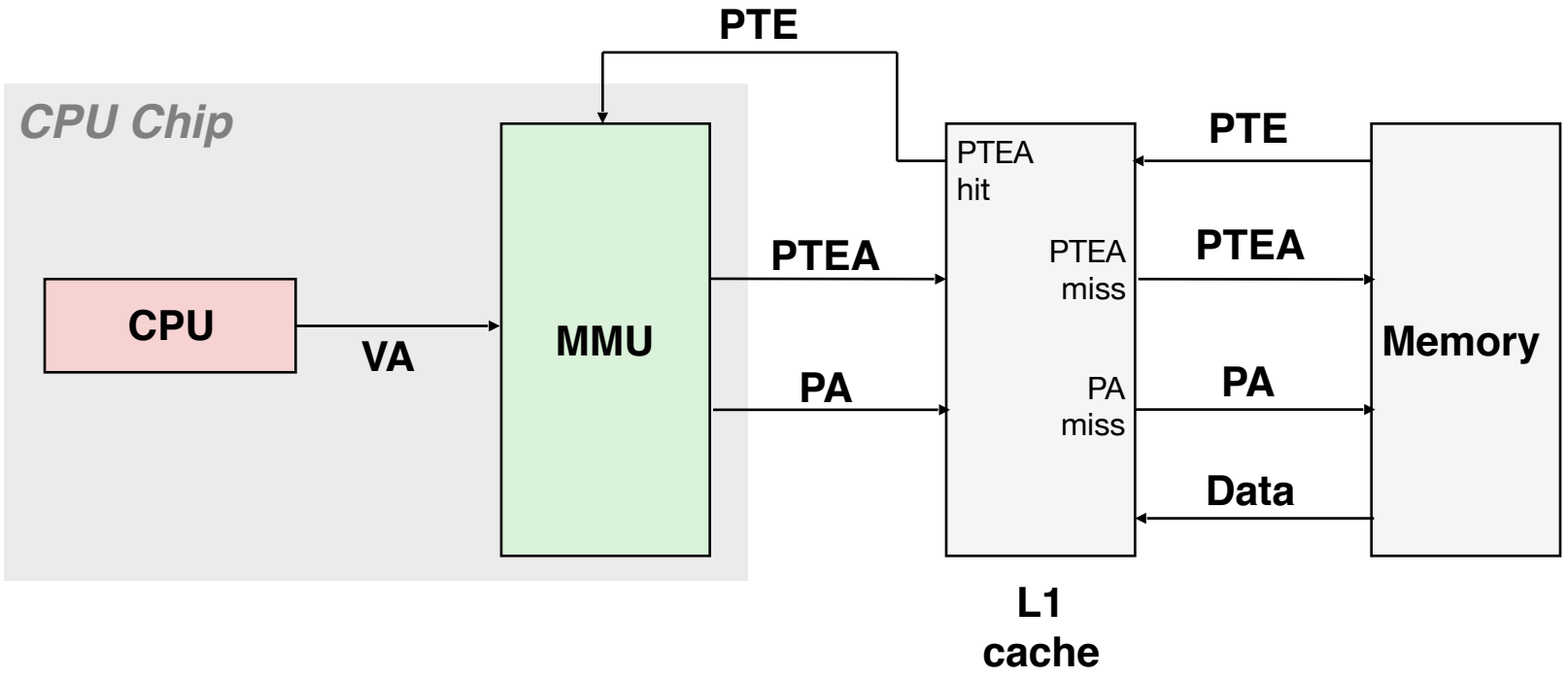

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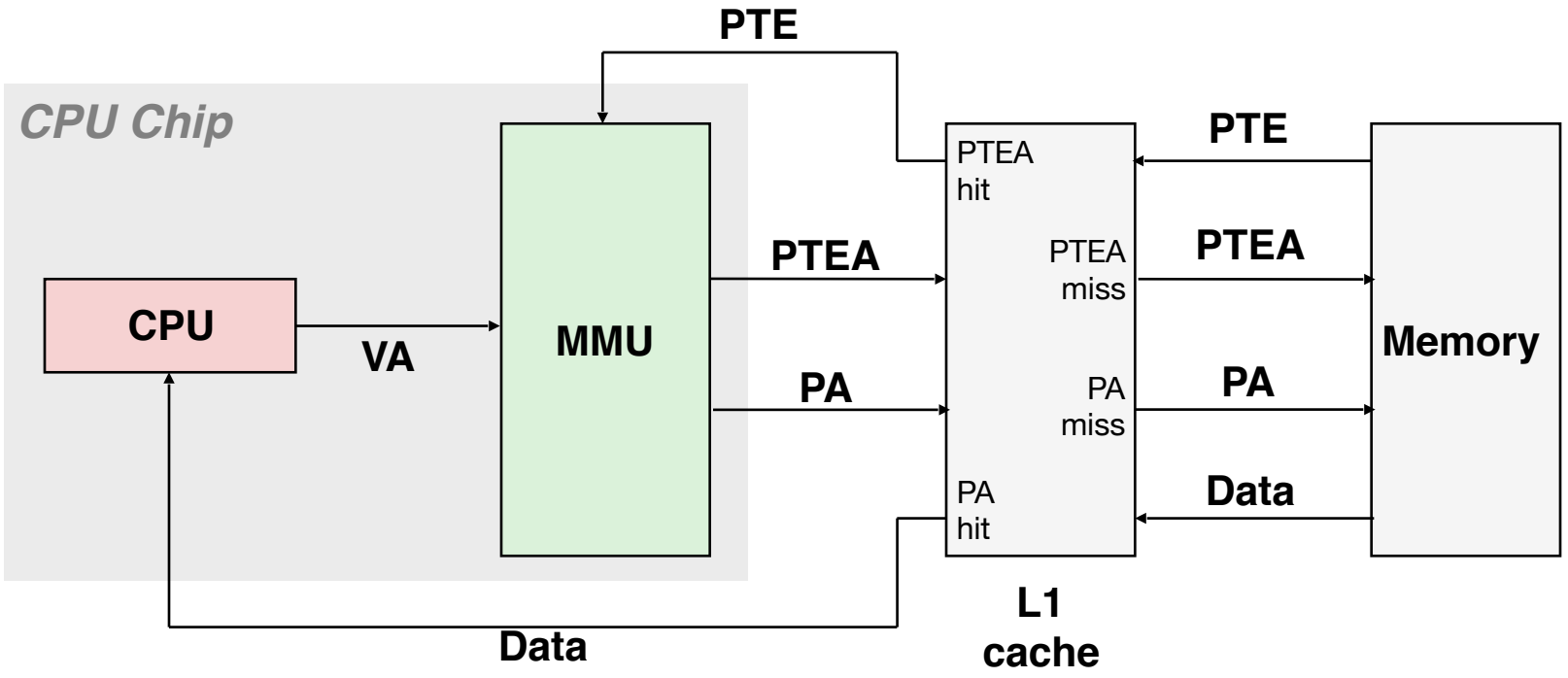

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Speeding up Translation with a TLB

- Solution: *Translation Lookaside Buffer* (TLB)
  - Think of it as a dedicated cache for page table
  - Small set-associative hardware cache in MMU
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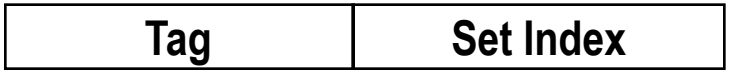

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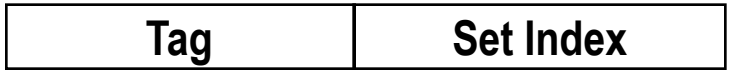

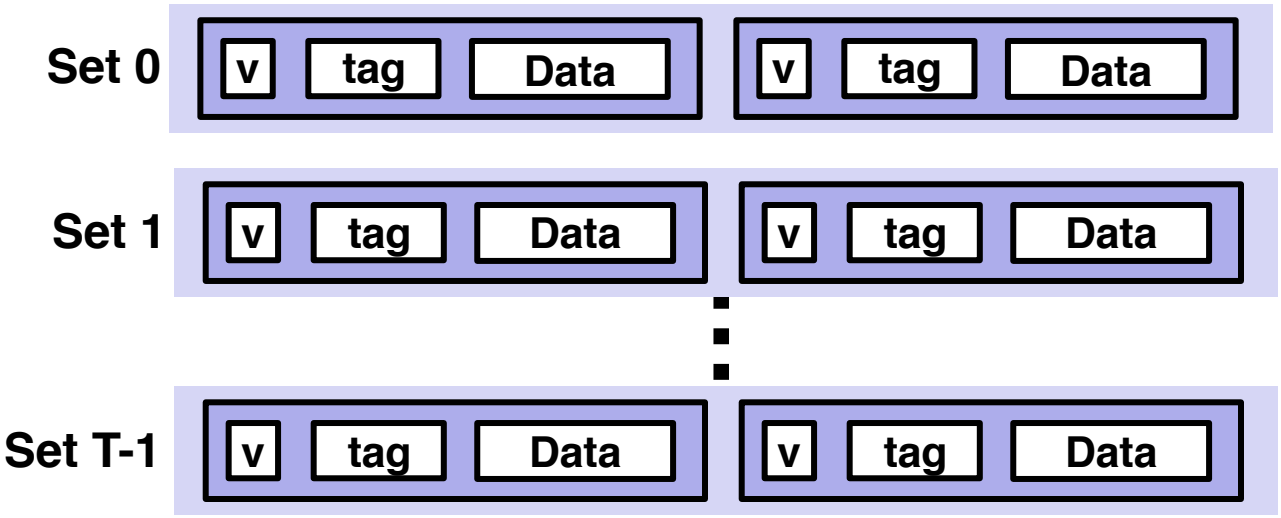

A Conventional Data Cache

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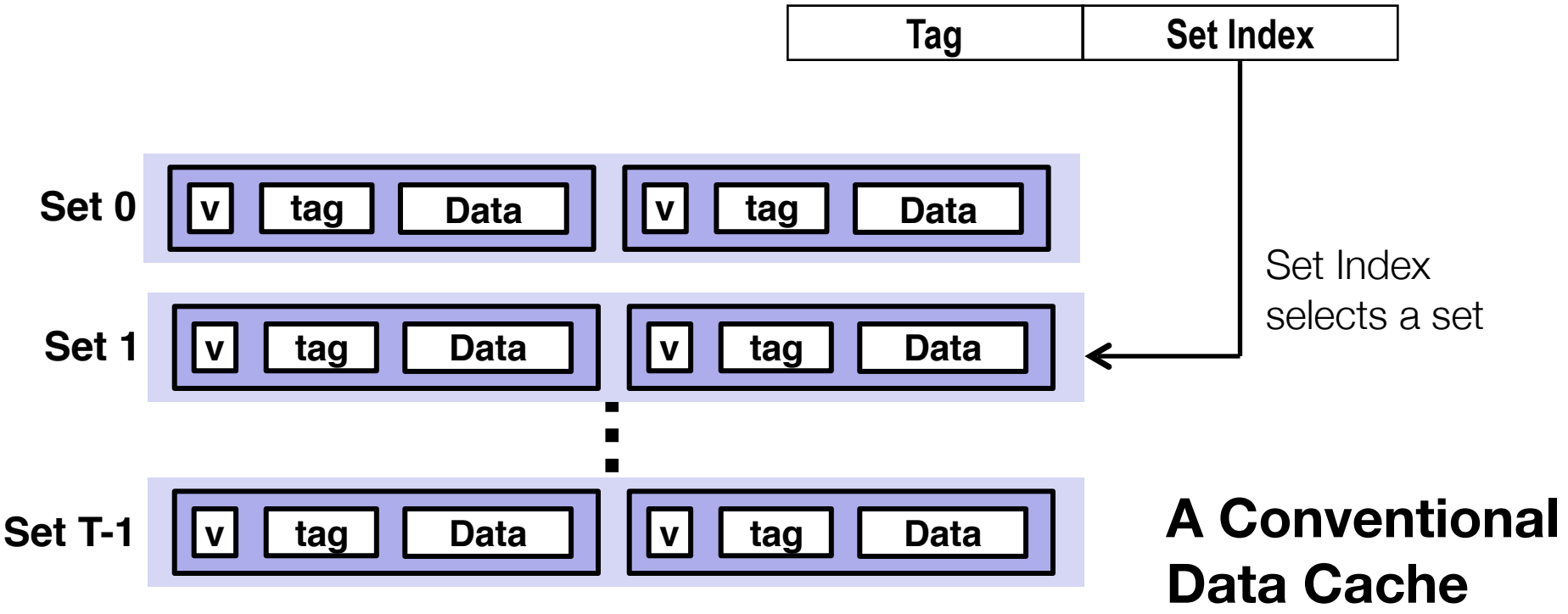

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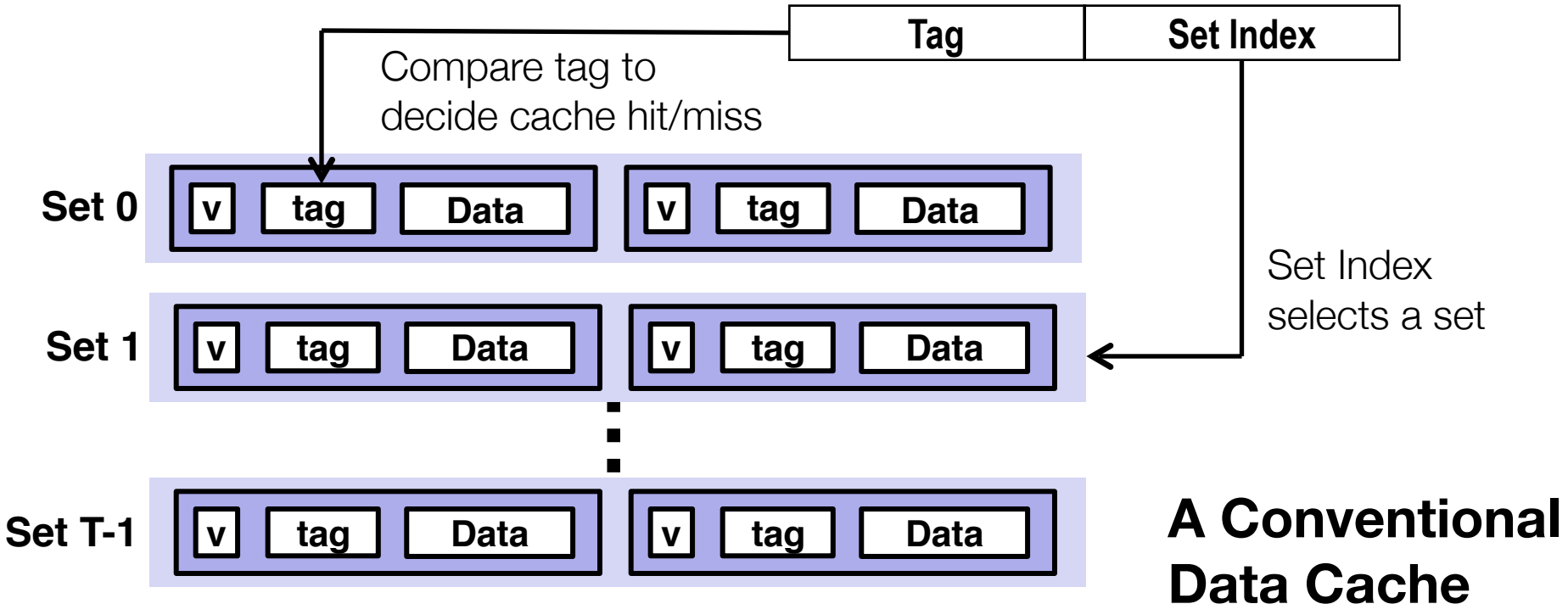
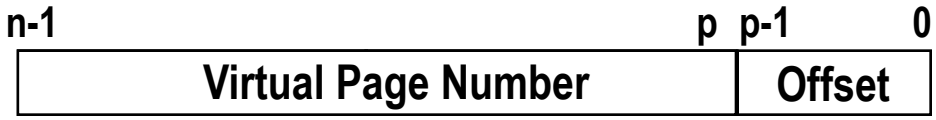
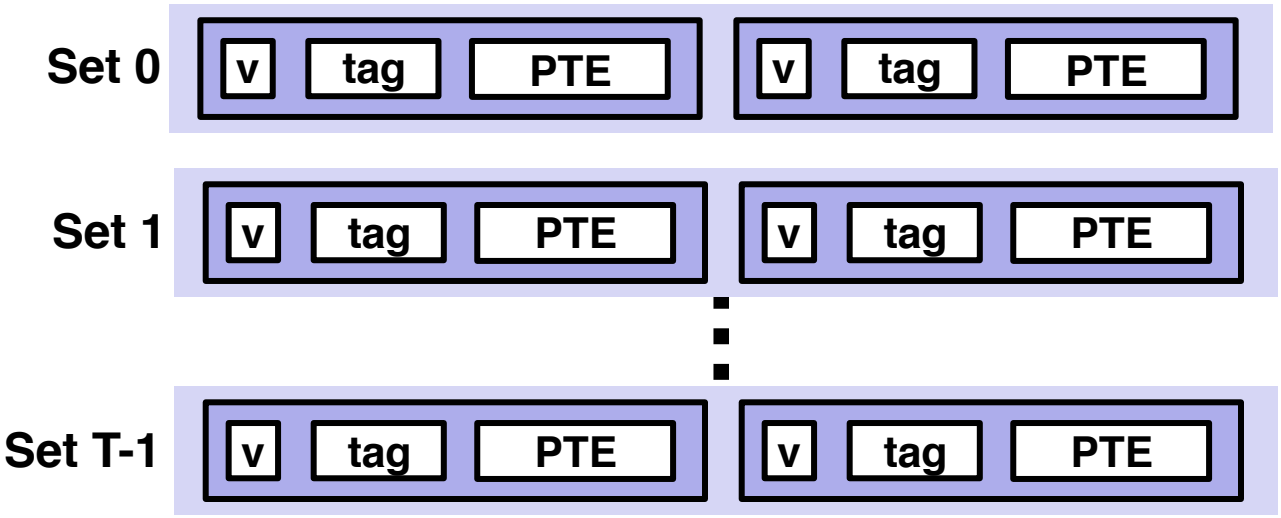


Accessing the TLB

- MMU uses the Virtual Page Number portion of the virtual address to access the TLB:





A Page Table Cache

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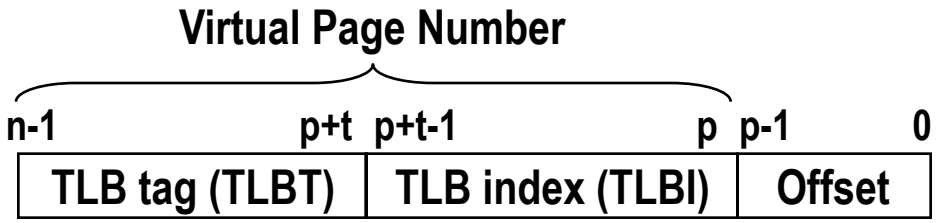

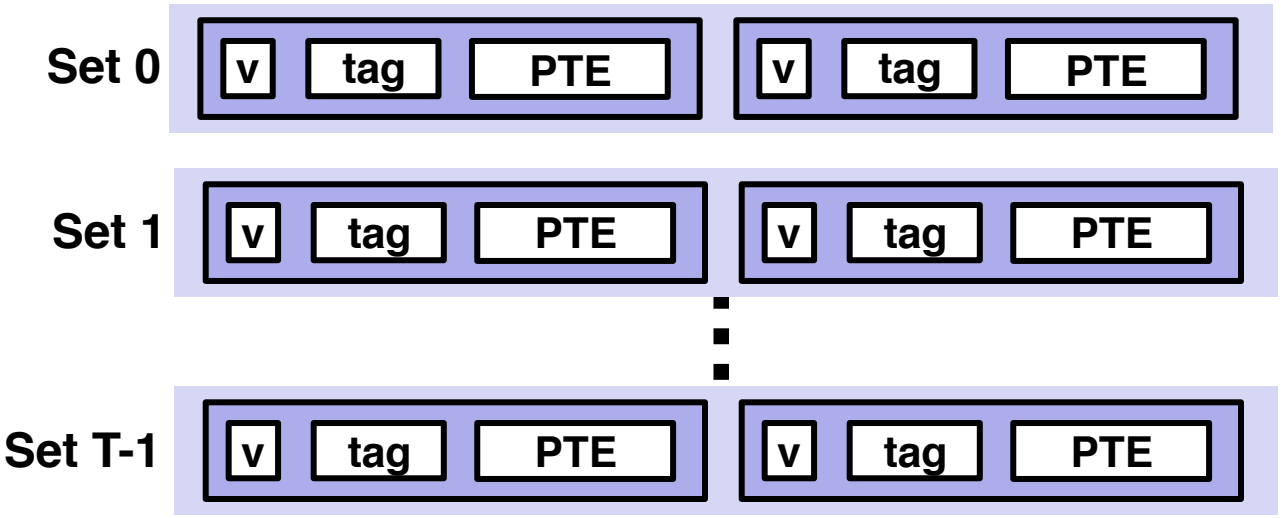

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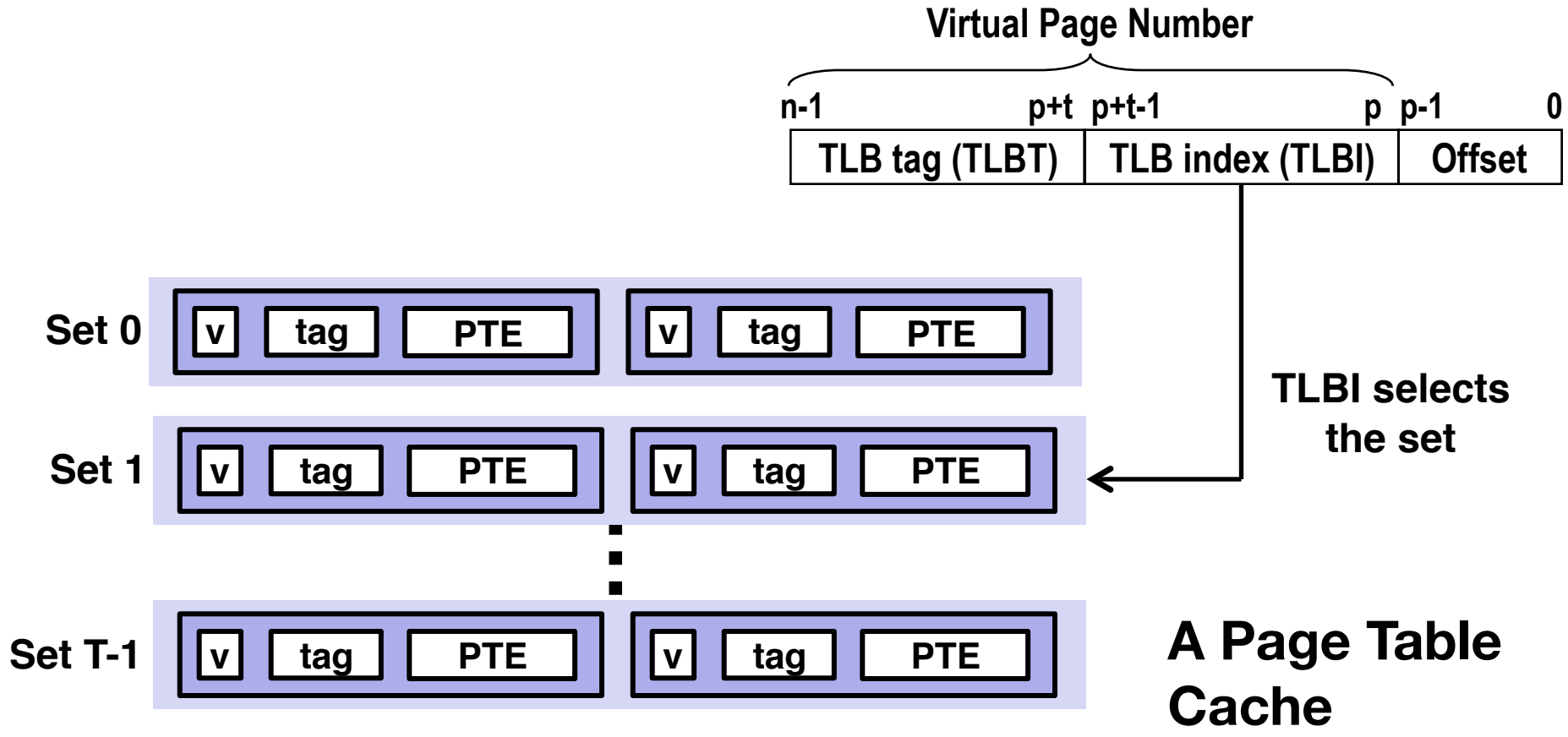

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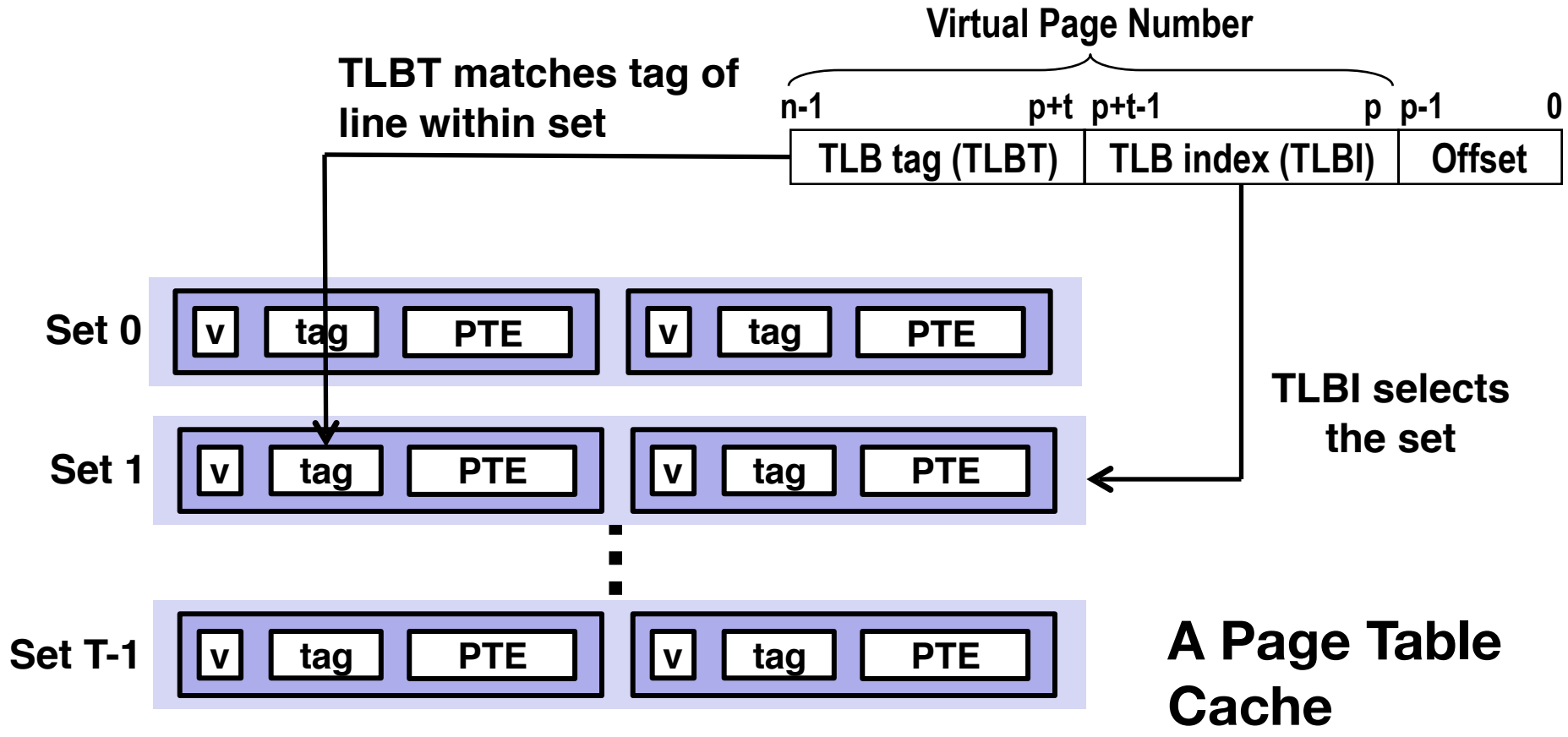
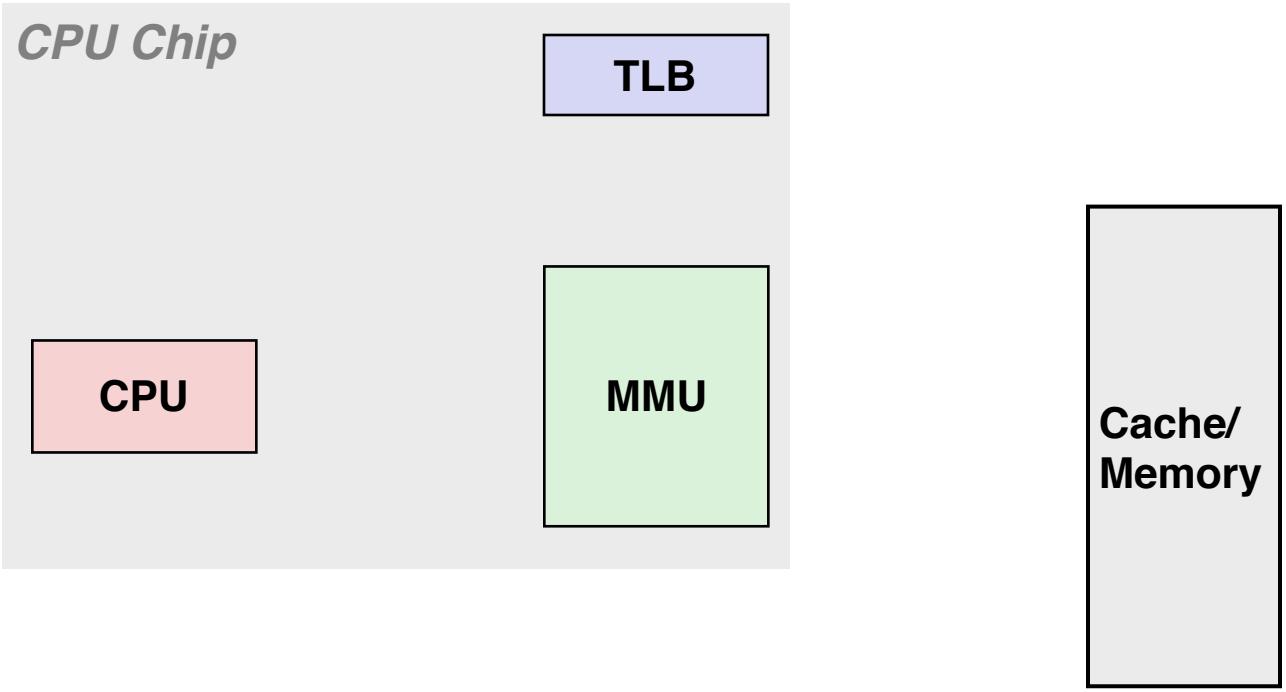
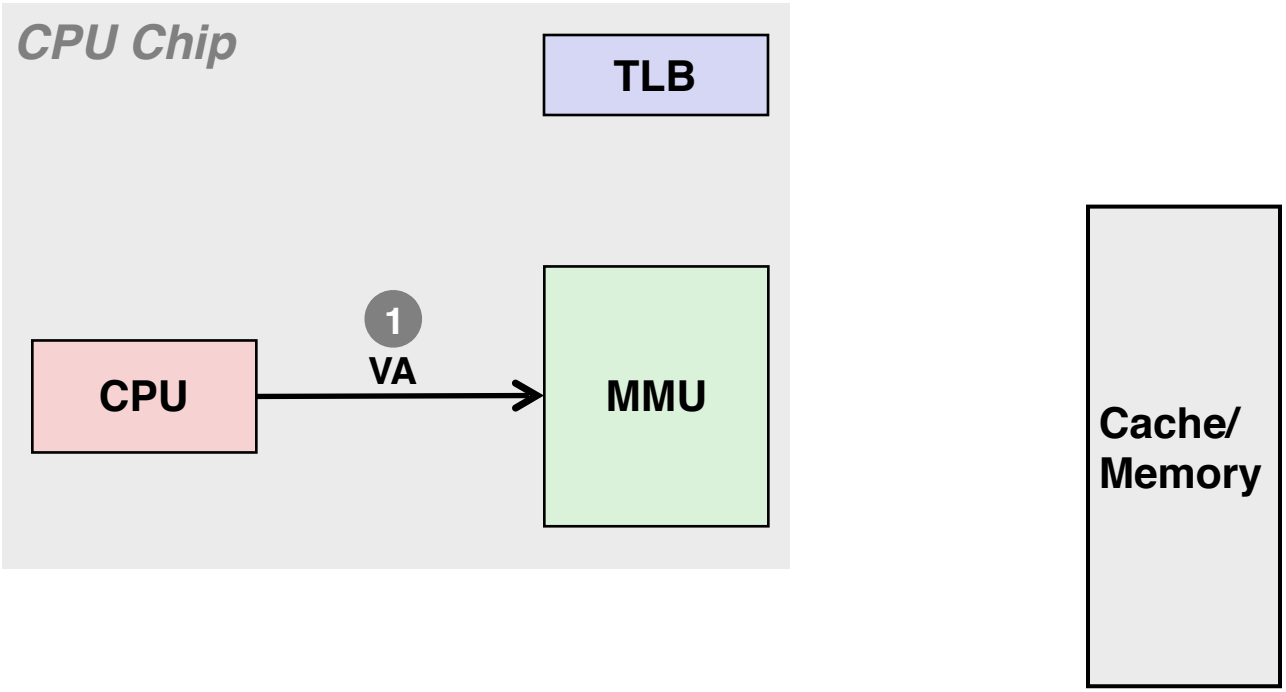


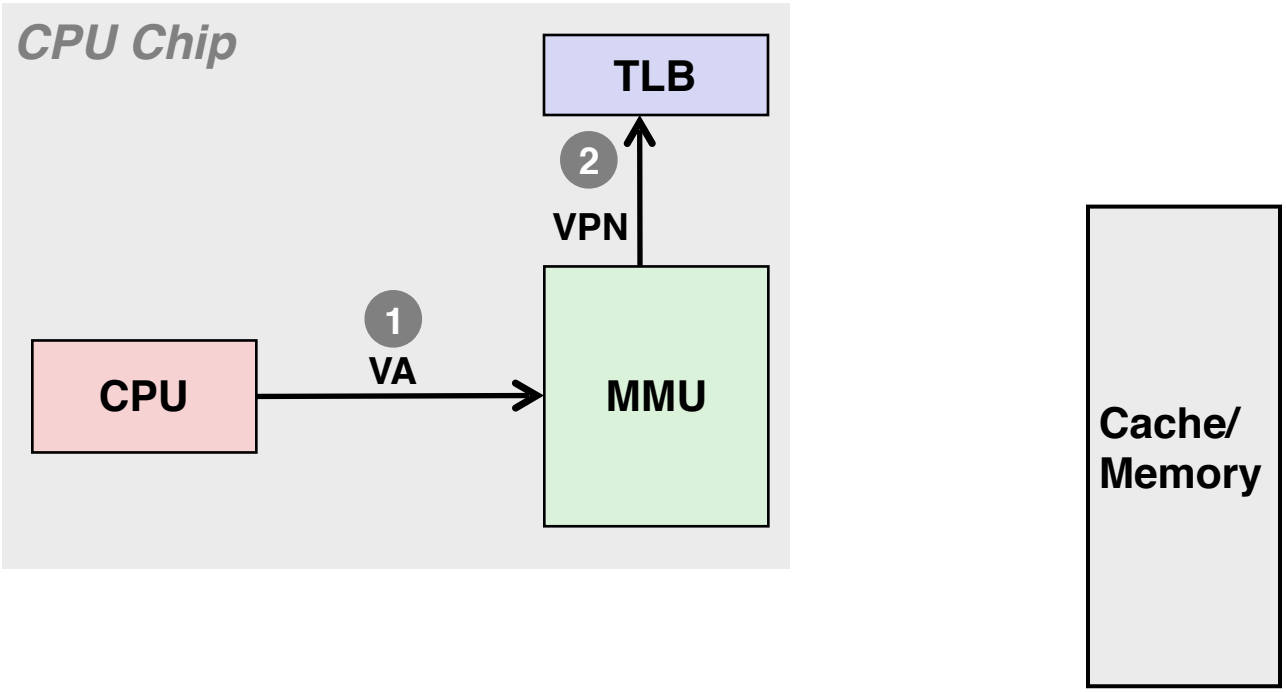
TLB Hit



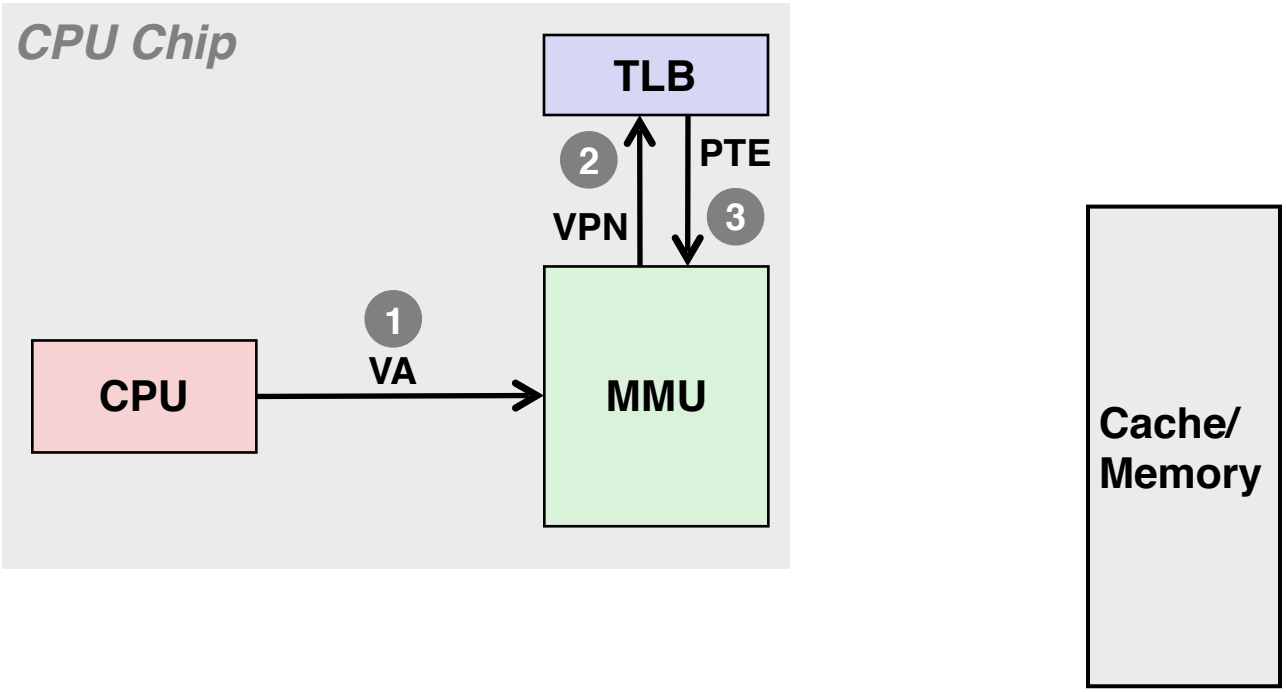
TLB Hit



TLB Hit



TLB Hit



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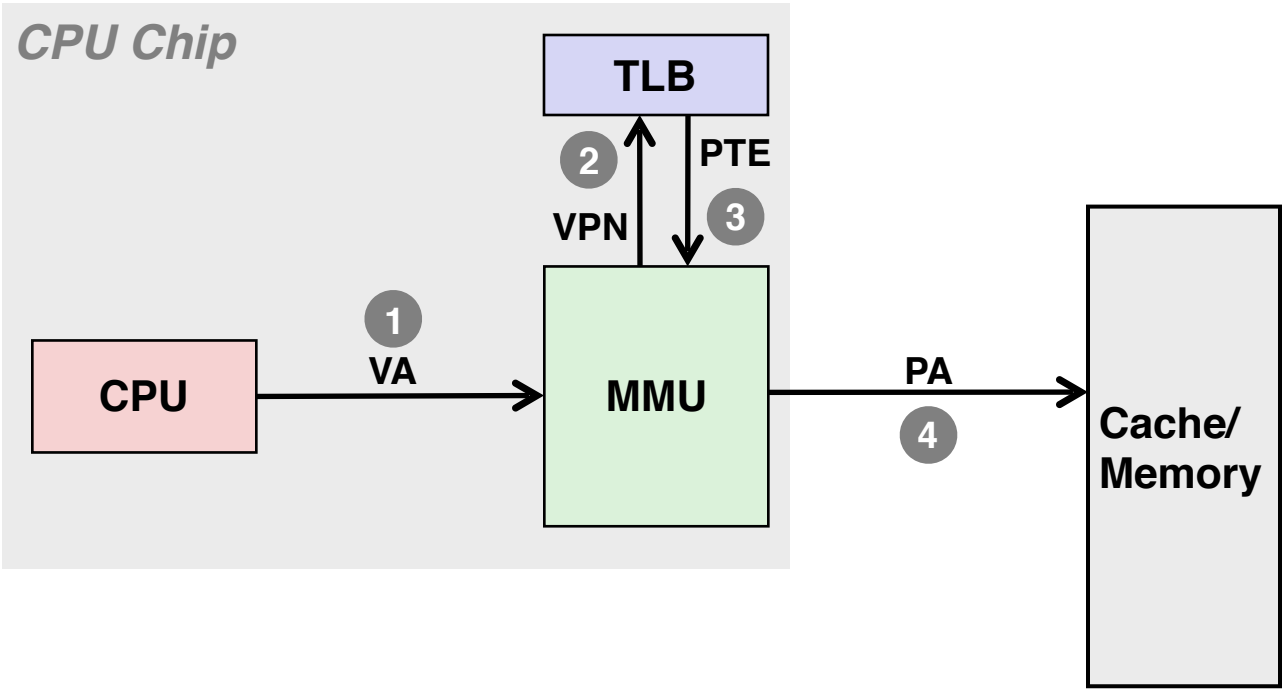
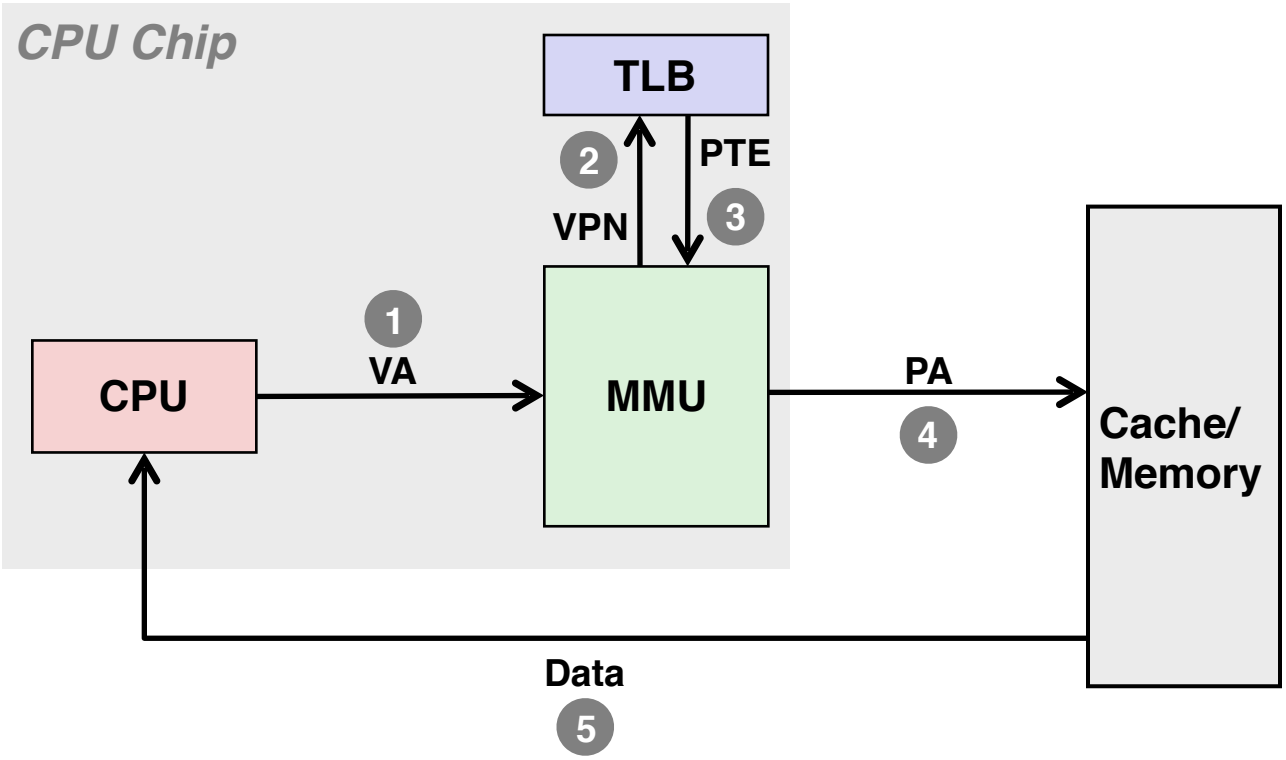
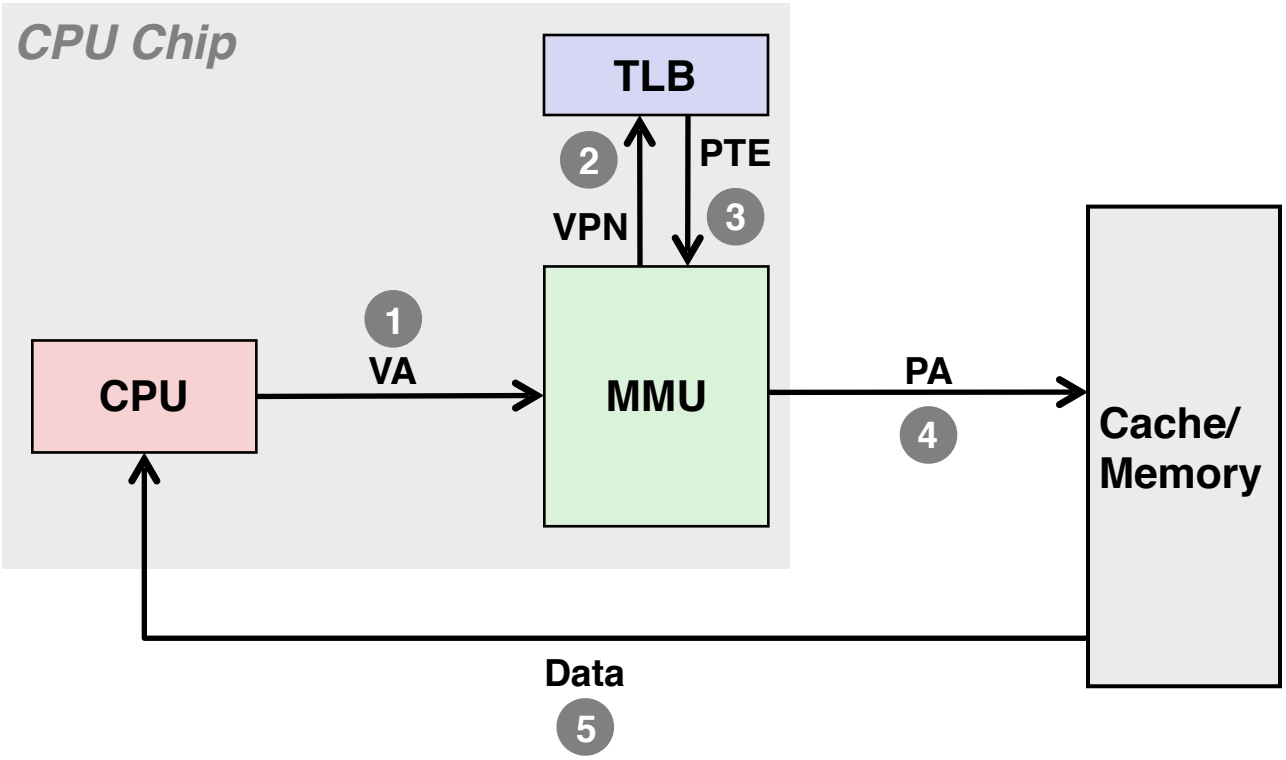


TLB Hit

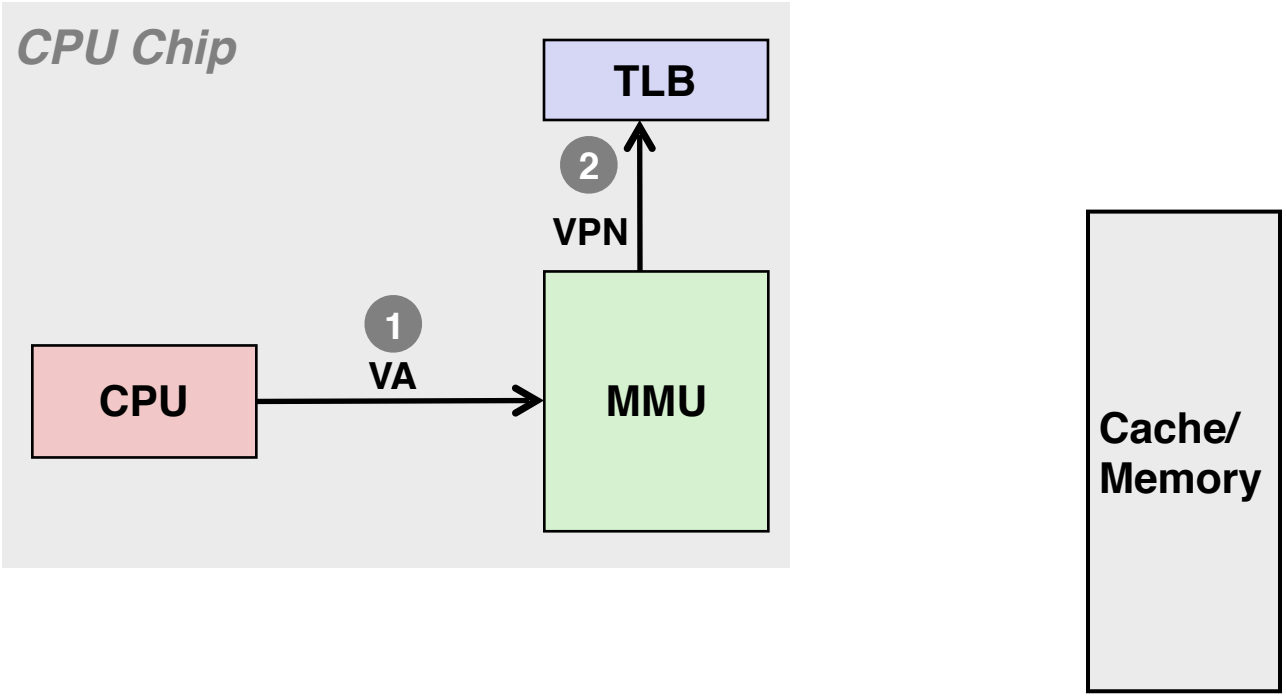


TLB Hit

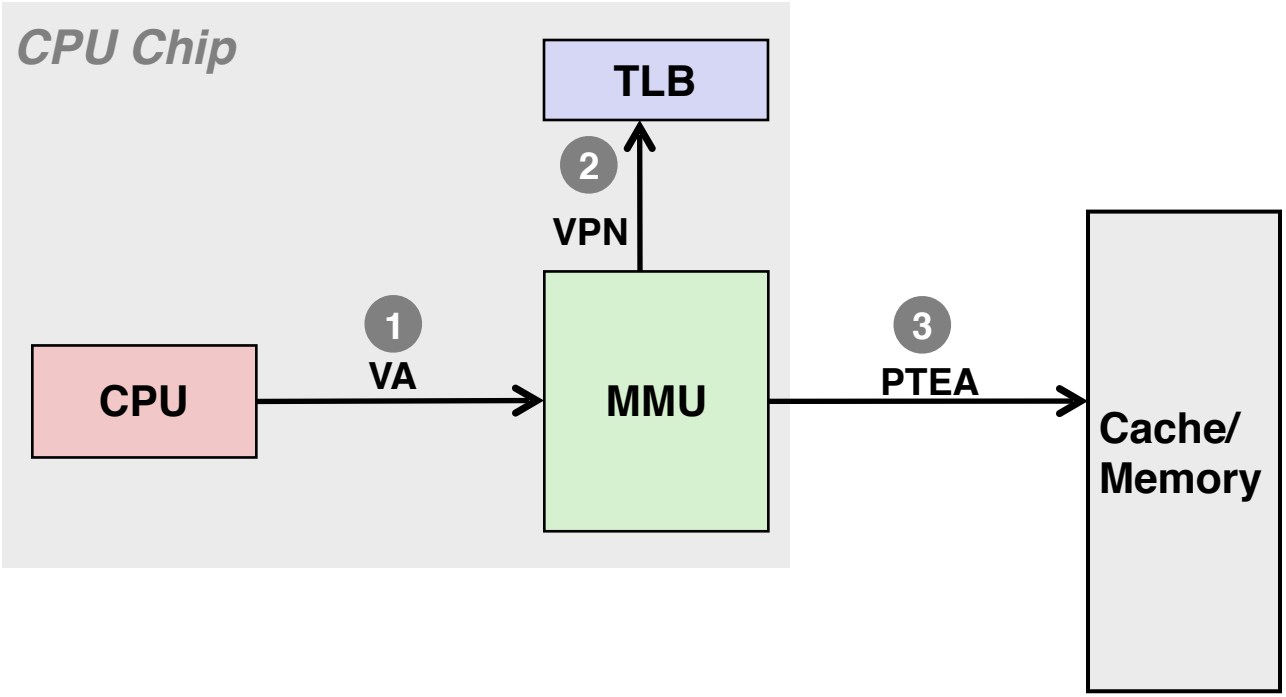


A TLB hit eliminates a memory access

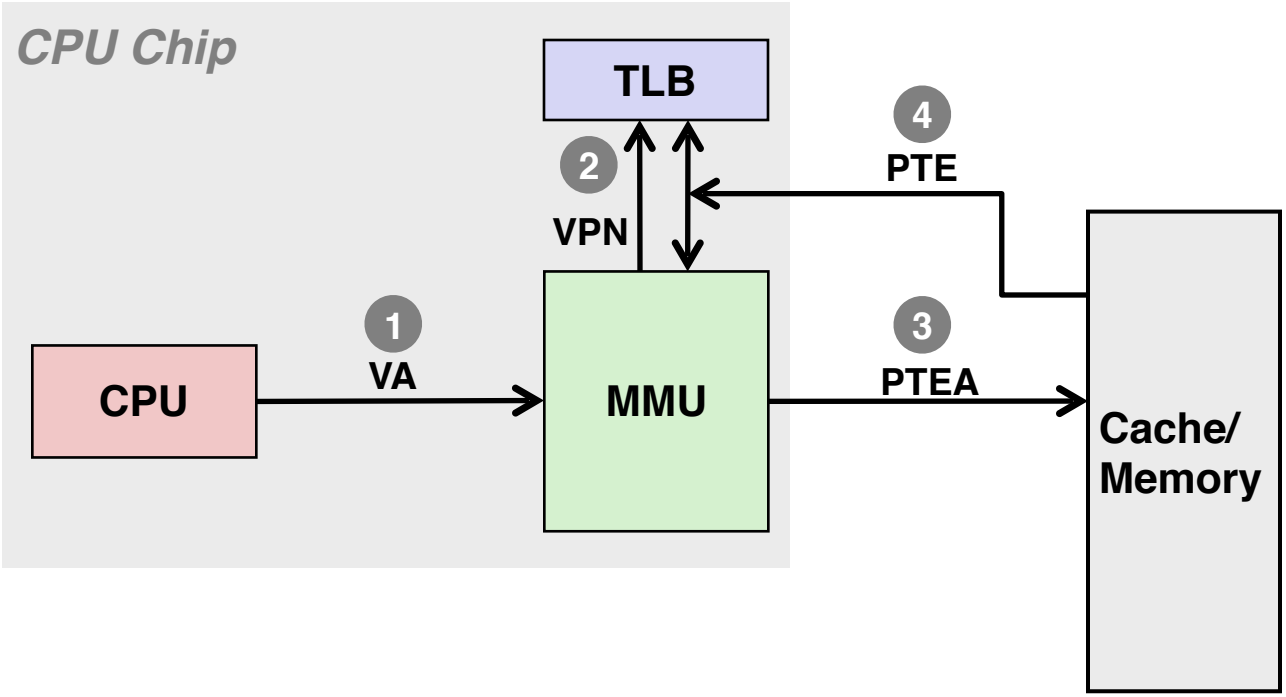
TLB Miss



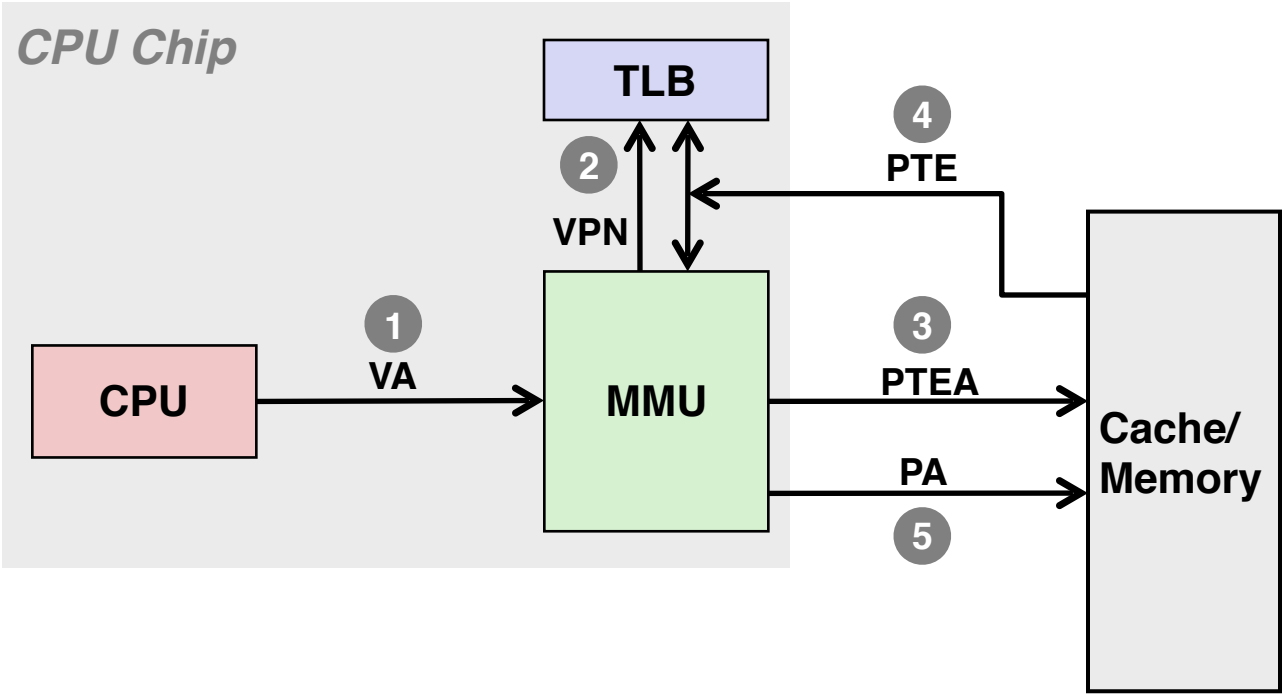
TLB Miss



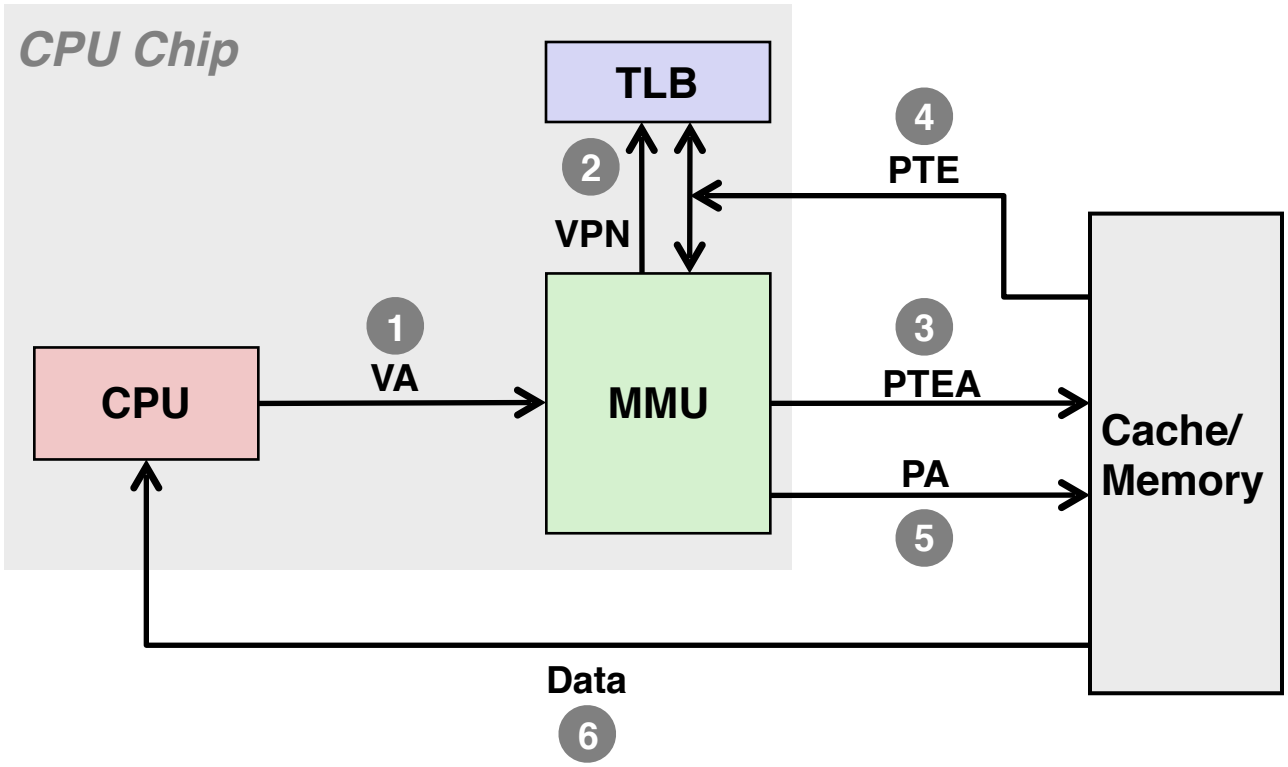
TLB Miss



TLB Miss



TLB Miss


CPU Chip
TLB
4
PTE
2
VPN
1
VA
3
PTEA
CPU
MMU
Cache/
Memory
PA
5
Data
6