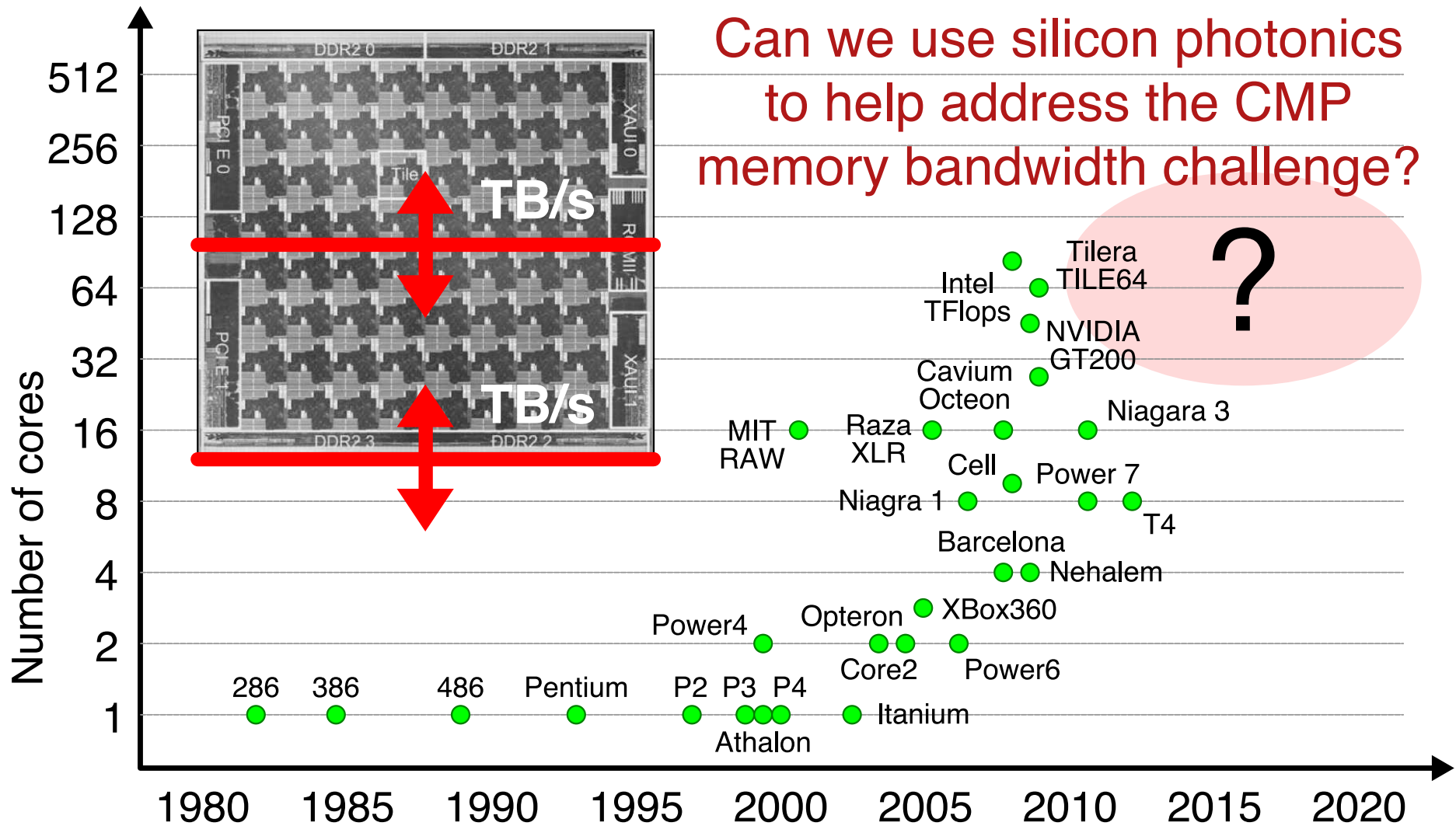


Designing Chip-Level Nanophotonic Interconnection Networks

Christopher Batten
Computer Systems Laboratory
Cornell University

ASPLOS PC Meeting Mini-Symposium
October 21, 2011

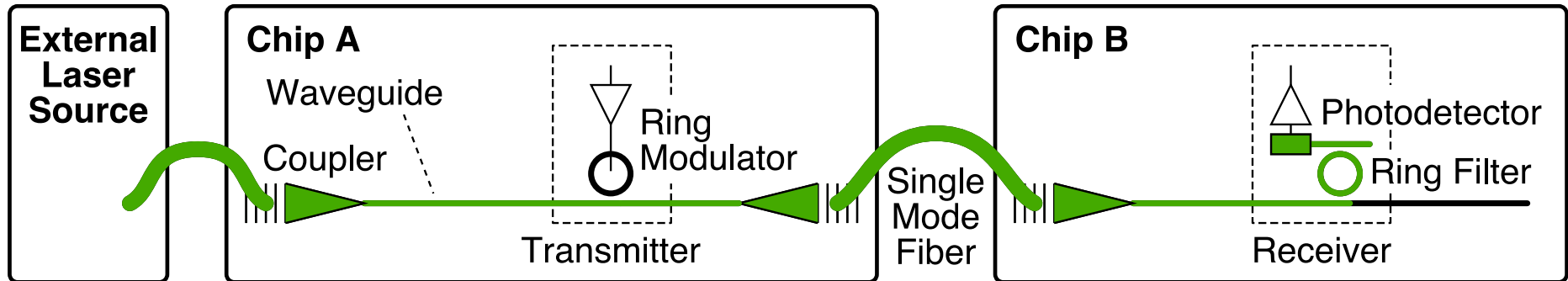
CMP Memory Bandwidth Challenge



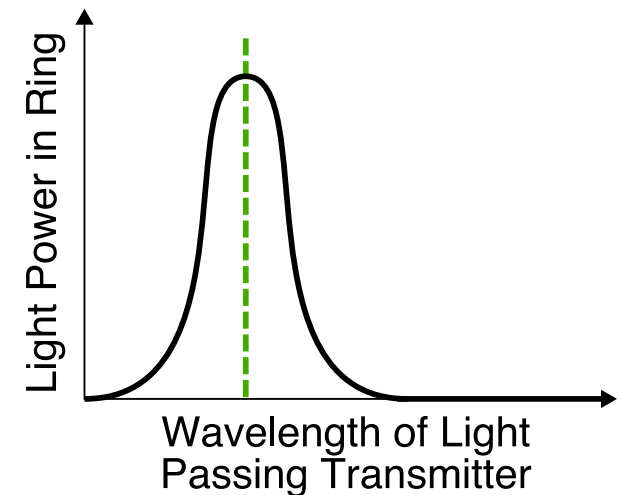
Goal for Talk

Illustrate the nanophotonic interconnection network design process and explain what research in this area is trying to achieve

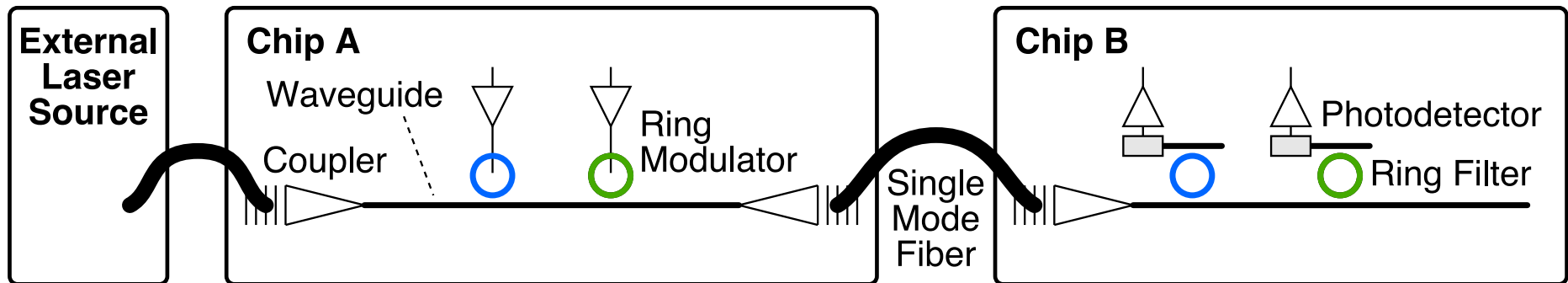
Implementing a Nanophotonic Channel



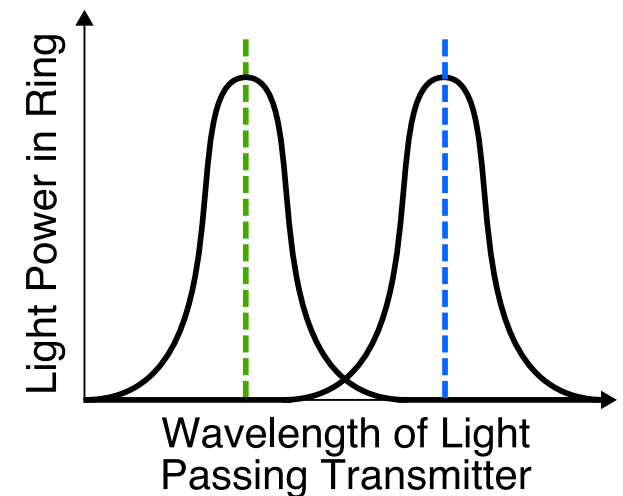
- Light coupled into waveguide on chip A
- Transmitter off : Light extracted by ring modulator
- Transmitter on : Light passes by ring modulator
- Light continues to receiver on chip B
- Light extracted by receiver's ring filter and guided to photodetector



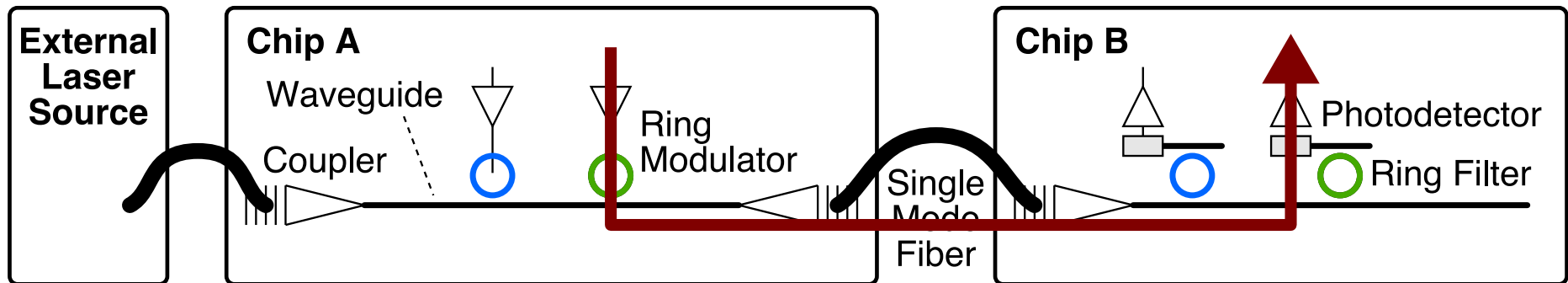
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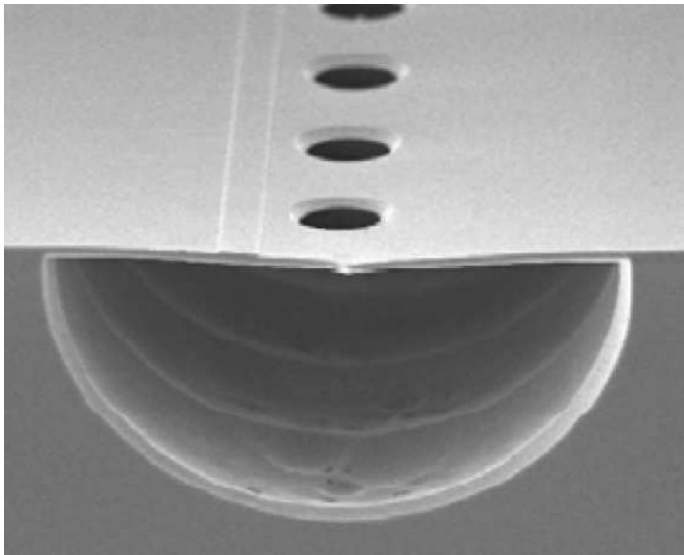
Energy Efficiency and Bandwidth Density



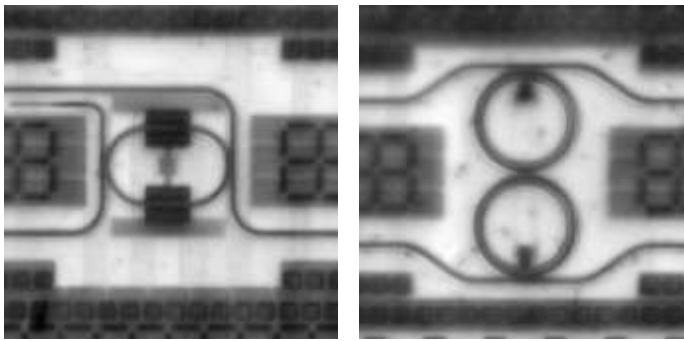
	Energy (pJ/b)	Bandwidth Density (Gb/s/ μm)
Global on-chip photonic link	0.25	160-320
Global on-chip optimally repeated M9 wire in 32 nm	1	5
Off-chip photonic link (50 μm coupler pitch)	0.25	13-26
Off-chip electrical SERDES (50 μm pitch)	5	0.2
On-chip/off-chip seamless photonic link	0.25	

Nanophotonic Device Integration Strategy

MIT: Devices monolithically integrated on active layer of standard CMOS process



Poly-Si Waveguides with Etched Air Gap

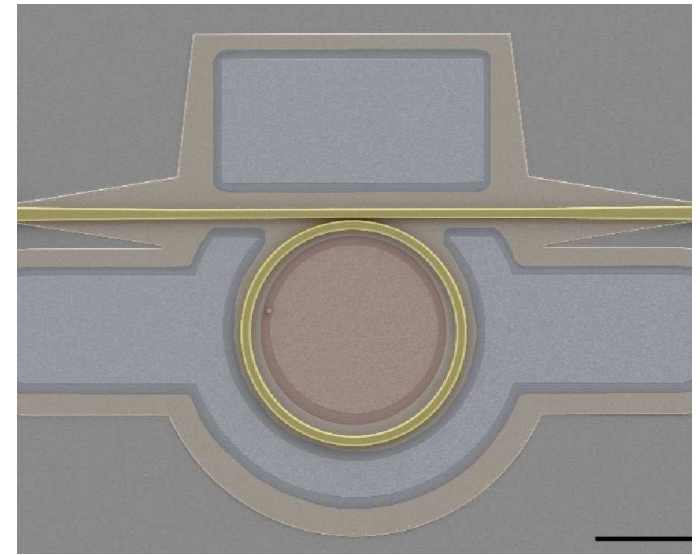


Poly-Si Modulator

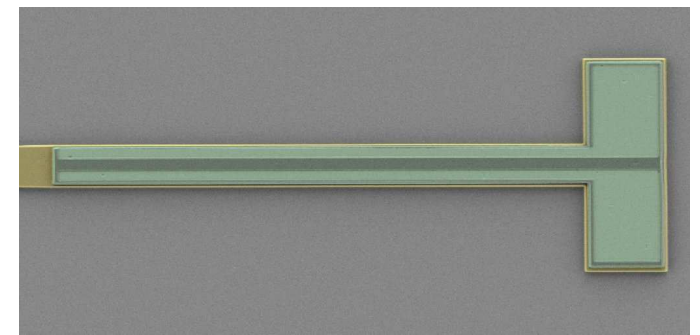
Poly-Si Passive Filter



Cornell: Devices deposited on top of metal interconnect stack of standard CMOS chips

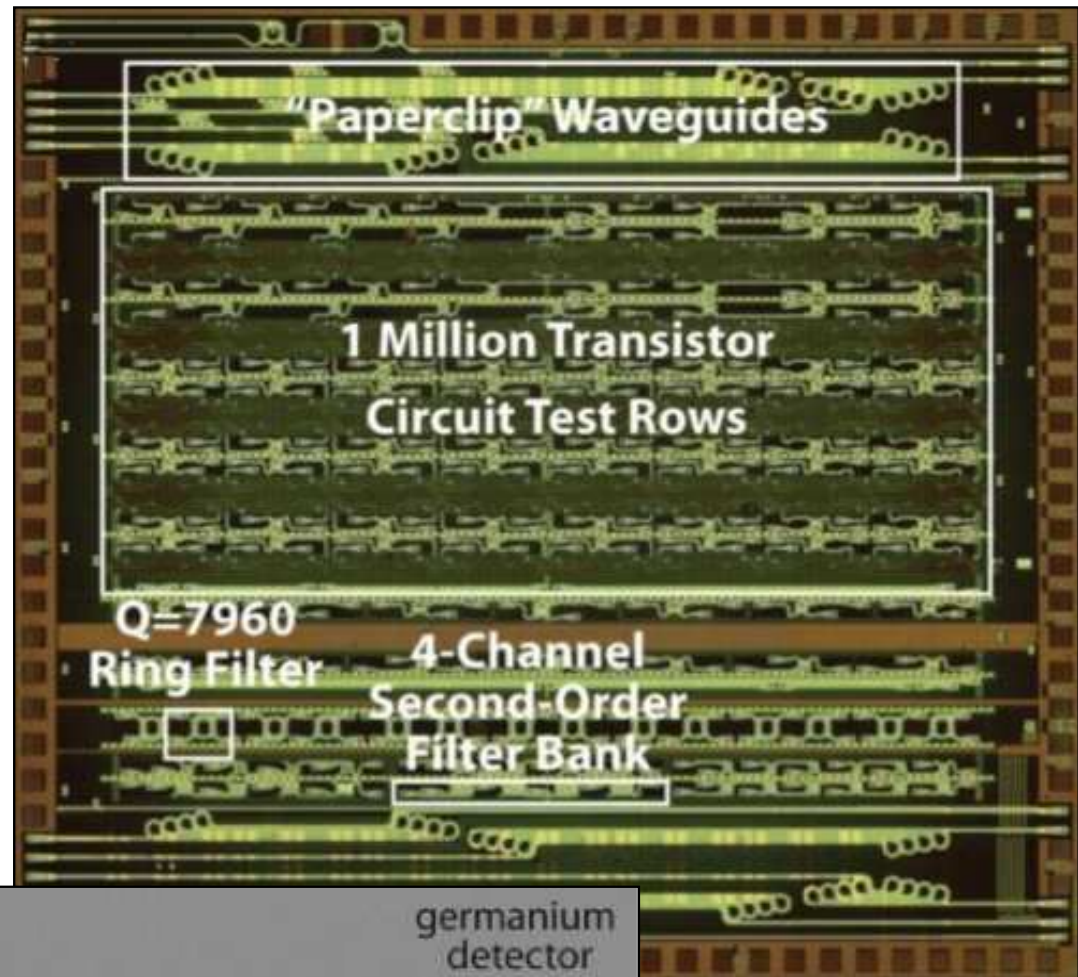


Modulator

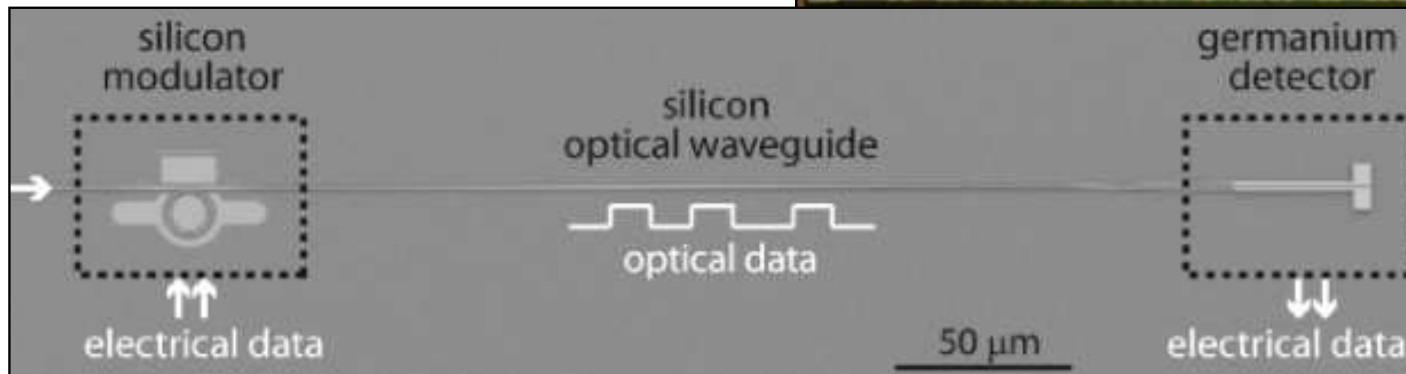


Receiver

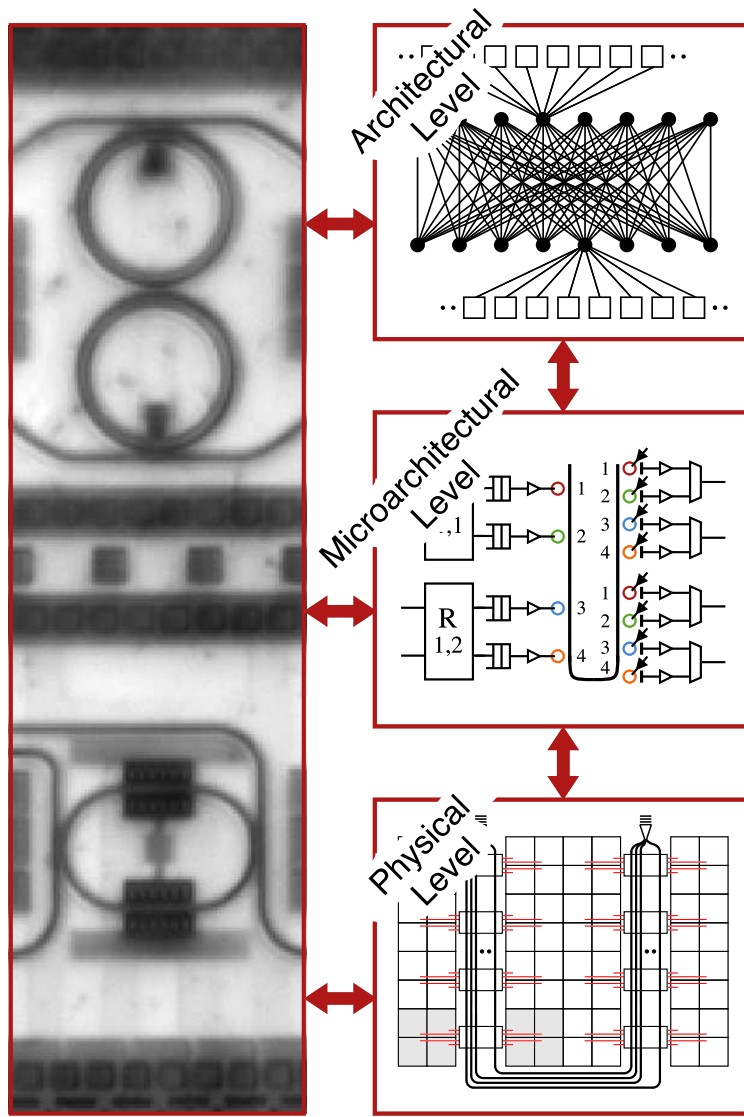
J. Orcutt et al.,
Optics Express, 2011



L. Chen et al.,
Optics Express, 2009

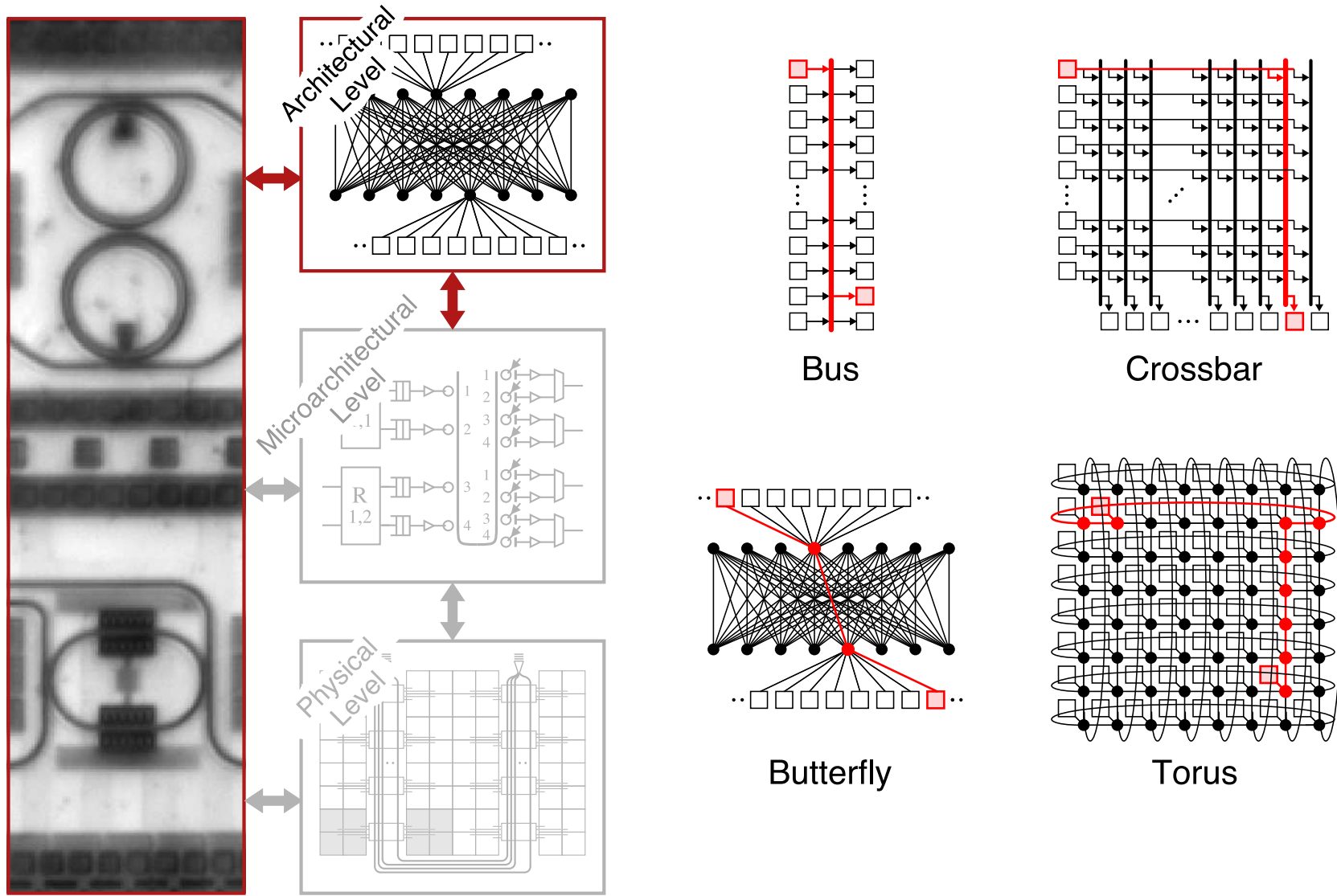


Designing Nanophotonic Interconnection Networks

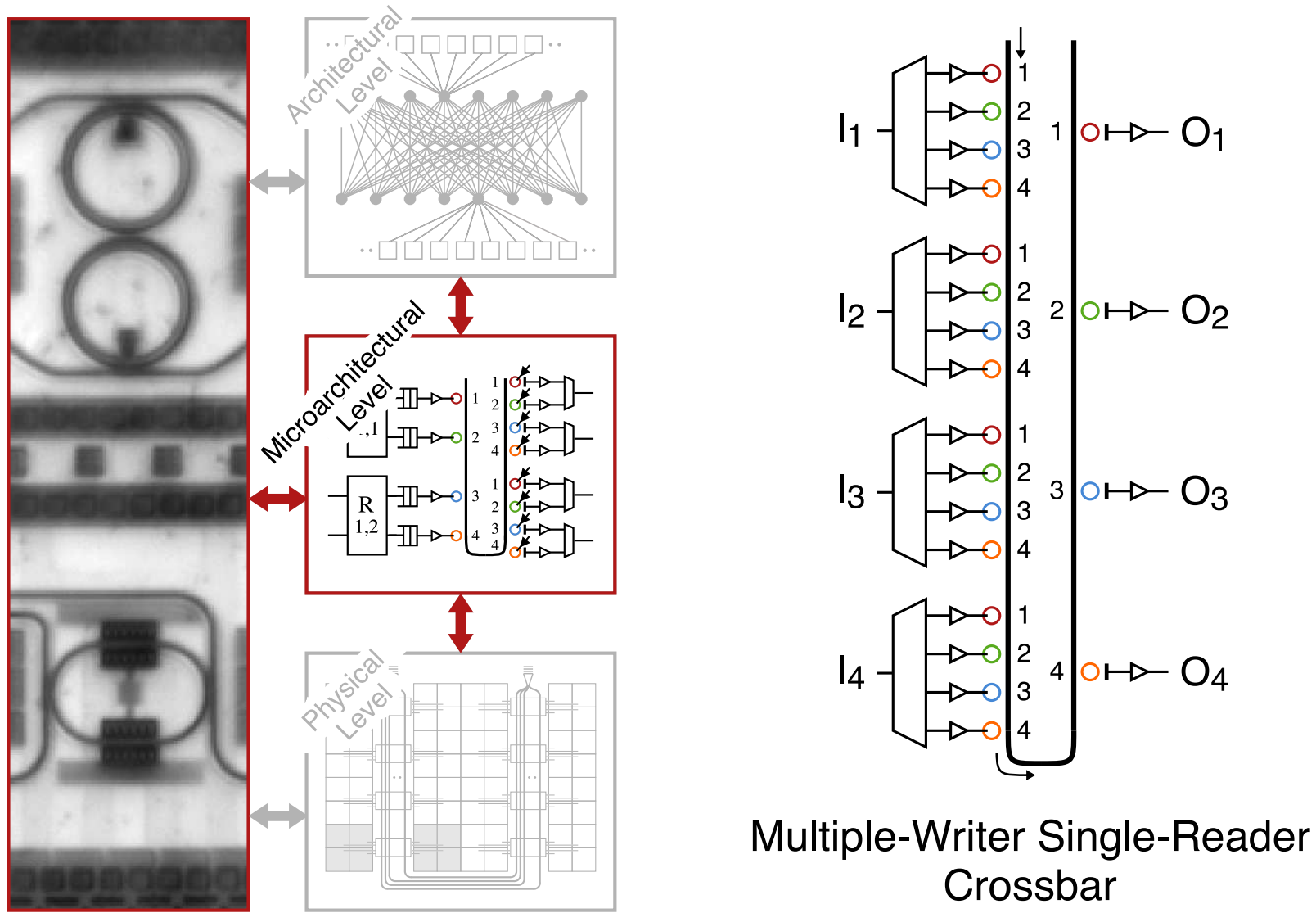


- ▶ **Architectural-Level Design**
 - ▷ Network topology, routing algorithm
 - ▷ Analytical bounds on performance
 - ▷ Electrical baseline network
- ▶ **Microarchitectural-Level Design**
 - ▷ Choose electrical vs. nanophotonic components
 - ▷ Flow control and arbitration
- ▶ **Physical-Level Design**
 - ▷ Map μ arch design to physical substrate
 - ▷ Assign wavelengths to waveguides/fibers
 - ▷ Decide how to layout waveguides and organize fibers

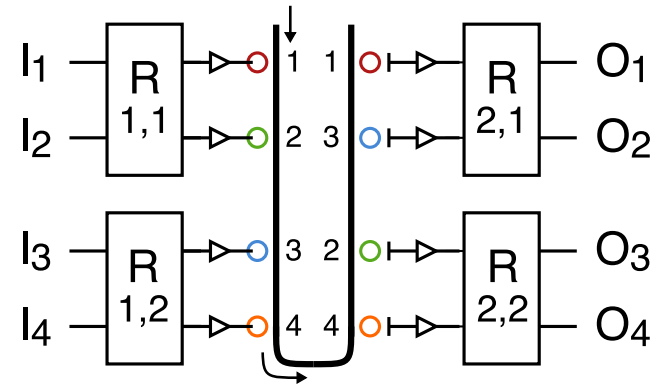
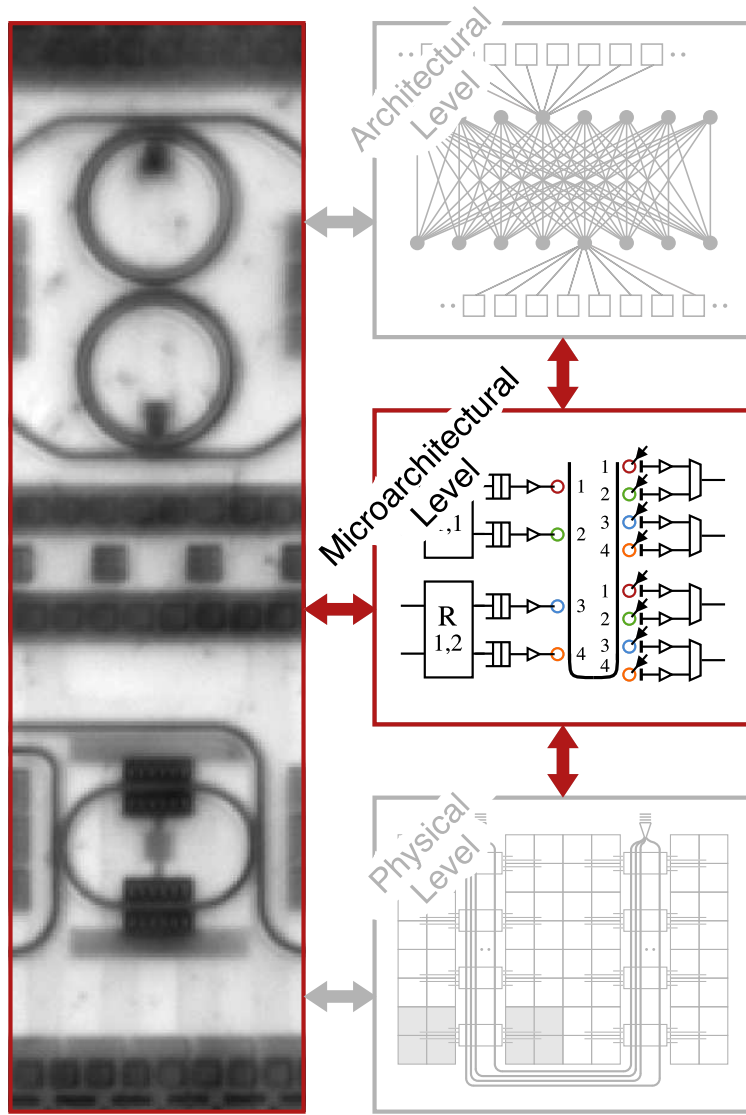
Architectural-Level Design



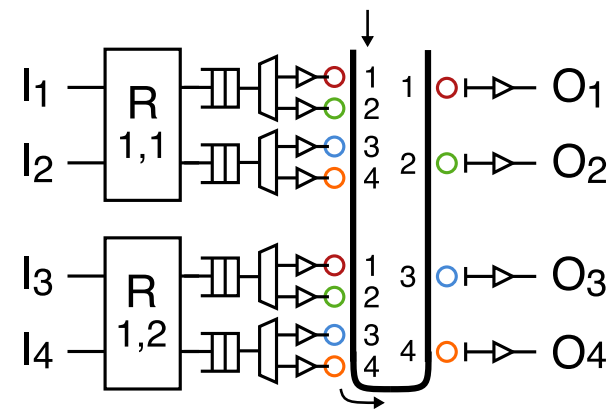
Microarchitectural-Level Design for Crossbar



Microarchitectural-Level Design for Butterfly

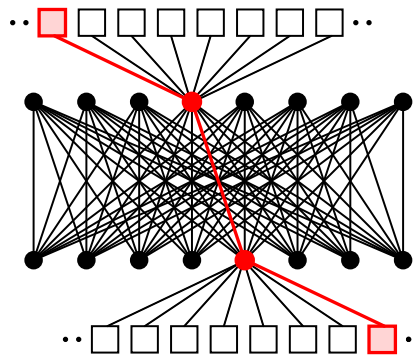


Nanophotonic Channels



Unified Nanophotonic Channels and Second-Stage Routers

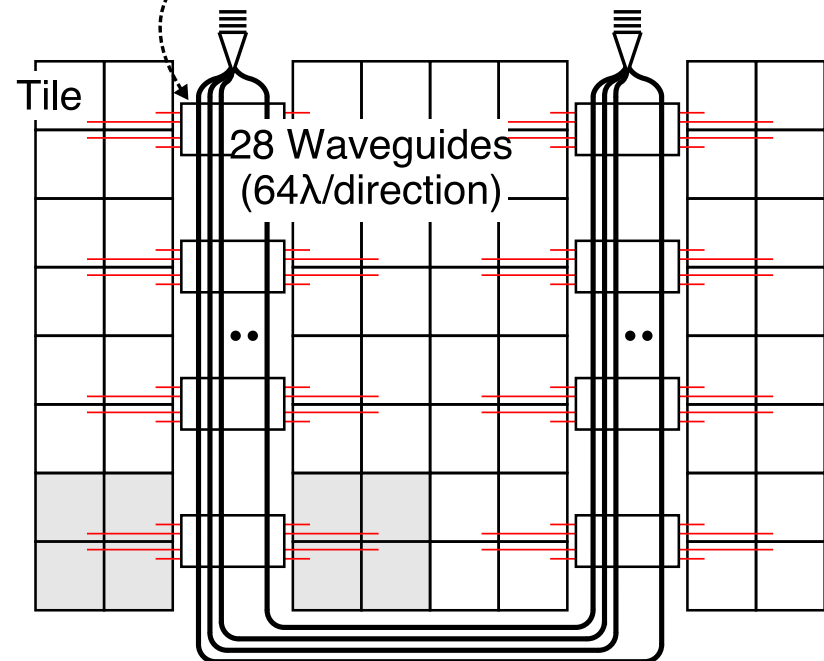
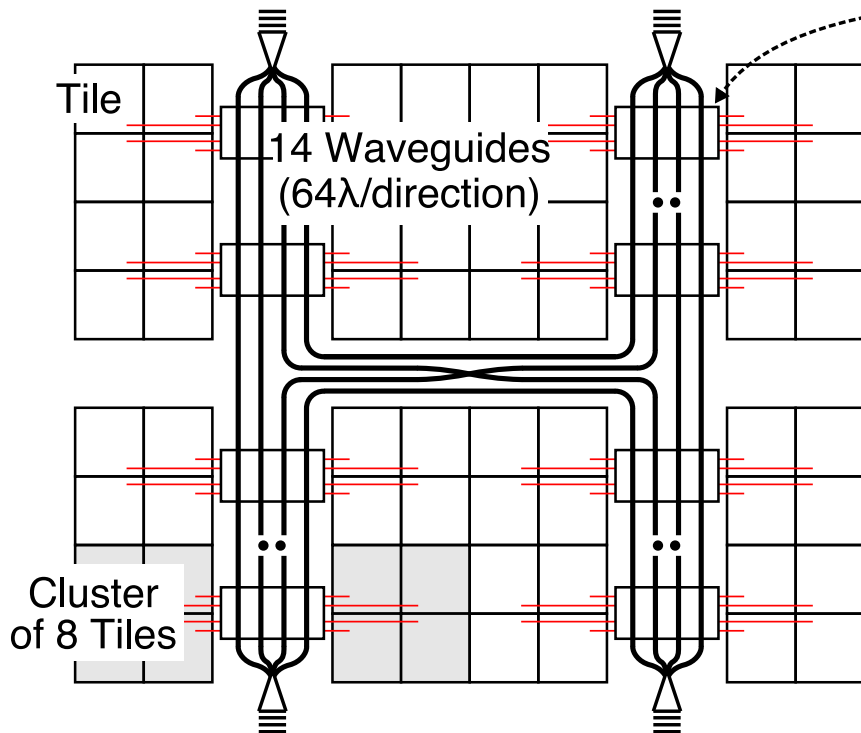
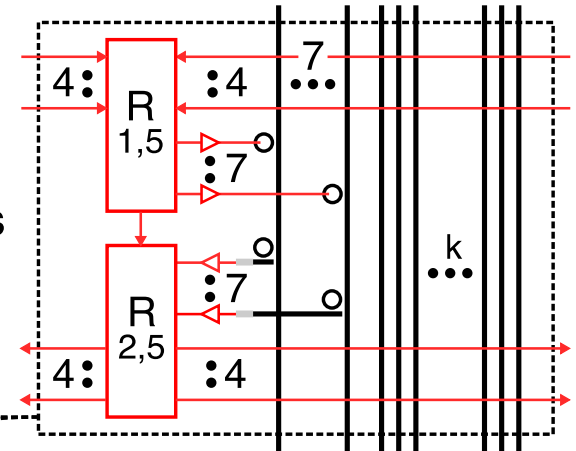
Physical Design for Butterfly



Architectural-Level
8-ary 2-fly Butterfly Topology

Microarchitectural-Level
Nanophotonic Channels, Electrical Routers

Physical-Level
Grid vs Serpentine Layout



Goals for Nanophotonic Network Research

Non-Goal

Photonic network A is 50% “better” than electrical network B

Goal #1

Develop design patterns and design guidelines that capture high-level design trade-offs and provide context for device-level researchers

Goal #2

Explore how this emerging and potentially disruptive technology can radically change high-performance system design

Past and Current Research

▶ Past Work

- ▷ Nanophotonic Processor-to-DRAM Networks [HOTI'08, IEEE Micro'09]
- ▷ Nanophotonic On-Chip Clos Network [NOCS'09]
- ▷ Nanophotonic DRAM Memory Channels [ISCA'10]
- ▷ Nanophotonic System-in-Package [WINDS'10]

▶ Current Work

- ▷ Design patterns/guidelines for nanophotonic interconnection networks
- ▷ More sophisticated models to bridge device-level to system-level gap
- ▷ Leveraging new nanophotonic devices
- ▷ Mitigating thermal sensitivity of silicon photonic devices
- ▷ Simple prototype nanophotonic networks