

FANGZHOU LIU

<https://www.cs.rochester.edu/u/fliu14/>
1446 30th Rd, Astoria, NY
(+1) 585-363-8290 ◊ fliu14@ur.rochester.edu

EDUCATION

M.S. and Ph.D in Computer Science

August 2016 - Present

Advisor: Prof. Chen Ding

University of Rochester, CGPA: 3.73/4.00

B.E. in Telecommunication Engineering

Sept 2012 - June 2016

Beijing University of Posts and Telecommunications, CGPA: 88.1/100

SKILLS AND INTERESTS

Skills C/C++, Python, Swift, Java, Ruby, LLVM, Mobile Apps Development(iOS),
SQL, Git, Pytorch

Interests Static Analysis and Optimization, Memory Locality Modeling for parallel program,
Heterogeneous Memory Systems

SELECTED WORKS

Compiler-assigned Reference Lease Cache

Sep. 2020 - Present

- Prove in mathematics the optimality of lease cache and its performance safety, do not introduces more cache misses than the LRU replacement policy.
- Conduct experiments on PolyBench showing our new lease cache scheme can achieve similar cache miss with OPT cache replacement policy.
- Coauthor two papers published in ISMM'21 and TACO'22.

Static locality analysis for data-parallel program (OpenMP)

Feb. 2019 - May. 2021

- Design and implement PLUSS, a static analysis framework to derive the cache miss ratio of OpenMP kernels.
- Design a new sampling scheme, Island-hopping, that addresses the repetitive iteration traversal issue observed in the SPS design. This new design beats the SPS sampling scheme by 4.5x in speed.
- Conduct experiments and do poster presentation in PPOPP'20, give talk at CnC'21 workshop and submit a paper to TACO (under-review)

Locality analysis using static sampling

May. 2017 - June. 2018

- Help build the branch analysis pass in the SPS compiler to correctly measure data reuses inside and across branch conditions.
- Do miss ratio comparison with memory profiling, coauthor a paper published in PLDI'18 and do poster presentation in MEMSYS'18.

INTERNSHIP

Interim Engineer Intern

May 2022 - August 2022

Qualcomm Inc. Santa Clara, CA

- Summary six memory access patterns and six memory access shapes by inspecting 33 machine learning kernels in AdrenoDNN and 12 representative Geekbench shaders written in OpenCL.
- Design and implement a framework inside the LLVM compiler using C++ to automatically detect the memory access pattern of each buffer at the compile-time and then plot the access shape of each buffer using Python and DOT language.

Interim Engineer Intern

June 2021 - September 2021

Qualcomm Inc. Santa Clara, CA

- Refactor loop optimization passes to make them applicable to graphic shaders.
- Design and implement locality analysis inside the LLVM compiler using C++ to detect suboptimal loop nests in graphic shaders written in OpenGL/Vulkan.

Research Intern

June 2020 - September 2020

Alibaba Group (U.S.) Inc. Bellevue, WA

- Build a light-weight runtime profiler in C/C++ that collects page hotness information. The profiler introduces less than 10% runtime overhead.
- Design and implement three algorithms to reduce the slow memory access ratio. These algorithms use the page hotness info to move pages on a heterogeneous memory system, which equips two types of memory with different access latency.

PUBLICATIONS

1. Chen Ding, Dong Chen, Fangzhou Liu, Benjamin Reber, and Wesley Smith. CARL: Compiler Assigned Reference Leasing
2. Dong Chen, Chen Ding, Fangzhou Liu, Benjamin Reber, Wesley Smith, and Pengcheng Li. Uniform Lease vs. LRU Cache: Analysis and Evaluation. In *Proceedings of the 2021 ACM SIGPLAN International Symposium on Memory Management, ISMM 2021*, pages 15–27, New York, NY, USA, 2021. Association for Computing Machinery
3. Fangzhou Liu, Dong Chen, Wesley Smith, and Chen Ding. POSTER:PLUM: Static Parallel Program Locality Analysis under Uniform Multiplexing. In *Proceedings of the 25th ACM SIGPLAN Symposium on Principles and Practice of Parallel Programming, PPOPP '20*, pages 437–438, 2020
4. Dong Chen, Fangzhou Liu, Chen Ding, and Sreepathi Pai. Locality Analysis Through Static Parallel Sampling. In *Proceedings of the 39th ACM SIGPLAN Conference on Programming Language Design and Implementation, PLDI 2018*, pages 557–570, 2018

PROFESSIONAL SERVICES

Artifact Evaluation Committee

CGO'20, CGO'19

External Reviewer

TACO, TPDS, ACA'20, IPDPS'20, LCPC'19, PMAP'19, ICS'18

Student Volunteer

ICS'18 PC Meeting

Department PhD Admission Committee

2019 – 2021

AWARDS

SIGPLAN PAC Travel Grants for PLDI 2018
SIGPLAN

June 2018

Outstanding graduates in Beijing University of Posts and Telecommunications
Beijing University of Posts and Telecommunications

June 2016